GR551x Datasheet Brief

Version: 2.1

Release Date: 2023-04-20

Shenzhen Goodix Technology Co., Ltd.

Contents

1 GR551x Overview

The Goodix GR551x family is a single-mode, low-power Bluetooth 5.1 System-on-Chip (SoC). It can be configured as a Broadcaster, an Observer, a Central, or a Peripheral and supports the combination of all the above roles, making it an ideal choice for Internet of Things (IoT) and smart wearable devices.

Based on ARM® Cortex®-M4F CPU core, the GR551x series integrates Bluetooth 5.1 Protocol Stack, a 2.4 GHz RF transceiver, on-chip programmable Flash memory, RAM, and multiple peripherals.

GR551x SoCs are available in multiple packages (see Table 1-1) that meet your diverse project demands.

Table 1-1 GR551x series

Features	GR5515IGND	GR5515IENDU	GR5515I0NDA	GR5515RGBD	GR5515GGBD	GR5513BEND	GR5513BENDU
CPU	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F
RAM	256 KB	256 KB	256 KB	256 KB	256 KB	128 KB	128 KB
SiP Flash	1 MB	512 KB	N/A	1 MB	1 MB	512 KB	512 KB
I/O Number	39	39	39	39	29	22	22
Package (mm)	QFN56 (7 x 7 x 0.75)	QFN56 (7 x 7 x 0.75)	QFN56 (7 x 7 x 0.75)	BGA68 (5.3 x 5.3 x 0.88)	BGA55 (3.5 x 3.5 x 0.60)	QFN40 (5 x 5 x 0.75)	QFN40 (5 x 5 x 0.75)

Note:

GR5515IENDU and GR5513BENDU are embedded with wide-voltage Flash, with Flash power supply from 1.65 V to 3.6 V.

1.1 Features

- A Bluetooth Low Energy (Bluetooth LE) 5.1 transceiver integrates Controller and Host layers
  - Supported data rates: 1 Mbps, 2 Mbps, and Long Range (500 kbps, 125kbps)
  - TX power: -20 dBm to +7 dBm
  - -96 dBm sensitivity (in 1 Mbps mode)
  - -93 dBm sensitivity (in 2 Mbps mode)
  - -99 dBm sensitivity (in Long Range 500 kbps mode)
  - -102 dBm sensitivity (in Long Range 125 kbps mode)
  - TX current: 5.6 mA @ 0 dBm, 1 Mbps
  - RX current: 4.8 mA @ 1 Mbps
- ARM® Cortex®-M4F 32-bit micro-processor with floating point support
  - Up to 64 MHz clock frequency

- Built-in Memory Protection Unit (MPU) supporting eight programmable regions
- Hardware Floating Point Unit (FPU)
- Built-in Nested Vectored Interrupt Controller (NVIC)
- Non-maskable Interrupt (NMI) input
- Serial Wire Debug (SWD) with 6 breakpoints, two watchpoints, and a debug timestamp counter
- 51 µA/MHz execution from Flash @ 3.3 V, 64 MHz

- On-chip memory
  - 256 KB SRAM with retention capabilities (four 8 KB SRAM blocks and seven 32 KB SRAM blocks) for GR5515 series SoCs, and 128 KB SRAM with retention capabilities (four 8 KB SRAM blocks and three 32 KB SRAM blocks) for the GR5513 SoC
  - 8 KB cache SRAM with retention capabilities
  - Stack ROM (including boot ROM and Bluetooth LE Stack)
  - 1 MB internal QSPI Flash for GR5515 series SoCs and 512 KB internal QSPI Flash for the GR5513 SoC (exceptions: GR5515I0NDA requiring external QSPI Flash and GR5515IENDU requiring 512 KB embedded Flash)
- Digital peripherals
  - One general-purpose DMA engine with 8 channels and 16 handshaking interfaces
- Analog peripherals
  - One 13-bit Sense ADC with the sampling rate of 1 Msps. It supports up to five external I/O channels and three internal signal channels
  - Built-in temperature and voltage sensors
  - Low-power comparator, supporting wakeup from deep sleep mode
- Flexible serial peripherals
  - 2 x QSPI interfaces, up to 32 MHz
  - 2 x UART modules up to 4 Mbps, with all modules supporting flow control and only UART0 supporting DMA
  - 2 x I2C modules for peripheral communication, up to 2 MHz
  - 1x SPI master interface and 1 x SPI slave interface for host communication, up to 32 MHz
  - 2 x I2S interfaces (1 I2S master interface + 1 I2S slave interface)
  - ISO 7816 interface
- Security
  - Complete secure computing engine:
    - AES 128-bit/192-bit/256-bit symmetric encryption (ECB, CBC)

        - Hash-based Message Authentication Code (HMAC-SHA256)
        - Public key cryptography (PKC)
        - True random number generator (TRNG)
    - Comprehensive security operation mechanism:
        - Secure boot
        - Encrypted firmware running directly from Flash
        - eFuse for encrypted key storage
        - Differentiate application data key and firmware key, supporting one data key per device/product
- I/O peripherals
    - 39 I/O pins in total
        - 26 general-purpose I/O (GPIO) pins
        - 8 always-on I/O (AON IO) pins, supporting wakeup from deep sleep mode
        - 5 mixed signal I/O (MSIO) pins, configurable to be digital/analog signal interface
- Timer
    - Two general-purpose, 32-bit timer modules
    - A timer module composed of two programmable 32-bit or 16-bit down counters
    - An internal sleep timer that can be used to wake the device up from deep sleep mode
    - Two PWM modules with edge alignment mode and center alignment mode, each with 3 channels
    - 1 x real-time counter (RTC), can be used as Calendar
    - 1 x AON watchdog timer, working in both system sleep and active status
- Power management
    - On-chip DC-DC to provide RF Analog voltage and supply core LDO
    - On-chip I/O LDO to provide I/O voltage and supply external components, maximum I/O LDO drive strength: 30 mA
    - Programmable thresholds for brownout detection (BoD reset and BoD interrupt)
    - Supply voltage: 2.2 V to 3.8 V. The supply voltage of GR5515I0NDA (when the external Flash of GR5515I0NDA is supplied by high voltage) shall equal the working voltage of the external QSPI Flash
    - I/O voltage: 1.8 V to 3.3 V (Typical) (for GR5515I0NDA/GR5515IENDU/GR5513BENDU Flash using high voltage, the VIO_LDO_OUT shall be connected to VBATL in schematic circuit.)
- Low-power consumption modes
    - Deep sleep mode: 2.7 µA (Typical), with full 256 KB SRAM retention

- Ultra deep sleep mode: 1.8 µA (Typical), no SRAM retention
- Off mode: 0.15 uA (Typical), nothing on except VBAT, and chip in reset mode

- Packages
  - QFN56: 7 mm x 7 mm, 0.40 mm pitch
  - BGA68: 5.3 mm x 5.3 mm, 0.50 mm pitch
  - BGA55: 3.5 mm x 3.5 mm, 0.40 mm pitch
  - QFN40: 5 mm x 5 mm, 0.40 mm pitch
- Operating temperature range: -40°C to +85°C

1.2 Block Diagram

Figure 1-1 shows the block diagram of GR551x.

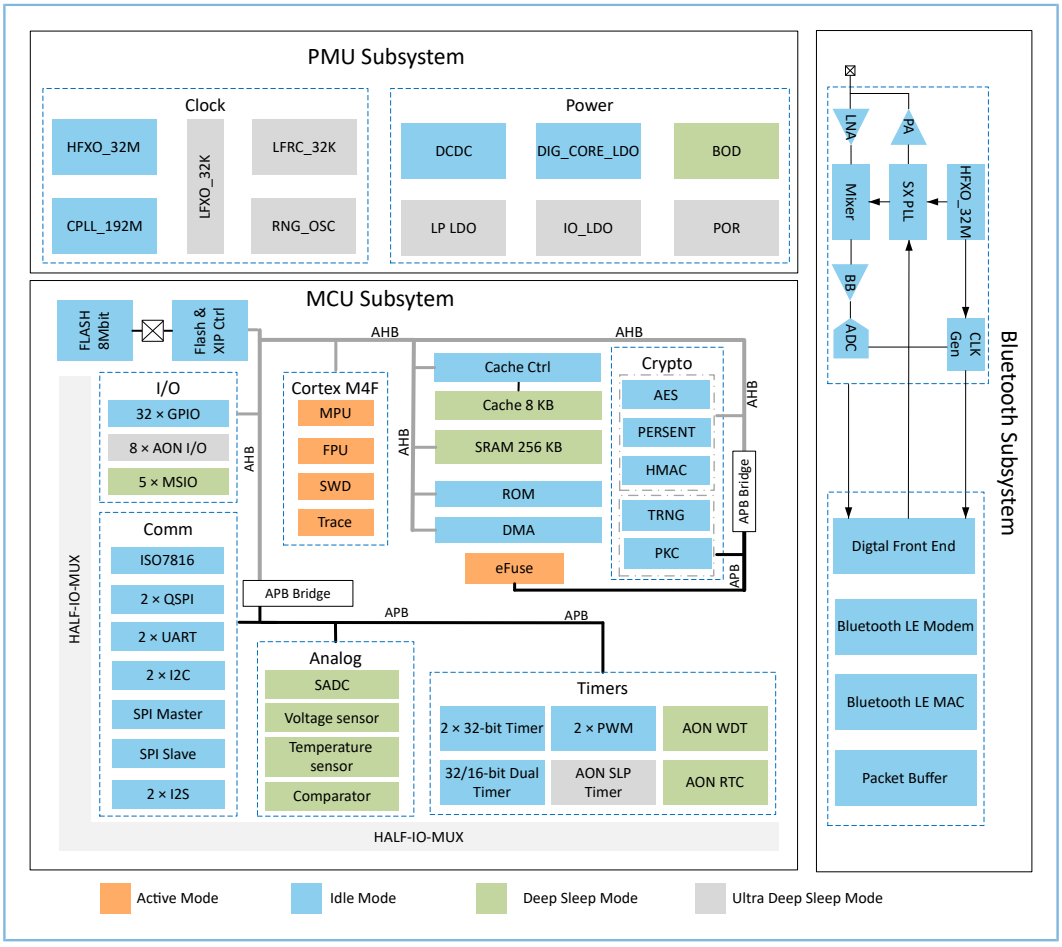

Figure 1-1 GR551x block diagram

- Bluetooth Subsystem
  - A 2.4 GHz transceiver and a digital communication core that supports Bluetooth LE 5.1.

- MCU Subsystem
  - An ARM® Cortex®-M4F with all the required memories and peripherals.
  - Security cores that can be used for application security and to secure boot implementation.
- Power Management Unit (PMU) Subsystem
  - All the required power management modules to supply sufficient power to both internal modules and external peripherals.
  - Modules required for ultra-low-power operation are in standby mode. CPLL_192M, RNG_OSC, LFRC_32K, wakeup GPIOs (Wake up), low-power comparator (LP Comp.), and power state controller (Power Sequencer) are used to control the state of different modules.

1.3 Applications

GR551x can be used in rich sets of applications. Examples of these applications include:

- Wearables
  - Sport bracelet
  - Smart watch
- Bluetooth HID devices
  - Voice remote control
  - Keyboard/Mouse
  - Gaming controller
  - Stylus pen
- IoT applications
  - Smart home
  - Electronic shelf label (ESL)
  - Beacon
  - Tire pressure monitoring system (TPMS)
  - Mesh applications
  - Asset tracking

2 Pinout

This chapter introduces GR551x pinout available in multiple packages and provides detailed descriptions.

2.1 GR5515IGND/GR5515IENDU QFN56

Figure 2-1 shows the pin assignments of GR5515IGND/GR5515IENDU QFN56 package (top view).

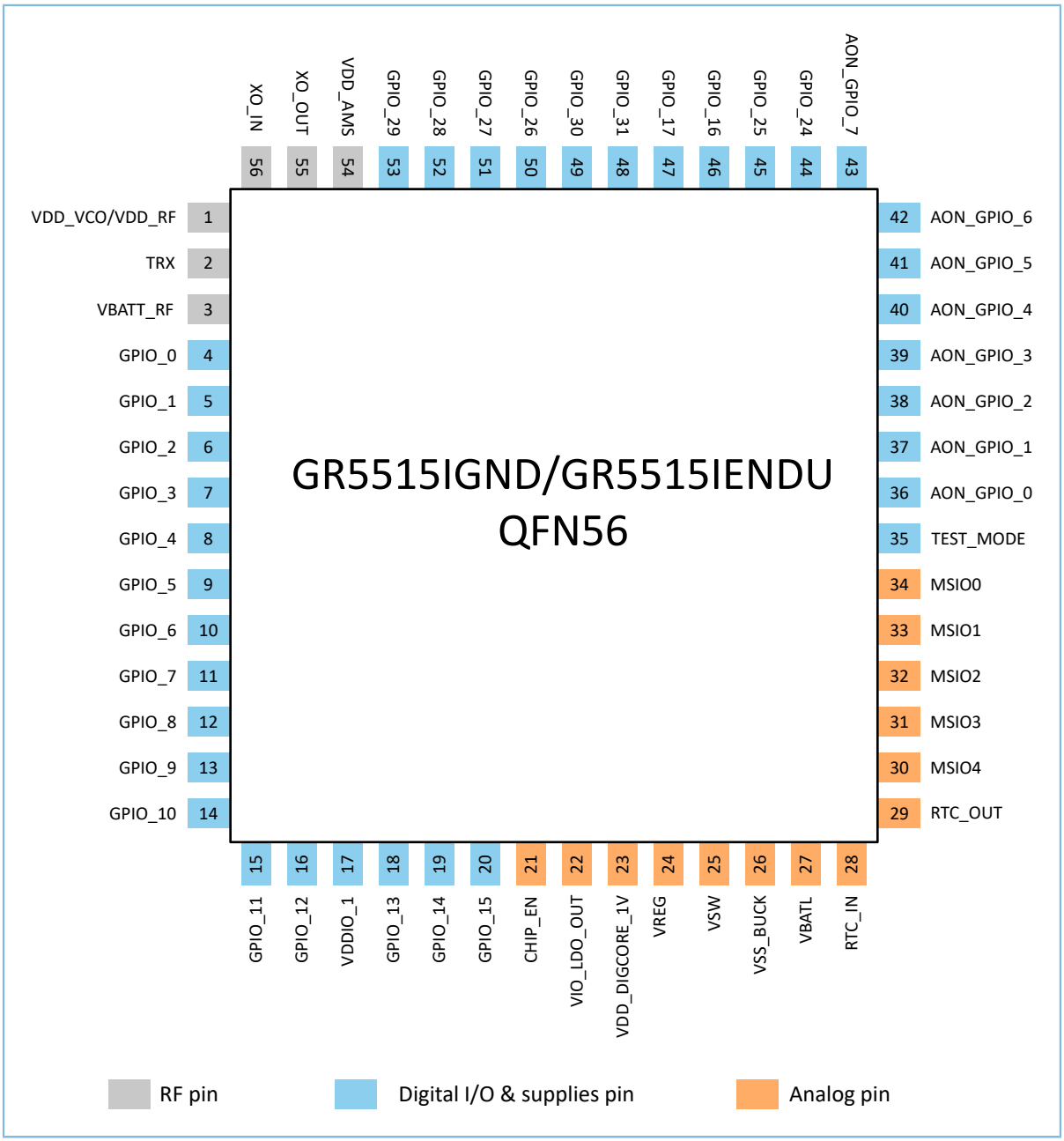

Figure 2-1 GR5515IGND/GR5515IENDU QFN56 package pinout

Table 2-1 shows pin descriptions of GR5515IGND/GR5515IENDU QFN56 package.

Table 2-1 GR5515IGND/GR5515IENDU QFN56 pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG.	
2	TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF Supply	Connect to VBATL.	
4	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 2 mA.	VDDIO1
5	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 2 mA.	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
12	GPIO_8	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
13	GPIO_9	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
14	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
15	GPIO_11	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
16	GPIO_12	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
17	VDDIO_1	Digital I/O supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
18	GPIO_13	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
19	GPIO_14	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
20	GPIO_15	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
21	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL. Minimum value of high level for CHIP_EN is 1 V.	
22	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator When GR5515IENDU is used and the Flash is supplied at a high voltage, the pin is used as the power input pin of VDDIO0 digital I/O domain by being connected to VBATL	Connected internally to VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
23	VDD_DIGCORE_1V	PMU	On-chip LDO output for digital core. Connect to a 1 µF capacitor.	
24	VREG	PMU	Feedback pin from switching regulator	
25	VSW	PMU	DC-DC converter switching node	
26	VSS_BUCK	PMU	DC-DC converter supply and general battery GND	
27	VBATL	PMU	Power supply: 2.2 V to 3.8 V	
28	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
29	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
30	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
31	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
32	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
33	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
34	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
35	TEST_MODE	Digital I/O	Factory test mode selection pin • 1: test mode • 0: normal operation mode	VDDIO0
36	AON_GPIO_0	Digital I/O	Always-on GPIO	VDDIO0
37	AON_GPIO_1	Digital I/O	Always-on GPIO	VDDIO0
38	AON_GPIO_2	Digital I/O	Always-on GPIO	VDDIO0
39	AON_GPIO_3	Digital I/O	Always-on GPIO	VDDIO0
40	AON_GPIO_4	Digital I/O	Always-on GPIO	VDDIO0
41	AON_GPIO_5	Digital I/O	Always-on GPIO	VDDIO0
42	AON_GPIO_6	Digital I/O	Always-on GPIO	VDDIO0
43	AON_GPIO_7	Digital I/O	Always-on GPIO	VDDIO0
44	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
45	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
46	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
47	GPIO_17	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
48	GPIO_31	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
49	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
50	GPIO_26	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
51	GPIO_27	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
52	GPIO_28	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
53	GPIO_29	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
54	VDD_AMS	Analog/RF Supply	AMS supply 1.1 V; connect to VREG.	
55	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
56	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

2.2 GR5515I0NDA QFN56

Figure 2-2 shows the pin assignments of GR5515I0NDA QFN56 package (top view).

The pins (Pin 43 to Pin 53) of GR5515I0NDA QFN56 package are different from those of GR5515IGND/GR5515IENDU QFN56 package.

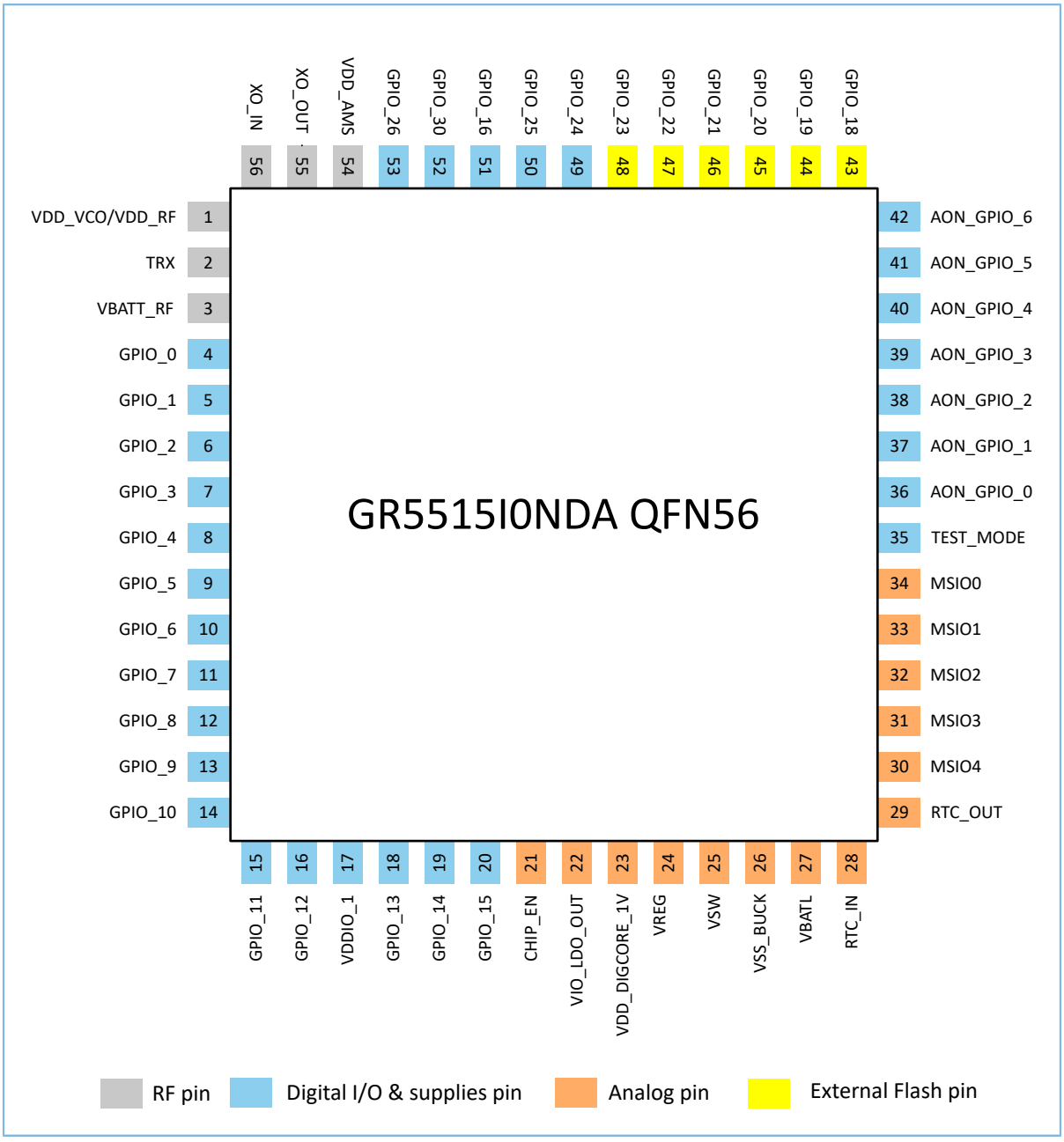

Figure 2-2 GR5515I0NDA QFN56 package pinout

Table 2-2 shows pin descriptions of GR5515I0NDA QFN56 package.

Table 2-2 GR5515I0NDA QFN56 pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG.	
2	TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF Supply	Connect to VBATL.	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
4	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 2 mA.	VDDIO1
5	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 2 mA.	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
12	GPIO_8	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
13	GPIO_9	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
14	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
15	GPIO_11	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
16	GPIO_12	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
17	VDDIO_1	Digital I/O supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
18	GPIO_13	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
19	GPIO_14	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
20	GPIO_15	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
21	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL.	
22	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator; when GR5515I0NDA is used (high Flash supply voltage for GR5515I0NDA), the pin is used as power input pin of VDDIO0 digital IO domain by being connected to VBATL	Connected internally to VDDIO0
23	VDD_DIGCORE_1V	PMU	On-chip LDO output for digital core. Connect to a 1 µF capacitor.	
24	VREG	PMU	Feedback pin from switching regulator	
25	VSW	PMU	DC-DC converter switching node	
26	VSS_BUCK	PMU	DC-DC converter supply and general battery GND	
27	VBATL	PMU	Power supply: 2.2 V to 3.8 V	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
28	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
29	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
30	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
31	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
32	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
33	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
34	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
35	TEST_MODE	Digital I/O	Factory test mode selection pin • 1: test mode • 0: normal operation mode	VDDIO0
36	AON_GPIO_0	Digital I/O	Always-on GPIO	VDDIO0
37	AON_GPIO_1	Digital I/O	Always-on GPIO	VDDIO0
38	AON_GPIO_2	Digital I/O	Always-on GPIO	VDDIO0
39	AON_GPIO_3	Digital I/O	Always-on GPIO	VDDIO0
40	AON_GPIO_4	Digital I/O	Always-on GPIO	VDDIO0
41	AON_GPIO_5	Digital I/O	Always-on GPIO	VDDIO0
42	AON_GPIO_6	Digital I/O	Always-on GPIO	VDDIO0
43	GPIO_18	Digital I/O	Connect to an external Flash	VDDIO0
44	GPIO_19	Digital I/O	Connect to an external Flash	VDDIO0
45	GPIO_20	Digital I/O	Connect to an external Flash	VDDIO0
46	GPIO_21	Digital I/O	Connect to an external Flash	VDDIO0
47	GPIO_22	Digital I/O	Connect to an external Flash	VDDIO0
48	GPIO_23	Digital I/O	Connect to an external Flash	VDDIO0
49	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
50	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
51	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
52	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
53	GPIO_26	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
54	VDD_AMS	Analog/RF Supply	AMS supply 1.1 V; connect to VREG.	
55	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
56	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

2.3 GR5515RGBD BGA68

Figure 2-3 shows the pin assignments of GR5515RGBD BGA68 package (top view).

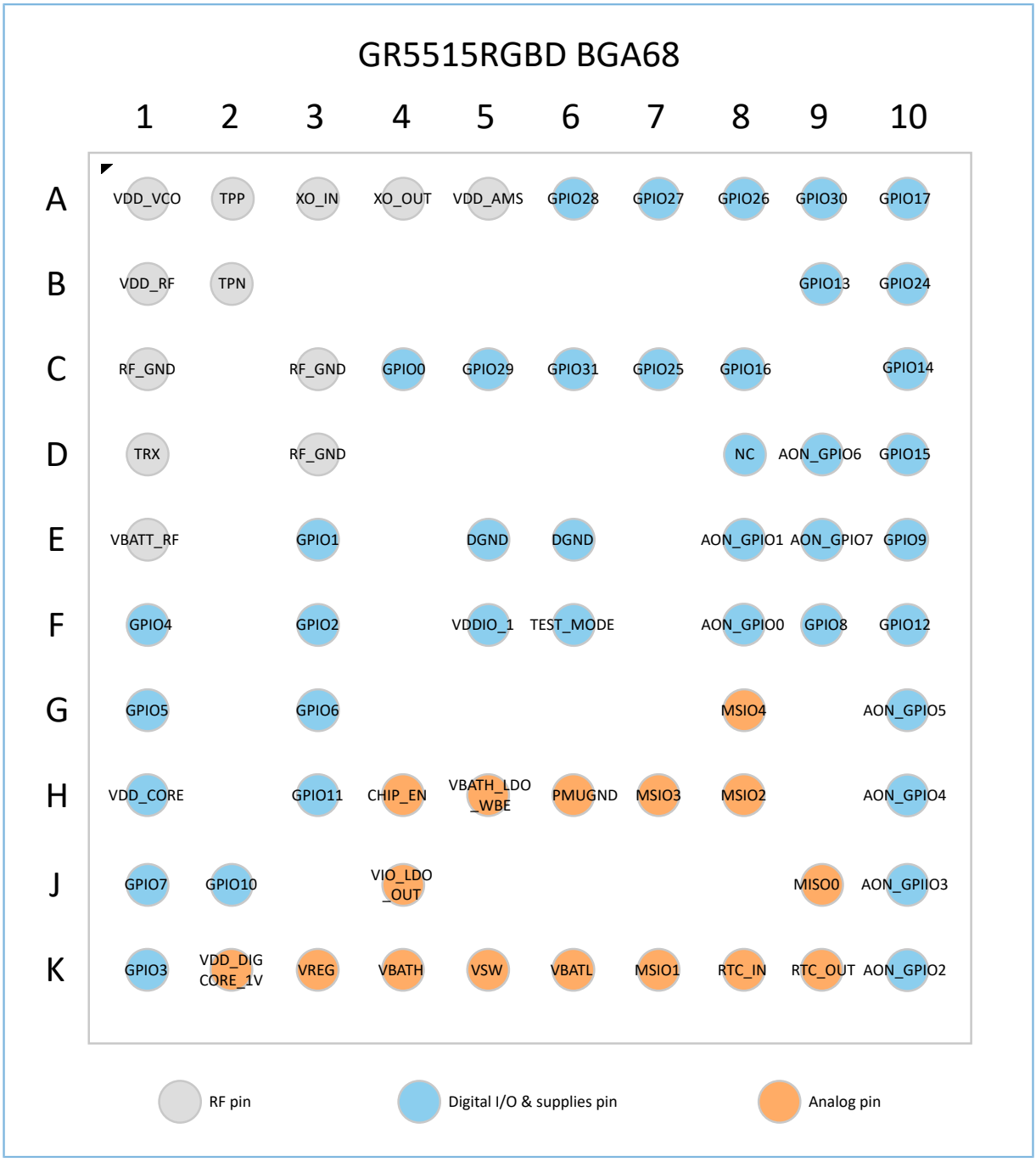

Figure 2-3 GR5515RGBD BGA68 package pinout

Table 2-3 shows pin descriptions of GR5515RGBD BGA68 package.

Table 2-3 GR5515RGBD BGA68 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A1	VDD_VCO	Analog/RF supply	Synthesizer VCO supply: 1.1 V; connect to VREG	
A2	TPP	Analog/RF	Test Mux +output	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A3	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
A4	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
A5	VDD_AMS	Analog/RF	AMS supply 1.1 V; connect to VREG	
A6	GPIO28	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
A7	GPIO27	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
A8	GPIO26	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
A9	GPIO30	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
A10	GPIO17	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
B1	VDD_RF	Analog/RF	RF supply: 1.1 V; connect to VREG	
B2	TPN	Analog/RF	Test Mux - output	
B9	GPIO13	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
B10	GPIO24	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
C1	RF_GND	Analog/RF	RF ground	
C3	RF_GND	Analog/RF	RF ground	
C4	GPIO0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 2 mA.	VDDIO1
C5	GPIO29	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
C6	GPIO31	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
C7	GPIO25	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
C8	GPIO16	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
C10	GPIO14	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
D1	TRX	Analog/RF	RX input and TX output	
D3	RF_GND	Analog/RF	RF ground	
D8	NC	-	-	
D9	AON_GPIO6	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
D10	GPIO15	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
E1	VBATT_RF	Analog/RF	Connect to VBATL	
E3	GPIO1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 2 mA.	VDDIO1
E5	DGND	Digital GND	Digital Ground	
E6	DGND	Digital GND	Digital Ground	
E8	AON_GPIO1	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
E9	AON_GPIO7	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
E10	GPIO9	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
F1	GPIO4	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
F3	GPIO2	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
F5	VDDIO_1	Digital Supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
F6	TEST_MODE	Digital I/O	Factory test mode selection pin • 1: test mode • 0: normal operation mode	VDDIO0
F8	AON_GPIO0	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
F9	GPIO8	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
F10	GPIO12	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
G1	GPIO5	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
G3	GPIO6	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
G8	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G10	AON_GPIO5	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
H1	VDD_CORE	Digital Supply	Digital core supply	
H3	GPIO11	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
H4	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL.	
H5	VBATH_LDO_WBE	Analog/PMU	Connect to GND.	
H6	PMUGND	Analog/PMU	DC-DC converter supply & general battery GND	
H7	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H8	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H10	AON_GPIO4	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
J1	GPIO7	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
J2	GPIO10	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
J4	VIO_LDO_OUT	Analog/PMU	Output of On-Chip I/O supply regulator.	Connected internally to VDDIO0
J9	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
J10	AON_GPIO3	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
K1	GPIO3	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
K2	VDD_DIGCORE_1V	Analog/PMU	On-chip LDO output for digital core, connected to 1 µF capacitor	
K3	VREG	Analog/PMU	Feedback pin of switch regulator	
K4	VBATH	Analog/PMU	Connect to VBATL	
K5	VSW	Analog/PMU	DC-DC Converter Switching Node	
K6	VBATL	Analog/PMU	Power supply: 2.2 V to 3.8 V	
K7	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
K8	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
K9	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
K10	AON_GPIO2	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0

2.4 GR5515GGBD BGA55

Figure 2-4 shows the pin assignments of GR5515GGBD BGA55 package (top view).

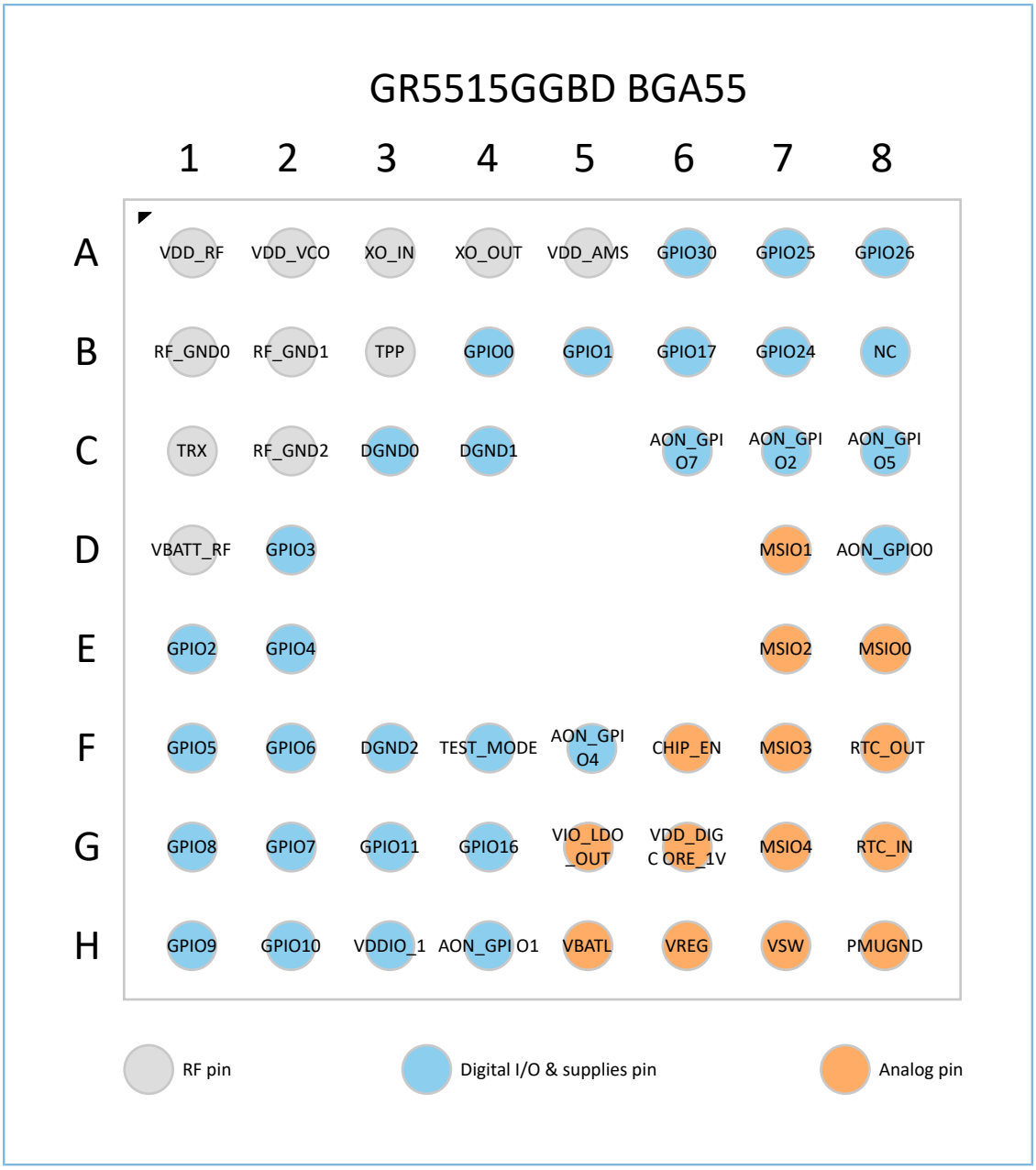

Figure 2-4 GR5515GGBD BGA55 package pinout

Table 2-4 shows pin descriptions of GR5515GGBD BGA55 package.

Table 2-4 GR5515GGBD BGA55 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A1	VDD_RF	Analog/RF supply	RF supply: 1.1 V	
A2	VDD_VCO	Analog/RF supply	Synthesizer VCO supply; connect to VREG	
A3	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A4	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
A5	VDD_AMS	Analog/RF supply	AMS supply 1.1 V; connect to VREG	
A6	GPIO30	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
A7	GPIO25	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
A8	GPIO26	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
B1	RF_GND0	Analog/RF	RF ground	
B2	RF_GND1	Analog/RF	RF ground	
B3	TPP	Analog/RF	Test Mux + output	
B4	GPIO0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 2 mA.	VDDIO1
B5	GPIO1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 2 mA.	VDDIO1
B6	GPIO17	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
B7	GPIO24	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
B8	NC	-	-	
C1	TRX	Analog/RF	RX input and TX output	
C2	RF_GND2	Analog/RF	RF ground	
C3	DGND0	Digital GND	Digital ground	
C4	DGND1	Digital GND	Digital ground	
C6	AON_GPIO7	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
C7	AON_GPIO2	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
C8	AON_GPIO5	Digital I/O	Always-on general purpose I/O	VDDIO0
D1	VBATT_RF	Analog/RF supply	Connect to VBATL	
D2	GPIO3	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
D7	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
D8	AON_GPIO0	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
E1	GPIO2	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
E2	GPIO4	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
E7	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
E8	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
F1	GPIO5	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
F2	GPIO6	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
F3	DGND2	Digital GND	Digital ground	
F4	TEST_MODE	Digital I/O	Factory test mode selection pin • 1: test mode • 0: in normal operation mode.	VDDIO0
F5	AON_GPIO4	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
F6	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL.	
F7	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
F8	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
G1	GPIO8	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
G2	GPIO7	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
G3	GPIO11	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
G4	GPIO16	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
G5	VIO_LDO_OUT	Analog/PMU	Output of On-Chip I/O supply regulator	Connected internally to VDDIO0
G6	VDD_DIGCORE_1V	Analog/PMU	On-chip LDO output for digital core, connected to 1 µF capacitor	
G7	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G8	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
H1	GPIO9	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
H2	GPIO10	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
H3	VDDIO_1	Digital I/O supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
H4	AON_GPIO1	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
H5	VBATL	Analog/PMU	Power supply: 2.2 V to 3.8 V	
H6	VREG	Analog/PMU	Feedback pin of switch regulator	
H7	VSW	Analog/PMU	DC-DC converter switching node	
H8	PMUGND	Analog/PMU	DC-DC converter & general battery GND pin	

2.5 GR5513BEND (NRND)/GR5513BENDU QFN40

Figure 2-5 shows the pinout of GR5513BEND/GR5513BENDU QFN40 package (top view).

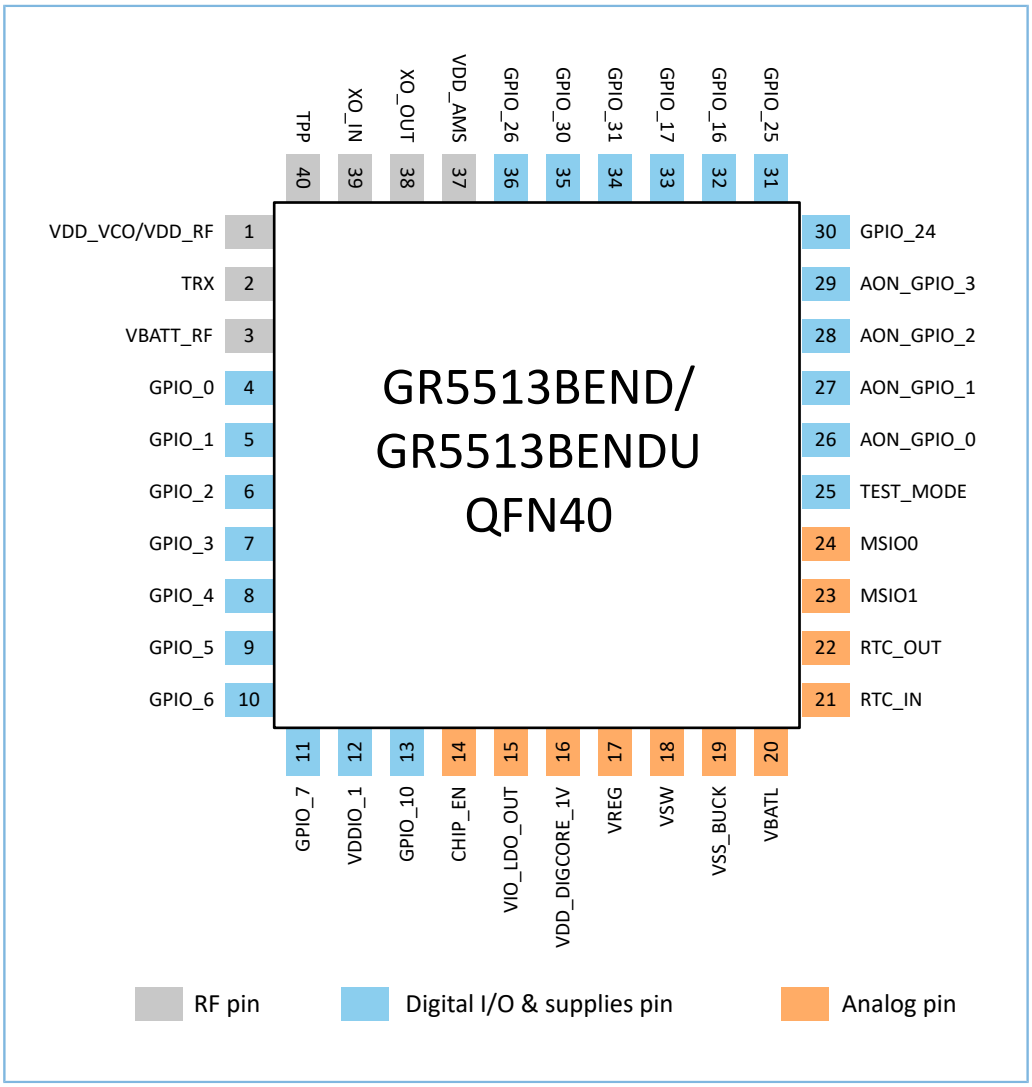

Figure 2-5 GR5513BEND/GR5513BENDU QFN40 package pinout

Table 2-5 shows pin descriptions of GR5513BEND/GR5513BENDU QFN40 package.

Table 2-5 GR5513BEND/GR5513BENDU QFN40 pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG.	
2	TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF	Connect to VBATL.	
4	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 2 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
5	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 2 mA.	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
12	VDDIO_1	Digital I/O Supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
13	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO1
14	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL.	
15	VIO_LDO_OUT	Analog/PMU	Output of on-chip I/O supply regulator. For GR5513BENDU, power input pin of VDDIO0 digital IO domain. When VDDIO0 is set to 3.3 V/ VBATL, VIO_LDO_OUT should be connected to 3.3 V/VBATL.	Connected internally to VDDIO0
16	VDD_DIGCORE_1V	Analog/PMU	On-chip LDO output for digital core. Connect to a 1 µF capacitor.	
17	VREG	Analog/PMU	Feedback pin from switching regulator	
18	VSW	Analog/PMU	DC/DC converter switching node	
19	VSS_BUCK	Analog/PMU	DC/DC converter supply and general battery GND	
20	VBATL	Analog/PMU	Power supply: 2.2 V to 3.8 V	
21	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
22	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
23	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
24	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
25	TEST_MODE	Digital I/O	Factory test mode selection pin	VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
			• 1: test mode • 0: normal operation mode.	
26	AON_GPIO_0	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
27	AON_GPIO_1	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
28	AON_GPIO_2	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
29	AON_GPIO_3	Digital I/O	Always-on GPIO; pad drive level is 2 mA.	VDDIO0
30	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
31	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
32	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
33	GPIO_17	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
34	GPIO_31	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
35	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 2 mA.	VDDIO0
36	GPIO_26	Digital I/O	General purpose I/O	VDDIO0
37	VDD_AMS	Analog/RF	AMS supply 1.1 V; connect to VREG.	
38	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
39	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
40	TPP	Analog/RF	Test Mux + output	

2.6 I/O Properties

Table 2-6 I/O properties

Index	Pin Name	Default Status After POR	Pullup/ Pulldown Enable After POR	Pullup/ Pulldown Selection After POR	Pin Interrupt	Wakeup Chip	Sleep Retention
1	AON_GPIO0	L	Y	PD	Y	Y	Y
2	AON_GPIO1	L	Y	PD	Y	Y	Y
3	AON_GPIO2	L	Y	PD	Y	Y	Y
4	AON_GPIO3	L	Y	PD	Y	Y	Y
7	AON_GPIO4	L	Y	PD	Y	Y	Y
8	AON_GPIO5	L	Y	PD	Y	Y	Y
5	AON_GPIO6	L	Y	PD	Y	Y	Y
6	AON_GPIO7	L	Y	PD	Y	Y	Y

Index	Pin Name	Default Status After POR	Pullup/ Pulldown Enable After POR	Pullup/ Pulldown Selection After POR	Pin Interrupt	Wakeup Chip	Sleep Retention
9	GPIO0	L	Y	PD	Y	N	Y
10	GPIO1	L	Y	PD	Y	N	Y
11	GPIO2	L	Y	PD	Y	N	Y
12	GPIO3	L	Y	PD	Y	N	Y
13	GPIO4	L	Y	PD	Y	N	Y
14	GPIO5	L	Y	PD	Y	N	Y
15	GPIO6	L	Y	PD	Y	N	Y
16	GPIO7	L	Y	PD	Y	N	Y
17	GPIO8	L	Y	PD	Y	N	Y
18	GPIO9	L	Y	PD	Y	N	Y
19	GPIO10	L	Y	PD	Y	N	Y
20	GPIO11	L	Y	PD	Y	N	Y
21	GPIO12	L	Y	PD	Y	N	Y
22	GPIO13	L	Y	PD	Y	N	Y
23	GPIO14	L	Y	PD	Y	N	Y
24	GPIO15	L	Y	PD	Y	N	Y
25	GPIO16	L	Y	PD	Y	N	Y
26	GPIO17	L	Y	PD	Y	N	Y
27	GPIO24	L	Y	PD	Y	N	Y
28	GPIO25	L	Y	PD	Y	N	Y
29	GPIO26	L	Y	PD	Y	N	Y
30	GPIO27	L	Y	PD	Y	N	Y
31	GPIO28	L	Y	PD	Y	N	Y
32	GPIO29	L	Y	PD	Y	N	Y
33	GPIO30	L	Y	PD	Y	N	Y
34	GPIO31	L	Y	PD	Y	N	Y
35	MSIO0	L	Y	PD	N	N	Y
36	MSIO1	L	Y	PD	N	N	Y
37	MSIO2	L	Y	PD	N	N	Y
38	MSIO3	L	Y	PD	N	N	Y
39	MSIO4	L	Y	PD	N	N	Y

Table 2-7 Abbreviations related to pin properties

Properties	Abbreviation	Description
Default status after POR	Hi-Z	High impedance
	H	High level
	L	Low level
Pullup/Pulldown enable after POR	Y	Enabled
	N	Disabled
Pullup/Pulldown selection after POR	PU	Pullup
	PD	Pulldown
Pin interrupt	N	No
	Y	Yes

3 Pin Mux

3.1 Introduction

GR551x has a configurable pin multiplexing module (Pin Mux) which can bring different peripherals on different GPIOs.

3.2 Main Features

Each of the GPIO, AON_GPIO, and MSIO pads can be configured to connect to 1 of 8 choices (MUX_0 – MUX_7) of internal signals by programming the DPAD_MUX_SEL_*, AON_PAD_MUX_SEL_*, and MSIO_MUX_SEL_* registers, respectively.

3.3 Functional Description

The pin multiplexing choices for all pads are shown in:

- Table 3-1 (GPIO_0 – GPIO_7)
- Table 3-2 (GPIO_8 – GPIO_15)
- Table 3-3 (GPIO_16 – GPIO_23)
- Table 3-4 (GPIO_24 – GPIO_31)
- Table 3-5 (MSIO_0 – MSIO_4)
- Table 3-6 (AON_GPIO_0 – AON_GPIO_7)

Basically,

- GPIO_0 - GPIO_15 are supplied by VDDIO_1
- GPIO_16 - GPIO_31 are supplied by VDDIO_0

There are 8 mux options (from MUX_0 to MUX_7) in the pin mux tables as follows.

Table 3-1 Pin multiplexing for GPIO_0 – GPIO_7

	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_4	GPIO_5	GPIO_6	GPIO_7
MUX_0	SWD_CLK	SWD_IO	UART0_CTS	UART0_TX	UART0_RX	UART0_RTS	I2S_M_WS	I2S_M_SDO
MUX_1	I2C0_SCL	I2C0_SDA	SIM_PRESENCE	SIM_RST	SIM_IO	SIM_CLK	I2S_S_WS	I2S_S_SDO
MUX_2	I2C1_SCL	I2C1_SDA	SWO	SPI_M_CLK	SPI_M_MOSI	SPI_M_MISO	SPI_M_CS0	SPI_M_CS1
MUX_3	UART1_RTS	UART1_CTS	SPI_S_CS	SPI_S_CLK	SPI_S_MISO	SPI_S_MOSI	UART1_RX	UART1_TX
MUX_4	UART0_TX	UART0_RX	I2C0_SDA	SPI_M_CS1	SPI_M_CS0	SPI_M_MISO	SPI_M_MOSI	SPI_M_CLK
MUX_5	UART1_TX	UART1_RX	PWM0_A	PWM0_B	PWM0_C	I2C0_SCL	I2C0_SDA	PWM1_A
MUX_6	UART0_RTS	UART0_CTS	-	-	-	-	-	-
MUX_7	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_4	GPIO_5	GPIO_6	GPIO_7

Table 3-2 Pin multiplexing for GPIO_8 – GPIO_15

	GPIO_8	GPIO_9	GPIO_10	GPIO_11	GPIO_12	GPIO_13	GPIO_14	GPIO_15
MUX_0	XQSPI_IO0	XQSPI_CLK	I2S_M_SDI	I2S_M_SCLK	XQSPI_IO3	XQSPI_IO2	XQSPI_IO1	XQSPI_CS
MUX_1	I2C1_SDA	I2C1_SCL	I2S_S_SDI	I2S_S_SCLK	SPI_M_CLK	SPI_M_MOSI	SPI_M_MISO	SPI_M_CS0
MUX_2	QSPI1_IO0	QSPI1_CLK	UART0_TX	UART0_RX	QSPI1_IO3	QSPI1_IO2	QSPI1_IO1	QSPI1_CS
MUX_3	UART1_RX	UART1_TX	-	-	SIM_PRESENCE	SIM_RST	SIM_IO	SIM_CLK
MUX_4	-	-	I2C0_SCL	I2C0_SDA	I2S_M_WS	I2S_M_SDO	I2S_M_SDI	I2S_M_SCLK
MUX_5	PWM1_B	PWM1_C	PWM1_B	PWM1_C	I2S_S_WS	I2S_S_SDO	I2S_S_SDI	I2S_S_SCLK
MUX_6	-	-	-	-	SPI_S_CS	SPI_S_CLK	SPI_S_MISO	SPI_S_MOSI
MUX_7	GPIO_8	GPIO_9	GPIO_10	GPIO_11	GPIO_12	GPIO_13	GPIO_14	GPIO_15

Table 3-3 Pin multiplexing for GPIO_16 – GPIO_23

	GPIO_16	GPIO17	GPIO_18	GPIO_19	GPIO_20	GPIO_21	GPIO_22	GPIO_23
MUX_0	SPI_M_MISO	SPI_M_CS0	QSPI0_CS	QSPI0_IO3	QSPI0_CLK	QSPI0_IO2	QSPI0_IO1	QSPI0_IO0
MUX_1	SPI_S_MOSI	SPI_S_CS	XQSPI_CS	XQSPI_IO3	XQSPI_CLK	XQSPI_IO2	XQSPI_IO1	XQSPI_IO0
MUX_2	SIM_IO	SIM_CLK	-	-	-	-	-	-
MUX_3	I2S_M_SDI	I2S_M_SCLK	-	-	-	-	-	-
MUX_4	I2S_S_SDI	I2S_S_SCLK	-	-	-	-	-	-
MUX_5	QSPI0_IO1	QSPI0_IO2	-	-	-	-	-	-
MUX_6	-	-	-	-	-	-	-	-
MUX_7	GPIO_16	GPIO_17	GPIO_18	GPIO_19	GPIO_20	GPIO_21	GPIO_22	GPIO_23

Table 3-4 Pin multiplexing for GPIO_24 – GPIO_31

	GPIO_24	GPIO_25	GPIO_26	GPIO_27	GPIO_28	GPIO_29	GPIO_30	GPIO_31
MUX_0	SPI_M_CLK	SPI_M_MOSI	I2C1_SDA	-	-	-	I2C1_SCL	SPI_M_CS1
MUX_1	SPI_S_CLK	SPI_S_MISO	UART1_RX	UART1_RTS	UART1_CTS	-	UART1_TX	-
MUX_2	SIM_PRESENCE	SIM_RST	I2C0_SDA	-	-	-	I2C0_SCL	-
MUX_3	I2S_M_WS	I2S_M_SDO	PWM0_C	-	-	-	PWM0_B	PWM0_A
MUX_4	I2S_S_WS	I2S_S_SDO	PWM1_C	-	-	-	PWM1_B	PWM1_A
MUX_5	QSPI0_CLK	QSPI0_IO0	UART0_RX	UART0_RTS	UART0_CTS	-	UART0_TX	QSPI0_IO3
MUX_6	-	-	-	-	-	-	-	-
MUX_7	GPIO_24	GPIO_25	GPIO_26	GPIO_27	GPIO_28	GPIO_29	GPIO_30	GPIO_31

Table 3-5 Pin multiplexing for MSIO_0 – MSIO_4

	MSIO_0	MSIO_1	MSIO_2	MSIO_3	MSIO_4
MUX_0	PWM0_A	PWM0_B	PWM0_C	PWM1_A	PWM1_B
MUX_1	UART0_TX	UART0_RX	-	UART0_RTS	UART0_CTS
MUX_2	UART1_TX	UART1_RX	-	UART1_RTS	UART1_CTS
MUX_3	I2C0_SCL	I2C0_SDA	-	I2C0_SCL	I2C0_SDA
MUX_4	I2C1_SCL	I2C1_SDA	-	I2C1_SCL	I2C1_SDA
MUX_5	-	-	-	-	-
MUX_6	-	-	-	-	-
MUX_7	MSIO_0	MSIO_1	MSIO_2	MSIO_3	MSIO_4

Table 3-6 Pin multiplexing for AON_GPIO_0 – AON_GPIO_7

	AON_GPIO_0	AON_GPIO_1	AON_GPIO_2	AON_GPIO_3	AON_GPIO_4	AON_GPIO_5	AON_GPIO_6	AON_GPIO_7
MUX_0	-	-	SIM_PRESENCE	SIM_RST	SIM_IO	SIM_CLK	-	-
MUX_1	-	-	QSPI1_CS	QSPI1_IO0	QSPI1_IO1	QSPI1_CLK	-	-
MUX_2	-	-	I2S_M_WS	I2S_M_SDO	I2S_M_SDI	I2S_M_SCLK	-	-
MUX_3	-	-	I2S_S_WS	I2S_S_SDO	I2S_S_SDI	I2S_S_SCLK	-	-
MUX_4	-	-	-	-	-	-	-	-
MUX_5	-	QSPI0_CS	PWM0_C	PWM1_A	PWM1_B	PWM1_C	-	-
MUX_6	-	-	-	-	-	-	-	-
MUX_7	AON_GPIO_0	AON_GPIO_1	AON_GPIO_2	AON_GPIO_3	AON_GPIO_4	AON_GPIO_5	AON_GPIO_6	AON_GPIO_7

Note:

Two PWM modules (PWM0 and PWM1) are provided, with each containing three separate output channels: PWMA, PWMB, and PWMC. Frequencies of the three PWM channels in one group are the same, and individual frequency control is not supported. Phase and duty cycle of each channel can be configured via registers.

4 Package Information

GR551x offers QFN56, BGA68, BGA55, and QFN40 packages to support different environmental requirements.

4.1 QFN56

GR551x QFN56, including GR5515IGND QFN56, GR5515IENDU QFN56, and GR5515I0NDA QFN56, is a 56-pin and 7 x 7 x 0.75 (mm) QFN package. It is qualified for MSL3.

Table 4-1 QFN56 package information

Parameter	Value	Unit	Tolerance
Package Size	7 x 7	mm	±0.1 mm
QFN Pad Count	56		
Total Thickness	0.75	mm	±0.05 mm
QFN Pad Pitch	0.40		
Pad Width	0.20		
Exposed Pad Size	5.2 x 5.2		±0.1 mm

The Figure 4-1 shows the QFN56 package outlines.

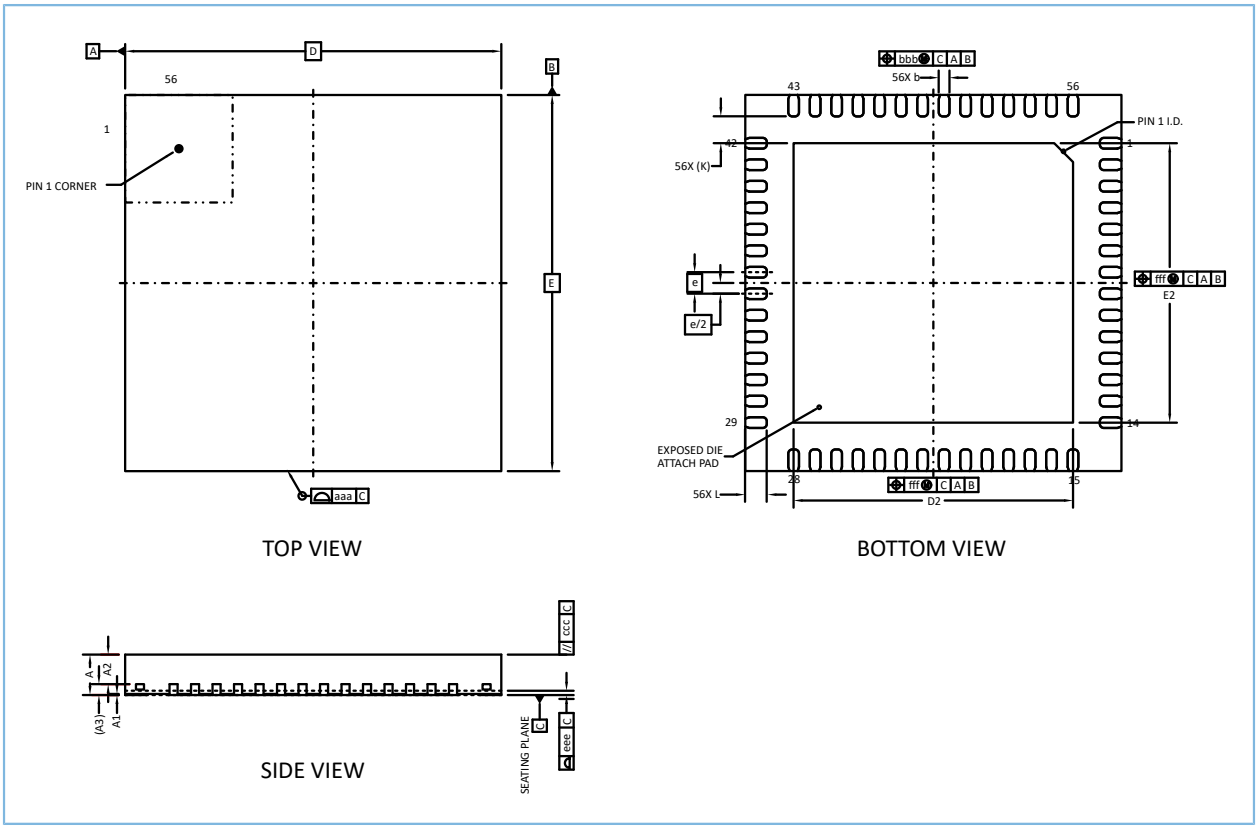

Figure 4-1 QFN56 package outlines

Note:

Drawing is not to scale.

Table 4-2 QFN56 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.550	-	-	0.022	-
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	7.000 BSC.			0.276 BSC.		
E	7.000 BSC.			0.276 BSC.		
e	0.400 BSC.			0.016 BSC.		
D2	5.100	5.200	5.300	0.201	0.205	0.209
E2	5.100	5.200	5.300	0.201	0.205	0.209
L	0.300	0.400	0.500	0.012	0.016	0.020
K	0.500 REF.			0.020 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

Refer to *JEDEC standard J-STD-020* for relevant soldering information.

4.2 BGA68

GR551x BGA68, including GR5515RGBD BGA68, is a 68-pin and 5.3 x 5.3 x 0.88 (mm) package. It is qualified for MSL3.

Table 4-3 BGA68 package information

Parameter	Value	Unit	Tolerance
Package Size	5.3 x 5.3	mm	±0.1 mm
BGA Ball Count	68		
Total Thickness	0.88	mm	±0.1 mm

Parameter	Value	Unit	Tolerance
BGA Ball Pitch	0.50		
Ball Diameter	0.25		
Ball Height	0.18		

Figure 4-2 below shows the BGA68 package outlines.

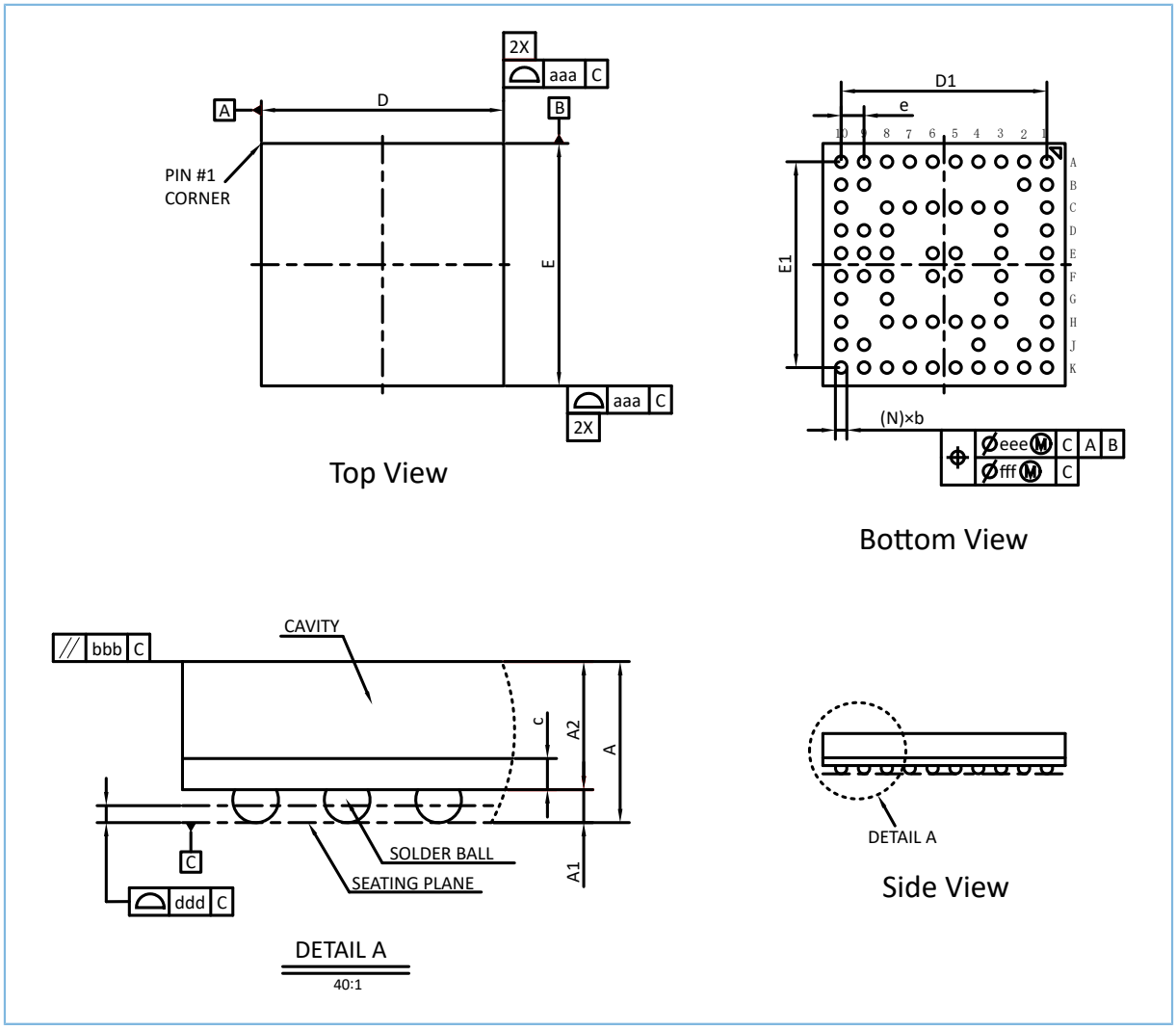

Figure 4-2 BGA68 package outlines

Note:

Drawing is not to scale.

Table 4-4 BGA68 package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.780	0.880	0.980	0.031	0.035	0.039
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.650	0.700	0.750	0.026	0.028	0.030
c	0.140	0.170	0.200	0.006	0.007	0.008
D	5.200	5.300	5.400	0.205	0.209	0.213
E	5.200	5.300	5.400	0.205	0.209	0.213
D1	--	4.500	--	--	0.177	--
E1	--	4.500	--	--	0.177	--
e	--	0.500	--	--	0.020	--
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		

Note:

Values in inches are converted from values in millimeters and rounded to 3 decimal digits.

4.3 BGA55

GR551x BGA55, including GR5515GGBD BGA55, is a 55-pin and 3.5 x 3.5 x 0.60 (mm) BGA package. It is qualified for MSL3.

Table 4-5 BGA55 package information

Parameter	Value	Unit	Tolerance
Package Size	3.5 x 3.5	mm	±0.1 mm
BGA Ball Count	55		
Total Thickness	0.60	mm	±0.05 mm
BGA Ball Pitch	0.40		
Ball Diameter	0.22		
Ball Height	0.12		±0.03 mm

The figure below shows the BGA55 package outlines.

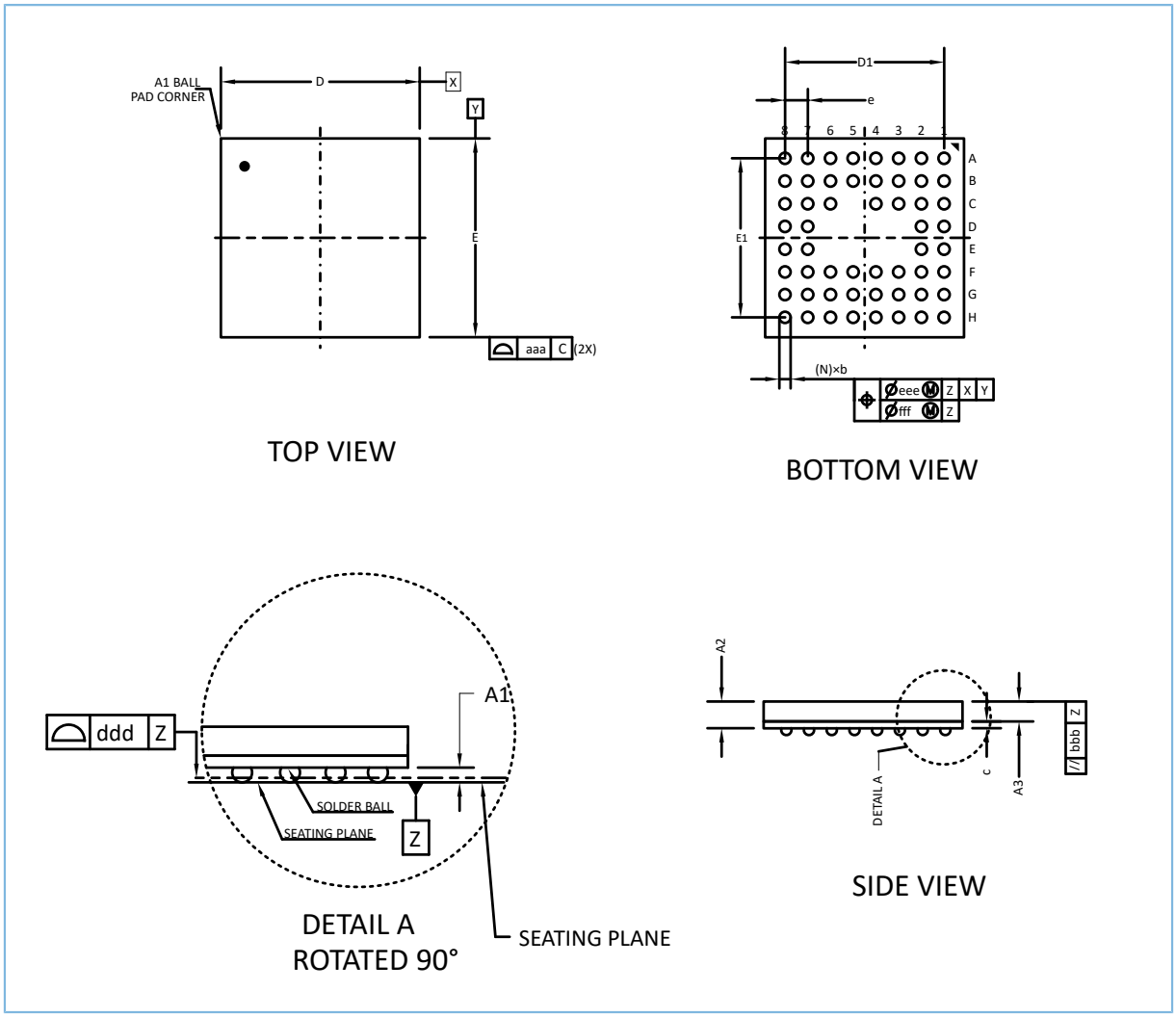

Figure 4-3 BGA55 package outlines

Note:

Drawing is not to scale.

Table 4-6 BGA55 package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.550	0.600	0.650	0.022	0.024	0.026
A1	0.090	0.120	0.150	0.004	0.005	0.006
A2	0.435	0.475	0.505	0.017	0.019	0.020
A3	0.350 REF.			0.014 REF.		
c	0.125 REF.			0.005 REF.		
D	-	3.500	-	-	0.138	-

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
E	-	3.500	-		0.138	
D1	-	2.800	-	-	0.110	-
E1	-	2.800	-	-	0.110	-
e	-	0.400	-	-	0.016	-
b	0.170	0.220	0.270	0.007	0.009	0.011
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		

Note:

Values in inches are converted from values in millimeters and rounded to 3 decimal digits.

4.4 QFN40

GR551x QFN40, including GR5513BEND QFN40 and GR5513BENDU QFN40, is a 40-pin and 5 x 5 x 0.75 (mm) package. It is qualified for MSL3.

Table 4-7 QFN40 package information

Parameter	Value	Unit	Tolerance
Package Size	5 x 5	mm	±0.1 mm
QFN Pad Count	40		
Total Thickness	0.75	mm	±0.05 mm
QFN Pad Pitch	0.40		
Pad Width	0.20		±0.05 mm
Exposed Pad Size	3.7 x 3.7		±0.1 mm

The figure below shows the QFN40 package outlines.

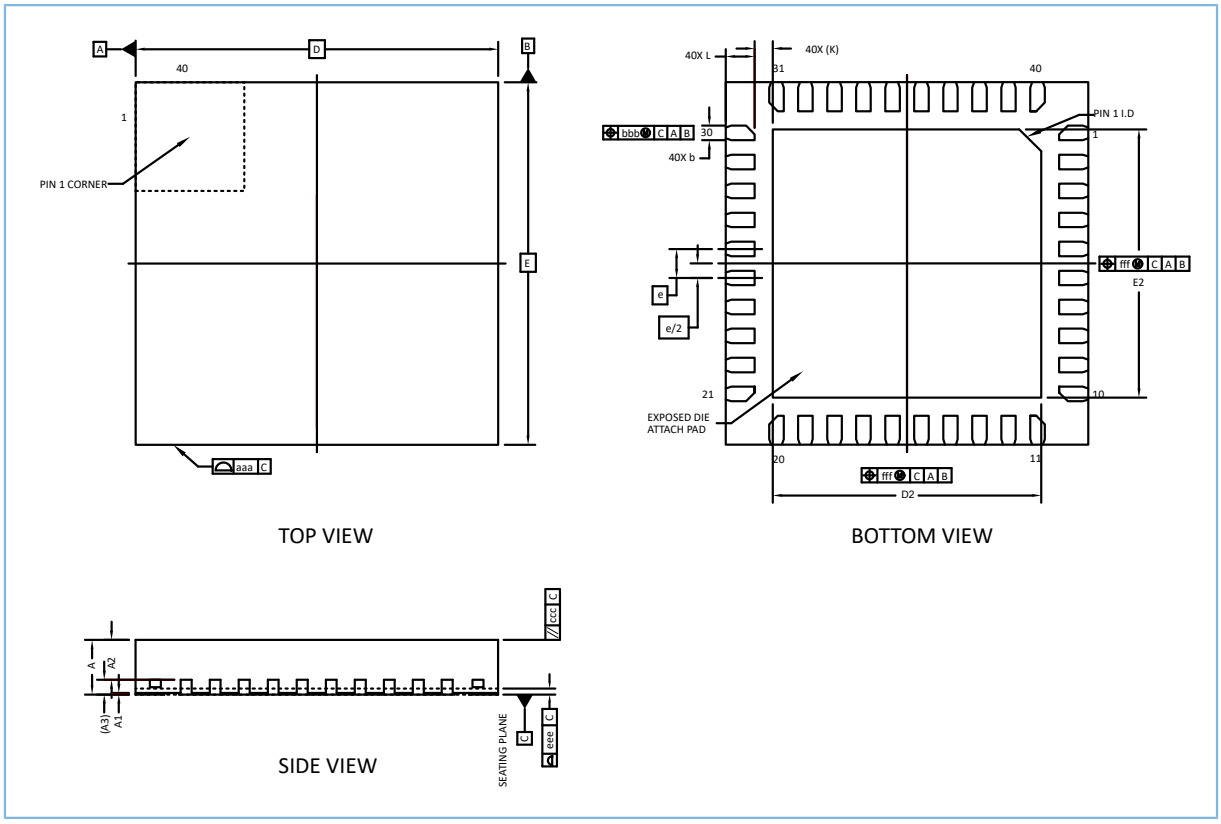

Figure 4-4 QFN40 package outlines

Note:

Drawing is not to scale.

Table 4-8 QFN40 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.550	-	-	0.022	-
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	5.000 BSC.			0.197 BSC.		
E	5.000 BSC.			0.197 BSC.		
e	0.400 BSC.			0.016 BSC.		
D2	3.600	3.700	3.800	0.142	0.146	0.150
E2	3.600	3.700	3.800	0.142	0.146	0.150
L	0.300	0.400	0.500	0.012	0.016	0.020

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
K	0.250 REF.			0.010 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.100			0.004		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

5 Glossary

Table 5-1 Glossary

Name	Description
ADC	Analog to Digital Converter
AMS	Analog Mix Signal
AON	Always-on
Bluetooth LE	Bluetooth Low Energy
LDO	Low Dropout
NRND	Not Recommended for New Designs
PMU	Power Management Unit
RNG	RING Oscillator
SoC	System-on-Chip
TPMS	Tire Pressure Monitor System
XO	Crystal Oscillator
VIO	I/O Voltage
Typ	Typical

6 Legal and Contact Information

Trademarks and Permissions

GOODiX and other Goodix trademarks are trademarks of Shenzhen Goodix Technology Co., Ltd. All other trademarks and trade names mentioned in this document are the property of their respective holders.

Disclaimer

Information contained in this document is intended for your convenience only and is subject to change without prior notice. It is your responsibility to ensure its application complies with technical specifications.

Shenzhen Goodix Technology Co., Ltd. (hereafter referred to as “Goodix”) makes no representation or guarantee for this information, express or implied, oral or written, statutory or otherwise, including but not limited to representation or guarantee for its application, quality, performance, merchantability or fitness for a particular purpose. Goodix shall assume no responsibility for this information and relevant consequences arising out of the use of such information.

Without written consent of Goodix, it is prohibited to use Goodix products as critical components in any life support system. Under the protection of Goodix intellectual property rights, no license may be transferred implicitly or by any other means.

Shenzhen Goodix Technology Co., Ltd.

Headquarters: Floor 12-13, Phase B, Tengfei Industrial Building, Futian Freetrade Zone, Shenzhen, China

TEL: +86-755-33338828 Zip Code: 518000

Website: www.goodix.com

7 Revision History

Table 7-1 Revision history

Version	Date	Description
1.5	2020-11-01	Initial release
1.6	2021-03-02	• Updated function descriptions on the TEST_MODE pin for all GR551x SoCs in “Pinout”. • Added the descriptions on I/O number for all GR551x SoCs in “GR551x Overview”. • Updated descriptions on I/O voltage of GR5515I0ND.
1.7	2021-06-15	Added a note of “not recommended for new designs” for GR5515RGBD.
1.8	2021-08-20	• Introduced GR5515IENDU and GR5515I0NDA and updated relevant chapters/sections (“GR551x Overview”, “Features”, “Pinout”, “Package Information” and "Ordering Information") accordingly. • Updated the pins name of RTC_N, RTC_P, XON, XOP to RTC_IN, RTC_OUT,XON_OUT, XO_IN in "Pinout". • Updated the description of Sleep mode in "Features". • Added "Glossary and Abbreviations".
1.9	2022-02-20	Introduced GR5513BENDU, a wide-voltage SoC.
2.0	2023-01-19	• Deleted the GR5515I0ND SoC. • Updated the GR5515RGBD status from "NRND" to "Active". • Added a note for classifying GR5513BEND as "NRND".
2.1	2023-04-20	• Updated the min value of supply voltage from 1.7 V to 2.2 V. • Updated the RX sensitivity value.