



GR533x Hardware Design Guidelines

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Preface

Purpose

This document presents the necessary circuit required for proper operation of GR533x Bluetooth System-on-Chips (SoCs). Recommended chip interfaces, peripherals, schematic diagram, and PCB layout guidelines of the GR533x SoC family are provided.

This *Hardware Design Guidelines* intends to help system designers build minimal Bluetooth Low Energy (Bluetooth LE) hardware circuits and develop Bluetooth products.

Audience

This document is intended for:

- Device user
- Developer
- Test engineer
- Technical support engineer

Release Notes

This document is the fifth release of *GR533x Hardware Design Guidelines*, corresponding to GR533x SoC series.

Revision History

Version	Date	Description
1.0	2023-10-18	Initial release
1.1	2023-11-14	Updated the power supply scheme.
1.2	2024-01-16	<ul style="list-style-type: none">• Updated layout requirements for the DC-DC switching regulator.• Added selection descriptions for the ferrite bead on the VDD_RF pin and updated the recommended bead model.
1.3	2024-06-06	<ul style="list-style-type: none">• Updated the reference design schematics.• Updated the recommended design for charger without PPM.• Updated selection of the 2.2 μH inductor.
1.4	2024-09-18	Added descriptions of GR5330 SoC.

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1 Product Overview

The Goodix GR533x series is a Bluetooth Low Energy (Bluetooth LE) 5.3 System-on-Chip (SoC), suitable for IoT applications, supporting Bluetooth mesh networking protocols.

Based on Arm[®] Cortex[®]-M4F CPU core running at 64 MHz, the GR533x integrates a 2.4 GHz RF transceiver, Bluetooth LE 5.3 protocol stack, 512 KB on-chip Flash memory, 96 KB system SRAM, and a rich set of peripherals. It provides outstanding RF performance, with a maximum TX power of +15 dBm, an RX sensitivity of -99 dBm in Bluetooth LE 1 Mbps mode, achieving an overall link budget of up to 114 dB.

With two main power supply schemes (DC-DC and system LDO), the GR533x offers flexible options to achieve a balance between low power consumption and economical BOM.

GR533x devices are offered in both QFN32 and QFN48 packages. The following table lists the detailed package configurations.

Table 1-1 GR533x series

Part Number	GR5330AENI	GR5331AENI	GR5331CENI	GR5332AENE	GR5332CENE
CPU	Cortex [®] -M4F				
RAM	64 KB	96 KB	96 KB	96 KB	96 KB
SiP Flash	512 KB				
TX power	Up to 6 dBm	Up to 6 dBm	Up to 6 dBm	Up to 15 dBm	Up to 15 dBm
RX sensitivity	-97.5 dBm @ 1 Mbps	-97.5 dBm @ 1 Mbps	-97.5 dBm @ 1 Mbps	-99 dBm @ 1 Mbps	-99 dBm @ 1 Mbps
Consumption	3.8 mA TX @ 0 dBm	3.8 mA TX @ 0 dBm	3.8 mA TX @ 0 dBm	5.9 mA TX @ 0 dBm	5.9 mA TX @ 0 dBm
	4.7 mA RX @ 1 Mbps	4.7 mA RX @ 1 Mbps	4.7 mA RX @ 1 Mbps	4.9 mA RX @ 1 Mbps	4.9 mA RX @ 1 Mbps
I/O number	16	16	32	16	32
Operating temperature	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 105°C	-40°C to 105°C
Package (mm)	QFN32 (4 x 4 x 0.75)	QFN32 (4 x 4 x 0.75)	QFN48 (6 x 6 x 0.75)	QFN32 (4 x 4 x 0.75)	QFN48 (6 x 6 x 0.75)

1.1 Features

- Bluetooth LE 5.3 transceiver
 - Supported data rates: 1 Mbps, 2 Mbps, and Long Range (500 kbps, 125 kbps)
 - TX power:
 - Up to 6 dBm on GR5330/GR5331
 - Up to 15 dBm on GR5332
 - RX sensitivity:
 - -97.5 dBm @ 1 Mbps on GR5330/GR5331
 - -99 dBm @ 1 Mbps on GR5332

- Power consumption at 3.3 V VBAT input on GR5330/GR5331:
 - 3.8 mA TX current @ 0 dBm output power (DC-DC supply, 16 MHz system clock)
 - 4.7 mA RX current @ 1 Mbps (DC-DC supply, 16 MHz system clock)
- Power consumption at 3.3 V VBAT input on GR5332:
 - 5.9 mA TX current @ 0 dBm output power (DC-DC supply, 16 MHz system clock)
 - 86.3 mA TX current @ 15 dBm output power (SYS_LDO supply, 64 MHz system clock)
 - 4.9 mA RX current @ 1 Mbps (DC-DC supply, 16 MHz system clock)
- Arm® Cortex® -M4F 32-bit micro-processor with floating point support:
 - Up to 64 MHz clock frequency
 - Built-in Memory Protection Unit (MPU) supporting eight programmable regions
 - Hardware Floating Point Unit (FPU)
 - Built-in Nested Vectored Interrupt Controller (NVIC)
 - Non-maskable Interrupt (NMI) input
 - Serial Wire Debug (SWD) with 16 breakpoints, two watchpoints, and a debug timestamp counter
 - 32 µA/MHz CoreMark running from Flash @ 3.3 V, 64 MHz from HFRC
- On-chip memory
 - ROM for chip bootloader, system drivers, and Bluetooth LE Protocol Stack code
 - RAM for data and instruction code, with retention capabilities in sleep mode. GR5330: 64 KB; GR5331/GR5332: 96 KB
 - 512 KB Flash for code, system parameter configuration, and user data
- Digital peripherals
 - 1 x general-purpose DMA engine with five channels and 16 handshaking interfaces
- Analog peripherals
 - 1 x 13-bit Sense ADC with a sampling rate of 1 Msps, supporting up to eight external I/O channels and three internal signal channels
 - Built-in die temperature and voltage sensors
 - Low-power comparator, supporting wakeup from sleep mode
- Flexible serial peripherals with arbitrary mapping on all digital I/Os
 - 2 x UART modules up to 2 Mbps with flow control and IrDA features
 - 2 x I2C modules for peripheral communication, up to 1 MHz, operating as either Master or Slave
 - 1 x 8-bit/16-bit/32-bit SPI master interface and 1 x SPI slave interface for host communication

- Security
 - AES 128-bit security module (ECB, CBC)
 - True random number generator (TRNG)
- I/O peripherals
 - Up to 32 multiplexed I/O pins in total
 - Up to 14 general-purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors
 - Up to eight always-on I/O (AON I/O) pins, supporting wakeup from sleep mode
 - Up to 10 mixed signal I/O (MSIO) pins, configurable to be digital/analog signal interfaces
- Timers
 - 2 x 32-bit general-purpose timers
 - 1 x dual timer with two programmable 32-bit or 16-bit down counters
 - 1 x sleep timer for waking the device up from sleep mode
 - 2 x 3-channel PWMs with edge-aligned mode and center-aligned mode
 - 1 x real-time counter
- Power management
 - On-chip DC-DC/SYS_LDO to provide RF analog voltage and supply CORE_LDO
 - On-chip I/O LDO to provide I/O voltage and supply external components
 - Programmable thresholds for brownout detector (BOD)
 - Supply voltage: 2.0 V–3.63 V
 - I/O voltage: 1.8 V–3.6 V
- Low-power consumption
 - Sleep mode: 2.6 μ A (Typical) at 3.3 V VBAT input, with 48 KB SRAM retention on, wakeup sources from AON I/Os, and LFXO_32K running
 - Ultra deep sleep mode: 2.2 μ A (Typical), with no memory data in retention and wakeup sources from SLP Timer or AON I/Os
 - OFF mode: 200 nA (Typical), with system in reset mode
- Operating temperature range
 - GR5330/GR5331: -40°C to 85°C
 - GR5332: -40°C to 105°C
- Packages
 - QFN32: 4.0 x 4.0 x 0.75 mm, 0.4 mm pitch

- QFN48: 6.0 x 6.0 x 0.75 mm, 0.4 mm pitch

1.2 Block Diagram

The SoC block diagram is shown in the figure below.

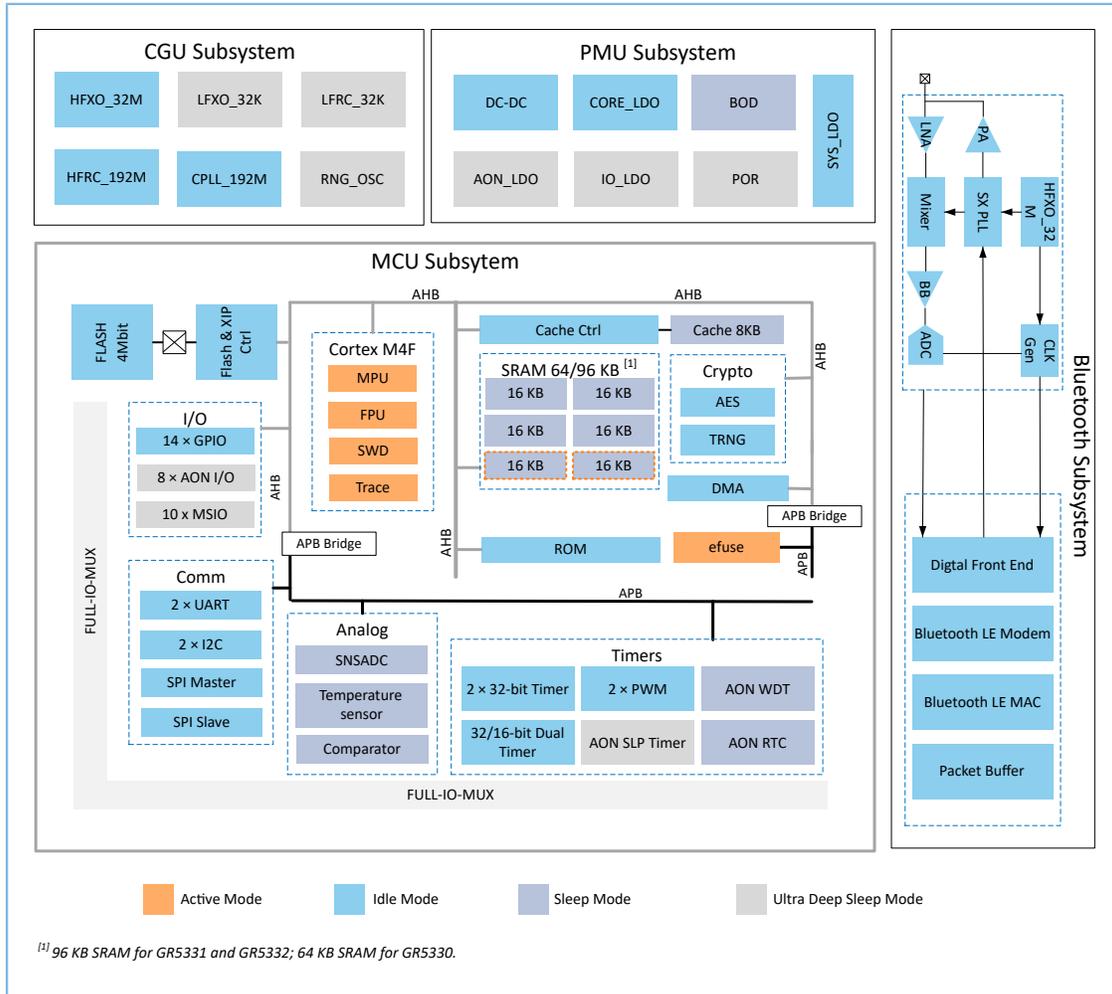


Figure 1-1 Block diagram

- Bluetooth subsystem
 - A 2.4 GHz transceiver and a digital communication core, both supporting Bluetooth LE 5.3
- MCU subsystem
 - An Arm® Cortex® -M4F with all the required memories and peripherals
- Power Management Unit (PMU) subsystem
 - Power supply for the whole SoC, including internal modules and external peripherals
 - Efficient and reliable SoC power management
- Clock Generation Unit (CGU) subsystem

- Providing stable, low-power, and accurate clock signals
- Optimizing SoC performance and minimizing power consumption, by adjusting clock frequency and selecting an appropriate clock.

1.3 Applications

The device can be used in a rich set of applications.

- IoT applications
 - Smart lock and smart home
 - Beacon and smart tracker
 - Electronic shelf label (ESL)
 - Mesh applications
 - Asset tracking
- Health and medical applications
 - Thermometer
 - SpO2 meter
 - Blood glucose and pressure meter
 - Weight scale
- Bluetooth HID devices
 - Remote control
 - Gaming controller
 - Stylus pen

2 Pinout

This chapter describes the pin assignment of the device and provides detailed information for each individual pin.

2.1 QFN32

The figure below shows the pin assignment for devices in QFN32 package.

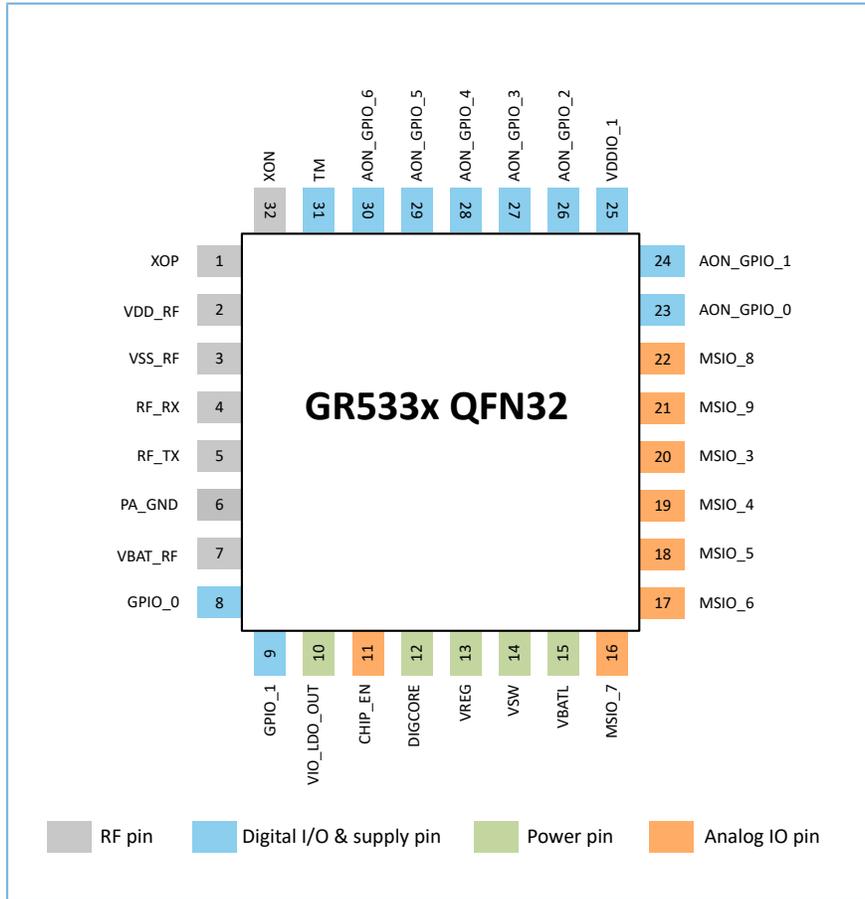


Figure 2-1 QFN32 device pinout (top view)

The following table provides the descriptions of pin functionality.

Table 2-1 Pin functions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	XOP	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
2	VDD_RF	Analog/RF supply	Input of RF supply; connect to VREG.	
3	VSS_RF	Analog/RF supply	RF GND; connect to GND.	
4	RF_RX	Analog/RF	RF transceiver RX input	
5	RF_TX	Analog/RF	RF transceiver TX output	
6	PA_GND	Analog/RF Supply	RF PA GND; connect to ground.	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
7	VBAT_RF	Analog/RF Supply	RF HPA and Bandgap supply; connect to VBATL.	
8	GPIO_0	Digital I/O	General-purpose I/O; default: SWD_CLK	VDDIO0
9	GPIO_1	Digital I/O	General-purpose I/O; default: SWD_IO	
10	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator; connect internally to VDDIO0. Typical output voltage: 1.8 V.	
11	CHIP_EN	Analog/PMU	Master Enable for chip reset pin Minimum value of high level for CHIP_EN: 1 V	
12	DIGCORE	Analog/PMU	On-chip LDO output for digital core	
13	VREG	Analog/PMU	DC-DC feedback pin of switch regulator/SYS_LDO output pin	
14	VSW	Analog/PMU	DC-DC converter switching node	
15	VBATL	Analog/PMU	Power supply: 2.0 V to 3.63 V	
16	MSIO_7	PMU/Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO and SNSADC Multiplexed by writing eFuse using external 2.5 V voltage.	VBATL
17	MSIO_6	Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO and SNSADC	
18	MSIO_5	Mixed Signal I/O		
19	MSIO_4	Mixed Signal I/O		
20	MSIO_3	Mixed Signal I/O		
21	MSIO_9	Mixed Signal I/O		Configurable mixed-signal I/O with digital GPIO Multiplexed as RTC_32K_OUT.
22	MSIO_8	Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO Multiplexed as RTC_32K_IN.	VDDIO1
23	AON_GPIO_0	Digital I/O	Always-on GPIO, can wake up chip from sleep modes	
24	AON_GPIO_1	Digital I/O		
25	VDDIO_1	Digital I/O supply	Digital I/O supply input. Support external 1.8 V–3.6 V input voltage.	
26	AON_GPIO_2	Digital I/O	Always-on GPIO, can wake up chip from sleep modes	
27	AON_GPIO_3	Digital I/O		
28	AON_GPIO_4	Digital I/O		
29	AON_GPIO_5	Digital I/O		
30	AON_GPIO_6	Digital I/O		
31	TM	Analog/RF		Input pin, used for factory test mode selection <ul style="list-style-type: none"> 1: factory test mode 0: normal operation mode

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
			Note: In practice, the value is set to 0 by default; connect to GND.	
32	XON	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	

Note:

The pad drive strength for all I/Os (including GPIOs/ AON_GPIOs/ MSIOs) can be configured to 2 mA/4 mA/8 mA/12 mA under 3.3 V voltage.

2.2 QFN48

The figure below shows the pin assignment for devices in QFN48 package.

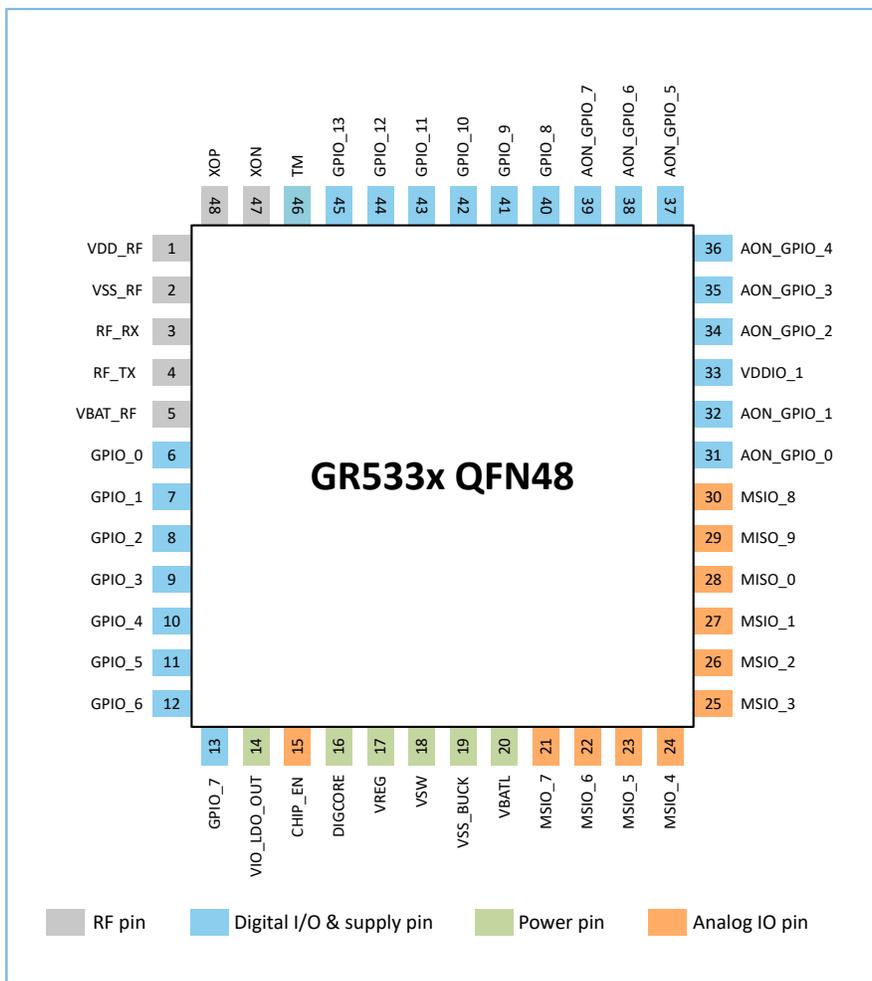


Figure 2-2 QFN48 device pinout (top view)

The following table provides the descriptions of pin functionality.

Table 2-2 Pin functions

Pin #	Pin Name	Pin Type	Description / Default Function	Voltage Domain
1	VDD_RF	Analog/RF supply	Input of synthesizer RF supply; connect to VREG.	
2	VSS_RF	Analog/RF supply	RF GND; connect to GND.	
3	RF_RX	Analog/RF	RF transceiver RX input	
4	RF_TX	Analog/RF	RF transceiver TX output	
5	VBAT_RF	Analog/RF Supply	RF HPA and Bandgap supply; connect to VBATL.	
6	GPIO_0	Digital I/O	General-purpose I/O; default: SWD_CLK	VDDIO0
7	GPIO_1	Digital I/O	General-purpose I/O; default: SWD_IO	
8	GPIO_2	Digital I/O	General-purpose I/O	
9	GPIO_3	Digital I/O		
10	GPIO_4	Digital I/O		
11	GPIO_5	Digital I/O		
12	GPIO_6	Digital I/O		
13	GPIO_7	Digital I/O		
14	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator; connect internally to VDDIO0. Typical output voltage: 1.8 V.	
15	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin Minimum value of high level for CHIP_EN: 1 V	
16	DIGCORE	Analog/PMU	On-chip LDO output for digital core	
17	VREG	Analog/PMU	DC-DC feedback pin of switch regulator/SYS_LDO output pin	
18	VSW	Analog/PMU	DC-DC converter switching node	
19	VSS_BUCK	PMU	DC-DC converter Power GND	
20	VBATL	PMU	Power supply: 2.0 V to 3.63 V	
21	MSIO_7	PMU/Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO and SNSADC Multiplexed by writing eFuse using external 2.5 V voltage	VBATL
22	MSIO_6	Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO and SNSADC	
23	MSIO_5	Mixed Signal I/O		
24	MSIO_4	Mixed Signal I/O		
25	MSIO_3	Mixed Signal I/O		
26	MSIO_2	Mixed Signal I/O		
27	MSIO_1	Mixed Signal I/O		
28	MSIO_0	Mixed Signal I/O		

Pin #	Pin Name	Pin Type	Description / Default Function	Voltage Domain
29	MSIO_9	Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO Multiplexed as RTC_32K_OUT.	VDDIO1
30	MSIO_8	Mixed Signal I/O	Configurable mixed-signal I/O with digital GPIO Multiplexed as RTC_32K_IN.	
31	AON_GPIO_0	Digital I/O	Always-on GPIO, can wake up chip from sleep modes.	
32	AON_GPIO_1	Digital I/O		
33	VDDIO_1	Digital I/O supply	Digital I/O supply input Support external 1.8 V–3.6 V input voltage.	
34	AON_GPIO_2	Digital I/O	Always-on GPIO, can wake up chip from sleep modes.	
35	AON_GPIO_3	Digital I/O		
36	AON_GPIO_4	Digital I/O		
37	AON_GPIO_5	Digital I/O		
38	AON_GPIO_6	Digital I/O		
39	AON_GPIO_7	Digital I/O		
40	GPIO_8	Digital I/O	General-purpose I/O	
41	GPIO_9	Digital I/O		
42	GPIO_10	Digital I/O		
43	GPIO_11	Digital I/O		
44	GPIO_12	Digital I/O		
45	GPIO_13	Digital I/O		
46	TM	Analog/RF	Input pin, used for factory test mode selection <ul style="list-style-type: none"> 1: factory test mode 0: normal operation mode Note: In practice, the value is set to 0 by default; connect to GND	
47	XON	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
48	XOP	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

Note:

The pad drive strength for all I/Os (including GPIOs/ AON_GPIOs/ MSIOs) can be configured to 2 mA/4 mA/8 mA/12 mA under 3.3 V voltage.

2.3 Pin Properties

2.3.1 PMU Pin Properties

Table 2-3 PMU pin properties

No.	Pin Name	Input/Output/GND	Min.	Typ.	Max.	Unit
1	VDD_RF	Input	1.0	1.05	1.21	V
2	VSS_RF	GND	-	0	-	V
3	VBAT_RF	Input	2.0	3.3	3.63	V
4	VIO_LDO_OUT	Output	1.7	1.8	3.63	V
5	CHIP_EN	Input	0	-	3.63	V
6	DIGCORE	Output	0.85	0.9	1.1	V
7	VREG	Output	0.95	1.05	1.21	V
8	VSW	Output	-	-	-	V
9	VSS_BUCK	GND	-	0	-	V
10	VBATL	Input	2.0	3.3	3.63	V
11	VDDIO_1	Input	1.7	1.8	3.63	V
12	TM	Input	-	0	-	V

2.3.2 I/O Pin Properties

Table 2-4 I/O pin properties

No.	Pin Name	Default Status After POR	Pull-up/Pull-down Enable After POR	Pull-up/Pull-down Selection After POR	Pin Interrupt	Chip Wake-up	Fast Capability
1	GPIO_0	L	Y	PD	Y	N	Y
2	GPIO_1	L	Y	PD	Y	N	Y
3	GPIO_2	L	Y	PD	Y	N	Y
4	GPIO_3	L	Y	PD	Y	N	Y
5	GPIO_4	L	Y	PD	Y	N	Y
6	GPIO_5	L	Y	PD	Y	N	Y
7	GPIO_6	L	Y	PD	Y	N	Y
8	GPIO_7	L	Y	PD	Y	N	Y
9	MSIO_7	Hi-Z	N	-	N	N	Y
10	MSIO_6	Hi-Z	N	-	N	N	Y
11	MSIO_5	Hi-Z	N	-	N	N	Y
12	MSIO_4	Hi-Z	N	-	N	N	Y
13	MSIO_3	Hi-Z	N	-	N	N	Y
14	MSIO_2	Hi-Z	N	-	N	N	Y

No.	Pin Name	Default Status After POR	Pull-up/Pull-down Enable After POR	Pull-up/Pull-down Selection After POR	Pin Interrupt	Chip Wake-up	Fast Capability
15	MSIO_1	Hi-Z	N	-	N	N	Y
16	MSIO_0	Hi-Z	N	-	N	N	Y
17	MSIO_9	Hi-Z	N	-	N	N	Y
18	MSIO_8	Hi-Z	N	-	N	N	Y
19	AON_GPIO_0	L	Y	PD	Y	Y	Y
20	AON_GPIO_1	L	Y	PD	Y	Y	Y
21	AON_GPIO_2	L	Y	PD	Y	Y	Y
22	AON_GPIO_3	L	Y	PD	Y	Y	Y
23	AON_GPIO_4	L	Y	PD	Y	Y	Y
24	AON_GPIO_5	L	Y	PD	Y	Y	Y
25	AON_GPIO_6	L	Y	PD	Y	Y	Y
26	AON_GPIO_7	L	Y	PD	Y	Y	Y
27	GPIO_8	L	Y	PD	Y	N	Y
28	GPIO_9	L	Y	PD	Y	N	Y
29	GPIO_10	L	Y	PD	Y	N	Y
30	GPIO_11	L	Y	PD	Y	N	Y
31	GPIO_12	L	Y	PD	Y	N	Y
32	GPIO_13	L	Y	PD	Y	N	Y

Abbreviations mentioned above are listed in the table below:

Table 2-5 Abbreviations related to pin properties

Properties	Abbreviation	Description
Default status after POR	Hi-Z	High impedance
	H	High level
	L	Low level
Pull-up/Pull-down enable after POR	Y	Enabled
	N	Disabled
Pull-up/Pull-down selection after POR	PU	Pull-up
	PD	Pull-down
Pin interrupt	N	No
	Y	Yes
Fast capability	N	Fast capability is not supported.

Properties	Abbreviation	Description
	Y	Fast capability is supported.

3 Minimal Design for GR533x SoC

The absolute necessary sections required for the GR533x SoC minimal system operation include

- Power supply
- Clock
- RF
- I/O pins
- SWD interfaces

To ensure the proper operation of a GR533x SoC, the design guidelines for the schematic diagram and the PCB layout are illustrated in the following sections.

3.1 Schematic Design Guideline

For the minimal schematic for a GR533x SoC, see [“Section 3.4 Reference Design”](#).

3.1.1 Power Supply

3.1.1.1 Introduction

GR533x SoCs are powered by external power sources through VBATL (voltage range: 2.0 V to 3.63 V).

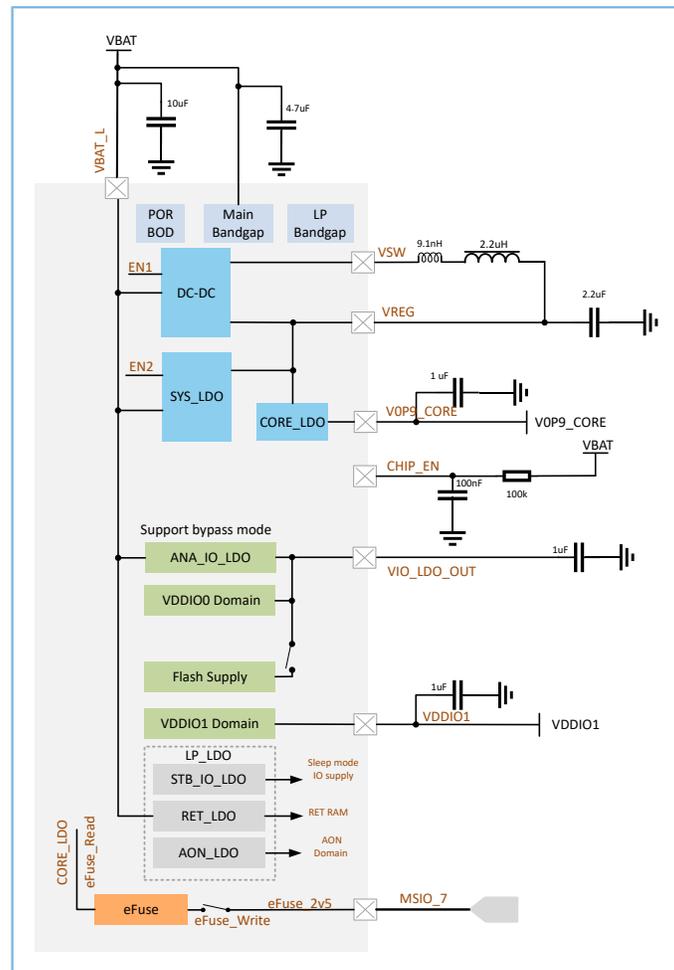


Figure 3-1 Power architecture

As shown in [Figure 3-1](#), the GR533x power supply architecture is based on the PMU that generates the following supplies from an external supply through VBATL.

- DC-DC/SYS_LDO: supply for RF domain and core LDO (Enabled by default).
- CORE_LDO: supply for digital logic blocks (Enabled by default).
- AON_LDO: supply for AON blocks (Enabled by default).
- RET_LDO: retention supply for memory instances (Enabled by default).
- ANA_IO_LDO: Used to generate the I/O voltage to supply the pads of GR533x and the external devices connecting to GR533x. It is also used to supply power to the stacked Flash (Enabled by default).
- STB_IO_LDO: Used to replace ANA_IO_LDO during sleep, which can help reduce sleep current.
- VDDIO1: supply for I/O1 group; from external power voltage or VIO_LDO_OUT.
- MSIO_7: input 2.5 V external voltage to burn eFuse. By burning the eFuse configuration, you can disable the SWD debugging function that is multiplexed by GPIO_0/GPIO_1.

Both VBATL and VBAT_RF come from the battery voltage VBAT. The VBAT_RF voltage is supplied to the RF domain alone, and the VBATL voltage is the input voltage of all blocks.

Tip:

- To avoid the switch overshoot caused by battery welding, connect a resistor ($0.39\ \Omega - 1\ \Omega$) between the battery and VBATL in series when powering on a GR533x SoC.
- It is recommended to convert the battery voltage to 3.3 V with LDO before supplying VBATL.

3.1.1.2 Power-on Sequence

The figure below shows the power-on sequence for GR533x.

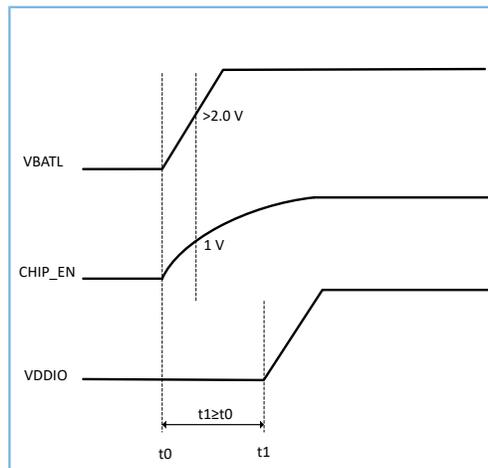


Figure 3-2 Power-on sequence

Note:

- After power-on, when CHIP_EN reaches 1 V, VBATL shall be above 2 V.
- Do not power on VDDIO before VBATL.
- When GR533x works as Slave, VBATL cannot be powered on after CHIP_EN is pulled low. Otherwise, the I/O state might be out of control and forced to output high level.

In GR533x applications where devices are supplied by rechargeable batteries but the charger does not support power path management (PPM), when the battery is recharged after its voltage decreases to 0 V (battery depletion due to self-discharge in long-term shipping or storage), the system will fail to be started because it fails to follow the power-on sequence. To avoid this problem, it is recommended to follow the charger solutions below:

- Using a charger with PPM
To use a charger that supports system power path management, follow the recommended circuit design in [Figure 3-3](#).

- The battery charging path and the system power supply path can be managed independently: When battery voltage drops to 0 V, connect the charger with an external power source from the USB port. After the input power going through Qbypass and Qrvs, the voltage V_{SYS} supplies the system, and the Vbat controlled by Qswitch supplies the 0 V battery.
- When charging starts, V_{SYS} will instantly rise to the pre-set value, and GR533x VBATL will also instantly reach the operating voltage or above. The system can keep working normally in this case, thanks to the delay circuit on CHIP_EN that helps ensure GR533x power-on sequence.

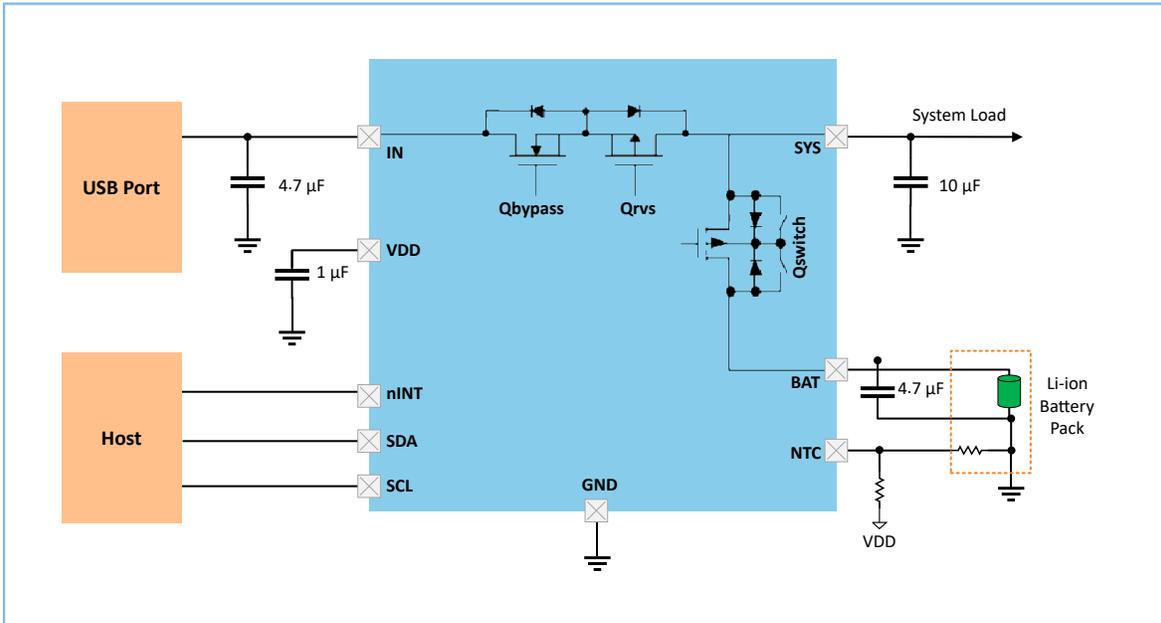


Figure 3-3 Reference design for charger with PPM

- Using a charger without PPM

To use a charger that does not support PPM, you can add an external circuit for power path management, as shown below.

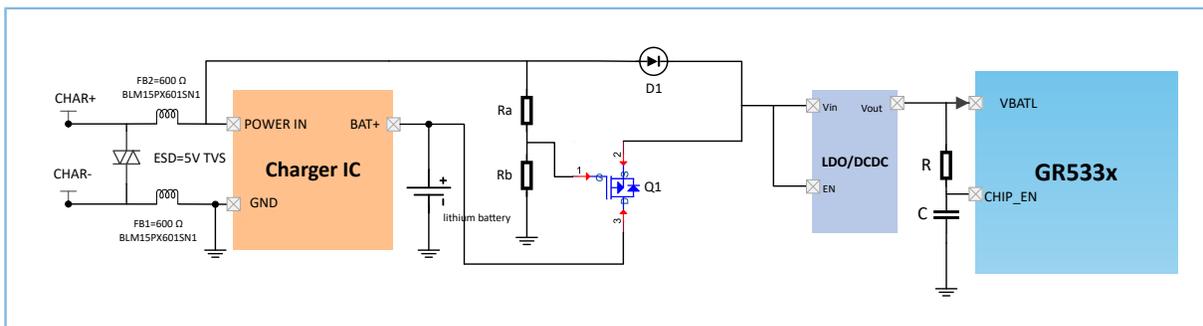


Figure 3-4 Reference design for charger not supporting PPM

- Power supply path in uncharged state

In uncharged state, the battery conducts through the body diode of the PMOS transistor (Q1) to the LDO input (Vin pin), providing a high voltage to the source voltage (V_s) of Q1. By setting the gate voltage (V_g)

of Q1 to 0 V with the pull-down of resistor Rb, Q1 is fully turned on, enabling the battery to power the subsequent system (such as the LDO). Additionally, a diode (D1) is used for reverse protection to prevent leakage current.

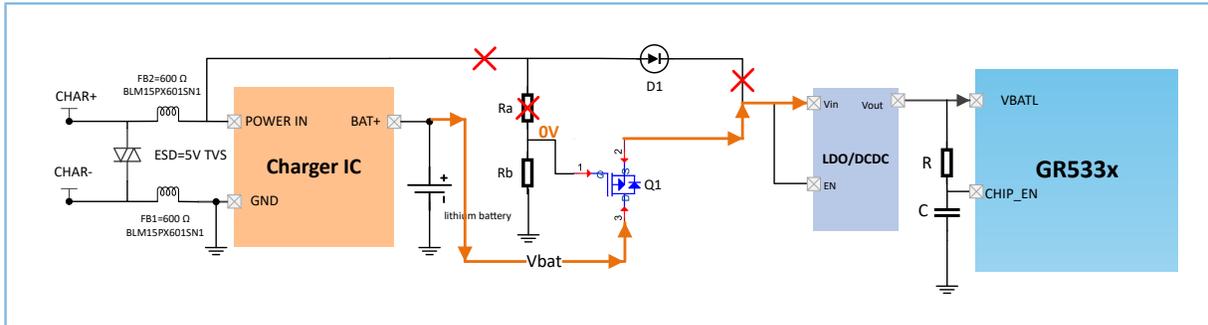


Figure 3-5 Power supply path in uncharged state

Power supply path in charging state or fully charged state

In charging state, the 5 V USB power source is stepped down through the diode D1 (assuming a voltage drop of 0.7 V) and outputs 4.3 V to power the system LDO. The gate voltage (Vg) of Q1 is divided by resistors Ra and Rb (typical values: Ra = 4.7 kΩ, Rb = 47 kΩ) to 4.54 V; the source voltage (Vs) of Q1 is 4.3 V. In this case, the voltage difference (Vgs) between the gate and source of Q1 is 0.24 V, Q1 is in off state, and the battery is in charging state and will not discharge.

In fully charged state, the voltage difference (Vsd) between the source and drain of Q1 is 0.1 V, and the internal body diode cannot conduct, so Q1 remains in off state, preventing the battery from supplying the system. In this case, the system is supplied by the external USB power source.

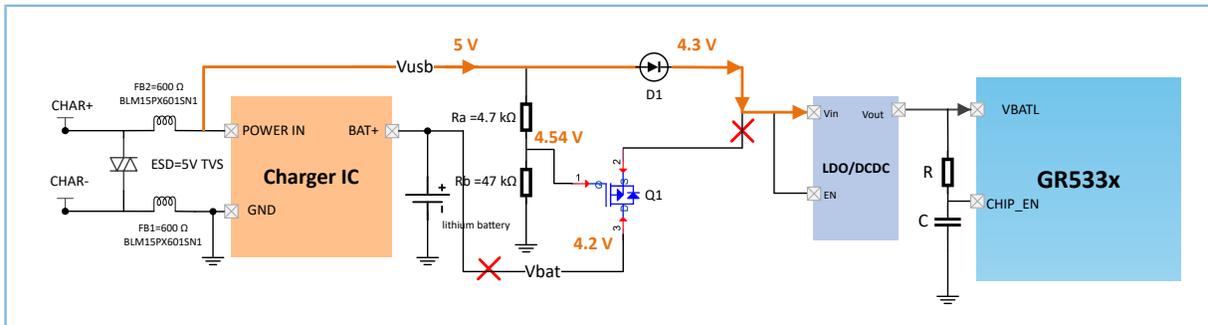


Figure 3-6 Power supply path in charging state or fully charged state

The reference formulas for voltage calculation are as follows:

$$V_g = V_{usb} * R_b / (R_a + R_b) = 4.54 \text{ V}$$

$$V_s = V_{usb} - V_{diode} = 4.3 \text{ V}$$

$$V_d = V_{bat} = 4.2 \text{ V (Max.)}$$

$$V_{gs} = V_g - V_s = 0.24 \text{ V}$$

$$V_{sd} \text{ (Min.)} = V_s - V_d \text{ (Max.)} = 0.1 \text{ V}$$

Recommended PMOS transistors and diodes are detailed as follows:

Table 3-1 Recommended PMOS transistor (Q1)

Part Number	Vgs(th)	Id	Rds(on) @Vgs = -2.5 V	Footprint Reference	Manufacturer
CJBB3139K	> -0.35 V (typical)	-0.66 μ A	780 m Ω	DFN1006-3L-A	JSET
NTK3139P	> -0.45 V (typical)	-1 μ A	520 m Ω	SOT-723	ON Semiconductor

Table 3-2 Recommended diode (D1)

Part Number	Vf	Ir	Footprint Reference	Manufacturer
1N4148WT	0.715 V (typical)	1 μ A @Vr =75 v	SOD-523	DIODES
BAS716	0.77 V (typical)	5 nA @Vr =75 v	SOT-523	NXP

 **Tip:**

- Choose a diode with an appropriate voltage drop according to the requirements on system power supply.
- Resistances of Ra and Rb can be set according to the parameters of Q1.
- The current carrying capacity of the USB charging adapter should be greater than the sum of the system current and the charging current.

3.1.1.3 I/O LDO

The GR533x has an on-chip linear LDO regulator that supplies always-on blocks, including always-on I/Os and digital logic blocks. Additionally, this regulator can supply external components (sensors) which interface to the GR533x. The LDO is capable of supplying up to 30 mA load current.

The output of this regulator is the VIO_LDO_OUT pin. A 1 μ F decoupling capacitor should be connected to this pin. Three I/O voltage domains are provided for GR533x: two digital voltage domains (VDDIO_0 and VDDIO_1), as well as one mixed signal I/O domain MSIO, corresponding to reference voltage levels at VDDIO_0, VDDIO_1, and VBATL respectively.

[Figure 3-7](#) is a circuit diagram showing the connection between VIO_LDO_OUT and the I/O domains.

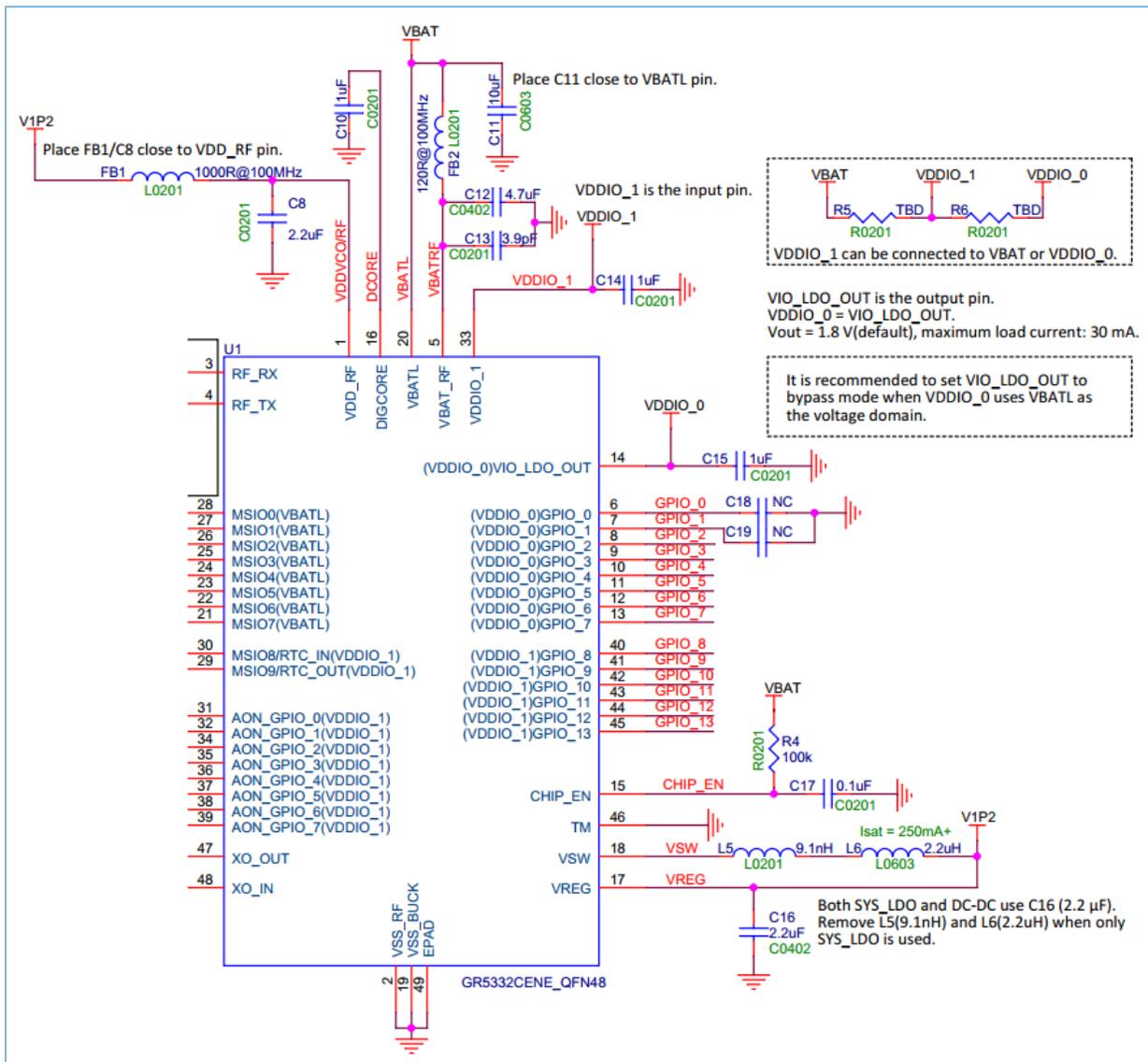


Figure 3-8 Power section

The detailed pin descriptions and connection guidance are as follows:

- **VDD_RF**: internal RF block supply, connected to V1P2 (output power net of DC-DC switching regulator) and a 2.2 μF decoupling capacitor.
- **DIGCORE**: output of digital LDO, which supplies the digital core logic. Connect a 1 μF decoupling capacitor to this pin.
- **VBATL**: input supply for chip – ranging from 2.0 V to 3.63 V; connected to a 10 μF decoupling capacitor; the ripple noise of the power supply does not exceed 40 mV.
- **VBAT_RF**: connected to VBATL, as well as a 4.7 μF decoupling capacitor. Connect a 3.9 pF capacitor in parallel to filter out high-order harmonics. The capacitance of the pF capacitor can be adjusted to meet specific requirements for suppressing harmonics. The material selection is based on ensuring the minimum impedance at the positions where harmonic suppression is needed.

- **VIO_LDO_OUT:** connected to VDDIO0 internally by default, output of the on-chip VDDIO LDO regulator, used to supply the on-chip Flash. It can also supply the VDDIO pins and external sensors with load current up to 30 mA. Connected to a 1 μ F decoupling capacitor.
- **VSW:** DC-DC switching regulator output, connected to two inductors in series: a 9.1 nH inductor for reducing RF interference caused by switching noise and a 2.2 μ H power inductor, as well as a 2.2 μ F capacitor, to supply the SoC from V1P2 as a complete DC-DC circuit. The pin is also connected to VDD_RF through external circuits.
- **VREG:** feedback pin from the DC-DC switching regulator output (mux with SYS_LDO output), connected to V1P2.
- **VDDIO_1:** Provide power for I/O1 voltage domain; supplied from VIO_LDO_OUT or an external power source; connected to a 1 μ F decoupling capacitor.

 **Tip:**

- External input voltage to the VIO_LDO_OUT pin is prohibited. For example, it is strictly forbidden to directly connect VBATL to the VIO_LDO_OUT pin in the external circuit of the SoC. If the CHIPEN pin is pulled low and an external power supply is connected to this pin, it may cause leakage current.
- When the VIO_LDO_OUT output voltage is the same as the VBATL voltage, it is recommended to set VIO_LDO_OUT to bypass mode by configuring the eFuse.

Recommended capacitors, ferrite beads, and inductors are listed in [Table 3-3](#), [Table 3-4](#), and [Table 3-5](#).

Table 3-3 Recommended decoupling capacitors and ferrite beads for the power section

Reference	Description	Value	Package	Mfg Part #
C8	CAP, CER, 2.2 μ F, 10%, X5R, 0201, 6.3 V, -55°C to +85°C	2.2 μ F	0201	Murata GRM033R60J225ME01
C16	CAP, CER, 2.2 μ F, 10%, X6S, 0402, 10 V, -55°C to +105°C	2.2 μ F	0402	Murata GRM155C81A225KE11
C10, C14, C15	CAP, CER, 1 μ F, 20%, X6S, 0201, 10 V, -55°C to +105°C	1 μ F	0201	Murata GRM033C81A105ME05
C11	CAP, CER, 10 μ F, 20%, X6S, 0603, 10 V, -55°C to +105°C	10 μ F	0603	Murata GRM188C81A106MA73
C12	CAP, CER, 4.7 μ F, 20%, X6S, 0402, 10 V, -55°C to +105°C	4.7 μ F	0402	Murata GRM155C81A475ME01
C13	CAP, CER, 3.9 pF, +/-0.1 pF, NPO, 0201, 50 V, -55°C to +125°C	3.9 pF	0201	Murata GJM0335C1H3R9BB01
C17	CAP, CER, 0.1 μ F, 20%, X6S, 0201, 10 V, -55°C to +105°C	0.1 μ F	0201	Murata GRM033C81C104ME14
FB1	Ferrite bead, 1000 ohm @ 100 MHz, 200 mA, 1.25 mohm	1000 Ω @ 100 MHz	0201	Murata BLM03AX102SN1

Reference	Description	Value	Package	Mfg Part #
FB2	Ferrite bead, 120 ohm @ 100 MHz, 200 mA, 500 mohm	120 Ω @ 100 MHz	0201	Murata BLM03AG121SN1

 **Note:**

In cases where layout constraints lead to an abnormal increase in the ripple voltage of the DC-DC switching regulator, changing the material of the VDD_RF filter bead (FB1) can help minimize the ripple impact on RF characteristics. It is recommended to select a ferrite bead rated at 1000 ohm @ 100 MHz with a Direct Current Resistance (DCR) ranging from 0.5 ohm to 1.5 ohm.

Beads with a DCR less than 0.5 ohm may not effectively suppress the converter ripple, whereas those with a DCR greater than 2 ohm will cause a voltage drop that results in reduced SPA output power.

Table 3-4 Recommended DC-DC inductors (9.1 nH)

Reference	Value	DC Resistance (Max)	Saturation Current	Size L x W x H (mm)	Mfg Part #
L5	9.1 nH	0.4 Ω	250 mA	0.6 x 0.3 x 0.3	Murata LQP03TN9N1J02

Table 3-5 Recommended DC-DC inductors (2.2 μ H)

Reference	Value	DC Resistance (Typ)	Saturation Current	Size L x W x H (mm)	Mfg Part #
L6	2.2 μ H \pm 20%	0.2 Ω	250 mA	1.6 x 0.8 x 0.8	Murata LQM18PN2R2MGH
		0.3 Ω	250 mA	1.6 x 0.8 x 0.8	Sunlord MPH160809S2R2
		0.38 Ω	300 mA	1.6 x 0.8 x 0.8	Murata LQM18PN2R2MFH
		0.41 Ω	1.05 A	1.75 x 1.05 x 1.0	Scientific SDHK1608HB2R2MT

Tip:

- The 2.2 μH DC-DC inductors are adopted in DC-DC buck converter circuits in Pulse Skip Mode (PSM) and play a crucial role in these circuits. The saturation current of the circuit, which is the current value at which the nominal inductance decreases by 30%, should be equal to or higher than 250 mA. To ensure secure operation and to improve the performance of GR533x, inductors with higher saturation current and lower direct current resistance are preferred, because a higher direct current resistance means higher power consumption.
- If the system is powered by SYS_LDO, the 9.1 nH inductor and the 2.2 μH inductor can be removed from the power supply scheme.
- In scenarios where a magnet is close to the DC-DC inductor in the device system, it is recommended to choose the magnetically shielded inductor from Scientic (SDHK1608HB2R2MT) to reduce the impact of external magnetic fields on the inductance.

3.1.2 Clock

3.1.2.1 Introduction

GR533x clock source is generated by an external 32 MHz crystal oscillator, and the real-time clock by an external 32.768 kHz crystal oscillator.

3.1.2.2 HFXO_32M

The system clock, or CPU clock, is provided by an external 32 MHz crystal oscillator which connects to the XO_IN and XO_OUT pins of the SoC.

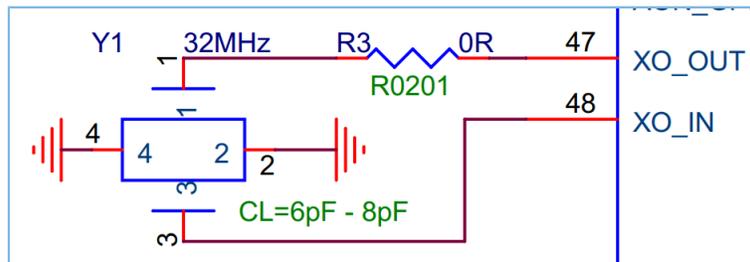


Figure 3-9 External 32 MHz crystal oscillator connection

Table 3-6 shows the specifications for the 32 MHz crystals that can be used for applications, and Table 3-7 shows several recommended crystal candidates.

Table 3-6 32 MHz crystal specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Crystal Freq	Crystal oscillator frequency	-	32	-	MHz
ESR	Equivalent series resistance	-	-	100	Ohm
C _{load}	Load capacitance	6	-	8	pF
f-Xtal	Crystal frequency initial tolerance	-	-	±50	ppm

Parameter	Description	Min.	Typ.	Max.	Unit
f-Xtal	Crystal frequency tolerance – over temperature	-	-	±30	ppm
f-Xtal	Crystal frequency tolerance – aging over life of product	-	-	±10	ppm
P _{DRV}	Maximum drive power	-	-	100	μW

Table 3-7 Recommended 32 MHz crystals

Part Number	ABRACON ABM11W-32MHz-6-R50-J2X	Murata XRCGB32M000F1SBAR0	Murata XRCGB32M000F1SAAR0	TXC 8Z32000004
Frequency	32 MHz	32 MHz	32 MHz	32 MHz
Initial tolerance	±20 ppm	±10 ppm	±10 ppm	±10 ppm
Tolerance over Temp.	±20 ppm	±20 ppm	±15 ppm	±20 ppm
Load capacitance	6 pF	6 pF	6 pF	8 pF
ESR	≤ 50 Ω	≤ 50 Ω	≤ 50 Ω	≤ 60 Ω
Temperature range	-40°C to +105°C	-40°C to +105°C	-40°C to +85°C	-40°C to +85°C
Size (L x W x H, mm)	2.0 x 1.6 x 0.5	2.0 x 1.6 x 0.65	2.0 x 1.6 x 0.65	2.5 x 2.0 x 0.55

Note:

- To ensure system stability and XO accuracy, load capacitance of the 32 MHz crystal oscillator should be within the range from 6 pF to 8 pF.
- The 32 MHz crystal oscillator does not require external load capacitors, but it needs to use the mass production tool for frequency offset calibration.
- When designing an application circuit, it is necessary to reserve interfaces or test points for the mass production tool. These include the required SWDCLK, SWDIO, CLK_TRIM (any GPIOs except MSIOs), GND, VBAT, and the optional MSIO_7.

3.1.2.3 LFXO_32K

The GR533x uses a low-power, low-frequency clock in sleep modes, which also extends battery lifespan. The utilization of the external 32.768 kHz crystal oscillator provides better accuracy, resulting in lower overall power consumption.

Note:

For applications that require less accurate real-time clocks, use an internal LFRC_32K instead of an external 32.768 kHz crystal oscillator to save device cost.

The GR533x integrates an adjustable load capacitance, so that the external 32.768 kHz crystal oscillator can be directly connected to the RTC_IN and RTC_OUT pins of GR533x, and no external load capacitors are required.

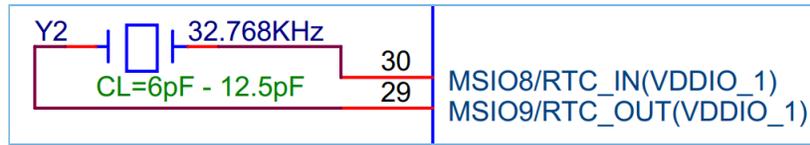


Figure 3-10 External 32.768 kHz crystal oscillator connection

The external crystal must meet the recommended operating conditions as indicated in Table 3-8, and Table 3-9 shows examples of crystals that meet the specifications.

Table 3-8 32.768 kHz crystal oscillator recommended operating conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Crystal Freq	Crystal oscillator frequency	-	-	32.768		kHz
ESR	Equivalent series resistance	-	-	-	100,000	Ohm
C _{load}	Load capacitance	-	6	-	12.5	pF
f-Xtal	Crystal frequency initial tolerance	-		-	±50	ppm
f-Xtal	Crystal frequency tolerance – over temperature and aging	-		-	±250	ppm
P _{DRV}	Max drive power	-	-	-	0.5	μW

Table 3-9 32.768 kHz crystal oscillator example specifications

Part Number	ABRACON ABS05-32.768KHZ-9-T
Frequency	32.768 kHz
Initial tolerance	±20 ppm
Tolerance over Temp.	±250 ppm
Load capacitance	9 pF
ESR	90,000 ohm
Temperature range	-40°C to +85°C
Size (L x W x H, mm)	1.6 x 1.0 x 0.50

Note:

To ensure system stability and XO accuracy, load capacitance of the 32.768 kHz crystal oscillator should be within the range from 6 pF to 12.5 pF.

3.1.3 RF

3.1.3.1 Introduction

GR533x integrates a 2.4G RF transceiver, which operates based on the mechanisms described below:

- On the receiver side:
 1. After the antenna receives an RF signal, the receiver digitizes the signal in a path: Low noise amplifier (LNA) > Mixer > Baseband (BB) amplifier > an analog-to-digital converter (ADC).
 2. The digitized signals are sent to the digital frontend (DFE) for demodulation.
 3. The digital frontend provides Automatic Gain Control (AGC) feedback signals to adjust the gain of the LNA and BB amplifier to maximize the signal-to-noise ratio (SNR) at the demodulation.
- On the transmitter side:
 1. The digital signal from the DFE is transmitted to a phase-locked loop (SXPLL) for modulation.
 2. The modulated carrier is delivered to a power amplifier (PA) with amplification factor configurable by the digital gain settings.
 3. The modulated carrier is transmitted to the antenna through a low-power or high-power PA path. The antenna radiates the amplified carrier through electromagnetic waves.

GR5332 differs from GR5331/GR5330 in the transceiver in use. The block diagrams of the two types of transceivers are presented in [Figure 3-11](#) and [Figure 3-12](#).

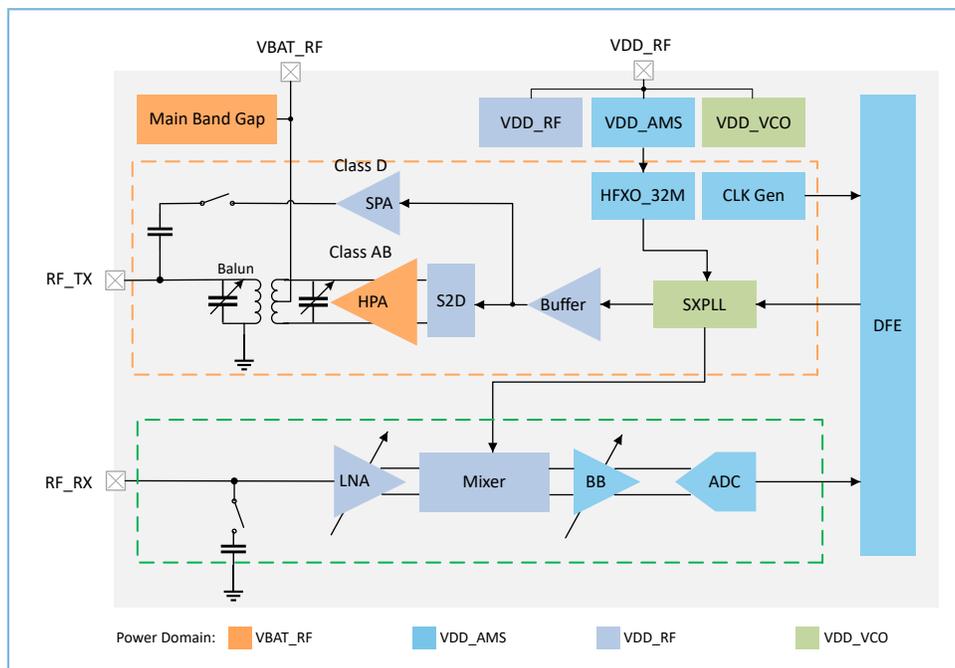


Figure 3-11 GR5332 transceiver block diagram

Note:

- Choose a high-power amplifier (HPA) or a small-power amplifier (SPA) for GR5332 based on the transmission power needed. An HPA supports transmission power between -10 dBm and 15 dBm, whereas -20 dBm and 5 dBm is supported for an SPA.
- The reference clock of SX PLL is generated by HFXO_32M.

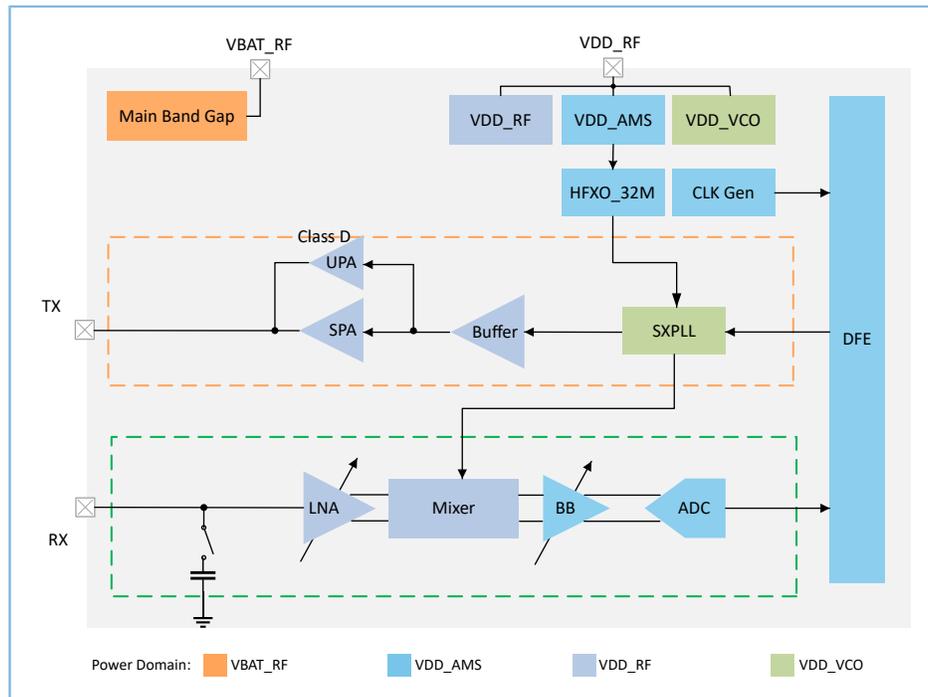


Figure 3-12 GR5331/GR5330 transceiver block diagram

Note:

- Choose a small-power amplifier (SPA) or an ultra-low power amplifier (UPA) for GR5331/GR5330 based on the transmission power needed. An SPA supports transmission power between -20 dBm and 6 dBm, whereas -15 dBm and 2 dBm is supported for a UPA.
- The reference clock of SX PLL is generated by HFXO_32M.

For detailed information about RF PA selection and matching circuit for GR533x, see *GR533x RF PA Application Note*.

3.1.3.2 RF Scheme

The following figure is the recommended RF matching circuit in the GR533x SoC minimal system.

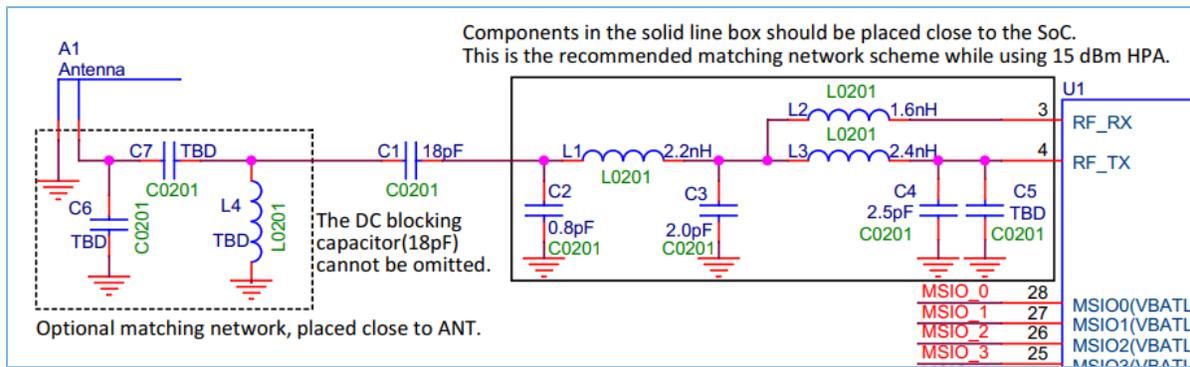


Figure 3-13 RF scheme

Two matching networks are recommended for the RF TRX path from the RF_TX/RX pin to the antenna, to achieve the matching of PA output impedance to antenna impedance.

- Antenna matching network

In the circuit, the left PI matching network (composed the inductor L4 plus capacitors C6 and C7) matches the antenna. Values of the matching component are adjusted according to the actual antenna used. It is recommended to use mature antenna schemes and recommended values from antenna manufacturers.

- SoC matching network

The PI type matching network (composed of the inductors L1, L2, and L3 plus capacitors C2, C3, C4, and C5) on the right matches the PA output impedance of GR533x.

Note:

- For GR5332 SoCs, C5 is reserved for tuning, and thus is not connected by default. For GR5331/GR5330 SoCs, C5 (0.3 pF) is used to suppress seventh-order harmonics.
- The DC blocking capacitor (C1) that connects the two matching networks cannot be omitted.

The recommended capacitors and inductors are specified in the table below by taking GR5332CENE (in QFN48) as an example.

Table 3-10 Recommended components for the RF section

Reference	Description	Value	Package Size	Mfg Part #
C1	CAP, CER, 18 pF (±5%), NPO, 0201, 50 V, -55°C to +125°C	18 pF	0201	Murata GRM0335C1H180JA01
C2	CAP, CER, 0.8 pF (±0.05 pF), NPO, 0201, 50 V, -55°C to +125°C	0.8 pF	0201	Murata GRM0335C1HR80WA01
C3	CAP, CER, 2.0 pF (±0.1 pF), NPO, 0201, 50 V, -55°C to +125°C	2.0 pF	0201	Murata GRM0335C1H2R0BA01
C4	CAP, CER, 2.5 pF (±0.1 pF), NPO, 0201, 50 V, -55°C to +125°C	2.5 pF	0201	Murata GRM0335C1H2R5BA01

Reference	Description	Value	Package Size	Mfg Part #
L1	Inductor, CHIP, 2.2 nH (± 0.1 nH), 200 mohm, Q = 14 @ 250 MHz, -55°C to +125°C, 0201	2.2 nH	0201	Murata LQP03TN2N2B02
L2	Inductor, CHIP, 1.6 nH (± 0.1 nH), 150 mohm, Q = 14 @ 250 MHz, -55°C to +125°C, 0201	1.6 nH	0201	Murata LQP03TN1N6B02
L3	Inductor, CHIP, 2.4 nH (± 0.1 nH), 200 mohm, Q = 14 @ 250 MHz, -55°C to +125°C, 0201	2.4 nH	0201	Murata LQP03TN2N4B02

 **Note:**

For details about the RF matching components specific to a GR533x part number, see the corresponding BOM table.

3.1.4 I/O Pins

The GR533x has software-configurable I/O pin assignment where different peripherals can be multiplexed out on different chip pins. When configured to GPIOs, they can be set as input, output, with configurable pull-up or pull-down resistors. I/O pins retain their last state when system enters the sleep or ultra deep sleep mode. Only AON_GPIOs can be used to wake up the system from sleep modes.

 **Note:**

- All I/Os can retain their output levels when the system enters sleep mode. During sleep mode, if an I/O is set to input mode, the external level should either be a specified high level (where the external voltage equals the corresponding I/O power domain voltage) or a low level (0 V). Any other voltage may cause leakage current and result in excessive power consumption in sleep mode.
- MSIO_0–MSIO_9 are in high impedance state by default.
- Except MSIO_0–MSIO_9, the I/O default state is input mode with pull-down.
- All I/Os (except MSIO_0–MSIO_9) can be configured as being triggered by high level, low level, rising edge, falling edge, or both edges.
- All I/Os support four configurable output drive strengths and two slew rate options: The fast slew rate should be used when speed or timing is a concern; the slow slew rate is used to reduce the switching noise.
- All I/Os can be individually multiplexed to all peripherals for layout flexibility.
- Input voltages of all I/Os and VIO_LDO_OUT/VDDIO_1 should not be higher than the VBATL voltage.

3.1.5 SWD Interfaces

GR533x connects to J-Link for debugging by using Serial Wire Debug (SWD) interfaces. The following table shows the pins to which the SWD interfaces connect in QFN48 and QFN32 packages.

Table 3-11 Pin matching for SWDIO and SWCLK in QFN48 and QFN32 packages

SWD	Pin # (QFN48)	Pin # (QFN32)
SWD_CLK	GPIO_0 (Pin 6)	GPIO_0 (Pin 8)
SWD_IO	GPIO_1 (Pin 7)	GPIO_1 (Pin 9)

These pins can be multiplexed as GPIOs when the SWD interfaces are not in use.

3.2 PCB Design and Layout Guideline

3.2.1 PCB Layer Stackup

A 4-layer PCB layout is recommended to be used for all GR533x package options. Figure 3-14 shows the recommended layer stackup (thickness: 1.6 mm) of GR533x.

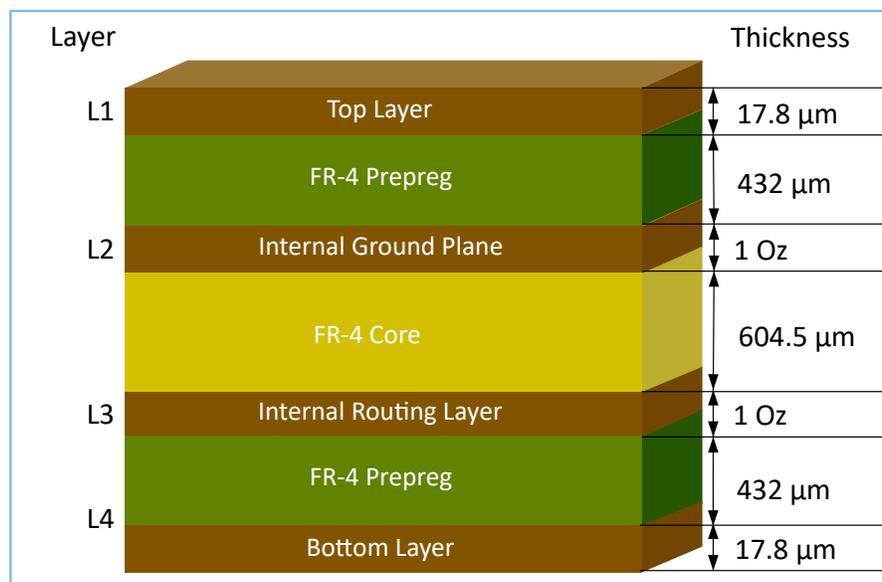


Figure 3-14 PCB layer stackup

- L1: top layer where components, RF transmission lines, and key signal lines are placed
- L2: internal ground plane, used for both the ground return path and the reference plane for the 50 ohm RF transmission line
- L3: internal routing layer, used to split power domains and place a small number of signal lines
- L4: bottom layer; it is recommended to maintain a complete ground plane.

3.2.2 Components Layout

All components operating at high frequency should have their layout made as compact as possible. This will prevent the cross-coupling between lines and also minimize the parasitic effects which will have a negative impact on the operating parameters.

When designing the layout, make sure the GR533x SoC is placed as close to the antenna interface as possible, and no other traces or components are under the RF routing if possible (the layout and routing of RF components are of higher priority).

3.2.3 Power Supply

Power supply is essential to ensure proper operation of an SoC, and therefore special attention should be paid on the layout and routing of the key power systems, which are DC-DC switching regulator and RF input power supply. To avoid system-level issues (such as poor performance in ESD protection and radiation off limits) caused by improper power design, abide by the design hints described in the two following sections.

3.2.3.1 DC-DC Switching Regulator

The chip includes a DC-DC switching regulator. To design the PCB layout involving a DC-DC switching regulator,

1. Minimizing the size of the DC-DC input/output loop is crucial to ensure optimal power quality. To achieve this, the DC-DC input capacitor, C11 (10 μ F), should be placed as close to the VBATL pin as possible, and the GND of the DC-DC output capacitor, C16 (2.2 μ F), should be as close to the GND of C11 (10 μ F) as possible. Additionally, ground vias should be placed around the GND pads of the input/output capacitors. For devices in QFN48 package, it is recommended to connect the GND pads of the DC-DC input/output capacitors directly to the VSS_BUCK pin via the ground plane; for devices in QFN32 package, where the VSS_BUCK pin is within the chip and bonded to the E-PAD, it is essential to route the GND pads of the input/output capacitors to return to the E-PAD projection area along the shortest path, in order to minimize the DC-DC input/output loop.
2. Components (9.1 nH inductor, 2.2 μ H inductor, and 2.2 μ F capacitor) connected to DC-DC switching regulator should be placed as close to the VSW and VREG pins of the chip as possible. A distance within 3 mm is recommended.
3. The net of VSW radiates stronger interference before VSW signals passing through the inductors, and thus should be placed at a minimum distance of 0.2 mm from other power nets and signals, especially V1P2 and DIGCORE.
4. The power trace of VREG should go through the DC-DC output capacitor (C16) first before being connected to VREG.
5. For devices in QFN48 package, it is recommended to connect the VSS_BUCK pin to the E-PAD through vias. Avoid connecting them on the same layer.

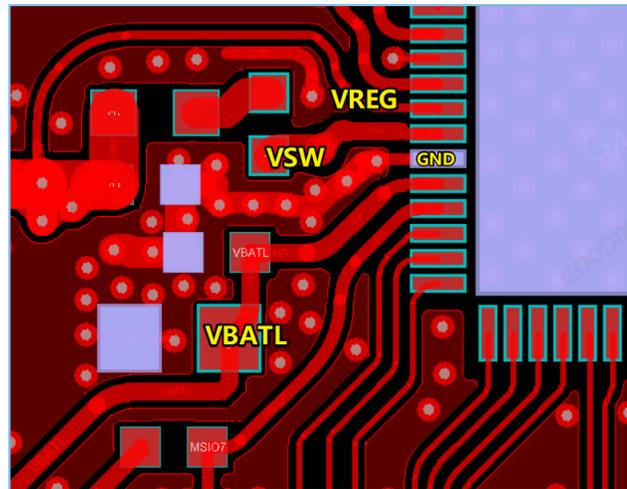


Figure 3-15 Reference layout and routing for DC-DC switching regulator (QFN48 device)

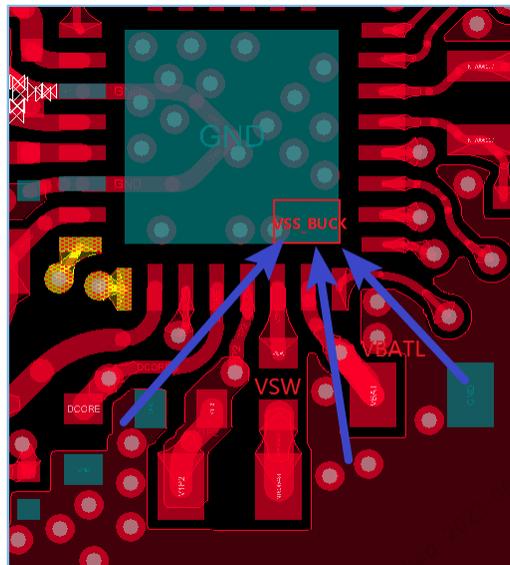


Figure 3-16 Reference layout and routing for DC-DC switching regulator (QFN32 device)

3.2.3.2 RF Input Power Supply

Make sure the following instructions are met when designing RF input power supply in PCB layout, to ensure optimal performance and to avoid excessively high radiation.

1. Decoupling capacitors connected to VDD_VCO and VBAT_RF should be as close to the corresponding pin as possible (around 1 mm is recommended, and should not exceed 3 mm). Place the capacitors on the same layer with the chip if possible, and make sure the routed trace goes through the capacitors first and then connected to the chip power pins. In case the capacitors are not placed on the same layer with the chip, they can be connected through vias, and the vias should be located close to the decoupling capacitors.
2. The power trace should be as short as possible, and at least 0.2 mm wide. A minimum distance at 0.2 mm from other signals should be guaranteed.

- It is recommended to route the V1P2 network directly through the area on the routing layer that is projected by E-PAD (GND) on the bottom of the SoC. If the SoC is placed on Layer 1: For a double-layer PCB layout design, V1P2 network routing shall pass through the E-PAD projection area on Layer 2; for a four-layer PCB layout design, V1P2 network routing shall pass through the E-PAD projection area on Layer 3, as shown below. Moreover, please be cautious not to route the trace too close to the GND plane near the RF pins.

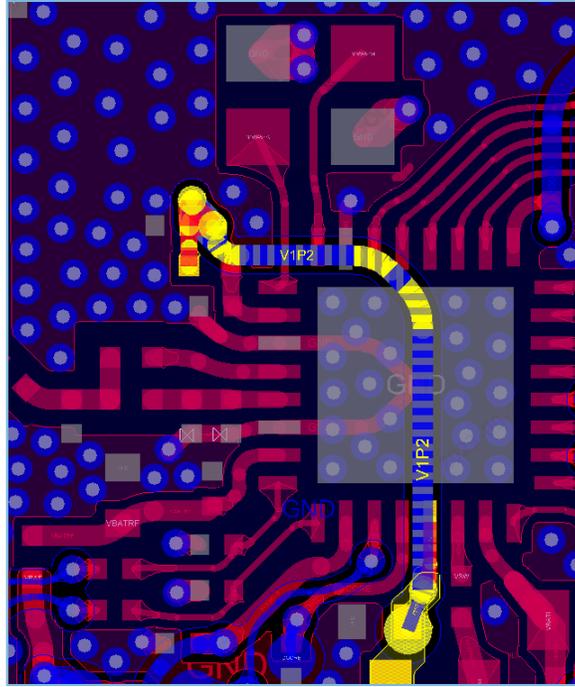


Figure 3-17 Reference layout and routing for RF input power supply

3.2.4 Clock

Place the crystal as close as possible to the corresponding pin of the chip (recommended distance: ≤ 4 mm). This will minimize any additional capacitive load on the input pins and reduce the chance of crosstalk and interference with other signals on the board. Make sure there is no other trace routed next to/under the crystal or the crystal routing traces. Shield the routing traces of the 32 MHz crystal with GND traces.

By taking 4-layer PCB as an example, if the ground below the crystal is clean and no crosstalk or interference is involved, provide openings underneath the crystal pads (as shown in [Figure 3-19](#)) to reduce parasitic capacitance.

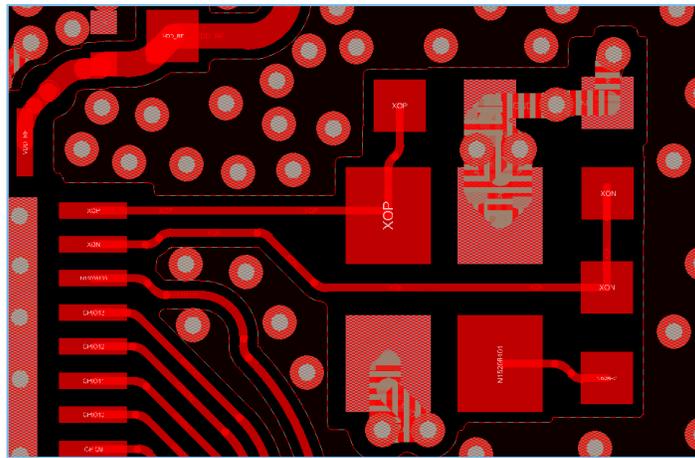


Figure 3-18 Reference clock layout for 4-layer PCB in QFN48

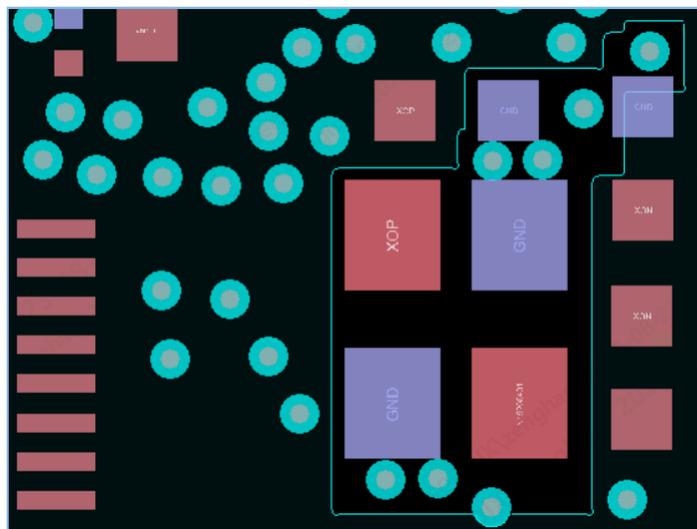


Figure 3-19 Openings under XO pads on 4-layer PCB

3.2.5 RF Port

A copper trace with a characteristic impedance of $50\ \Omega$ is required to interconnect the RF port and the antenna. Because the impedance of RF port is not $50\ \Omega$, a matching network is required to match the port impedance between the RF port and the $50\ \Omega$ transmission line.

Components in this matching network should be placed as close to the RF pins (RF_RX and RF_TX) as possible. Try to place the first component no further than 1 mm from the RF pin.

Figure 3-20 shows the PCB layout of the RF port.

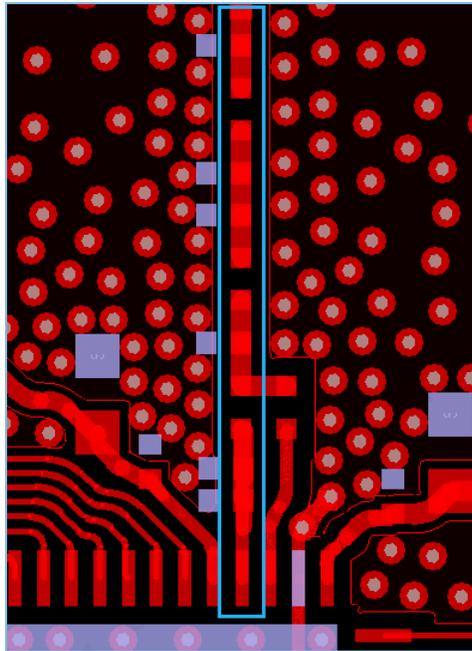


Figure 3-20 RF port PCB layout

Note:

- The RF routing traces should be straight and as short as possible. If a curving trace is necessary for a specific structure, an inverted arc is required for a turning, and angles at or less than 90° are not allowed.
- RF routing at the PCB surface (the top layer or the bottom layer) helps avoid using vias or switching layers, and is therefore preferred. Stub routing should be avoided.

Taking the 4-layer PCB layout design as an example, the transmission line is routed as a microstrip using layer-2 ground as the reference plane. The dimensions are:

- Trace width: 559 μm
- Spacing from trace to top layer: 178 μm
- Spacing from top layer to layer 2: 432 μm

The design uses FR-4 dielectric and 0.5 ounce copper on the outer layer. In actual design, PCB manufacturers are required to provide RF traces with an impedance of 50 Ω (+/-10%).

Ground vias should be placed along the transmission line every 1.25 mm and right next to the ground pads of the matching components.

In addition, the antenna matching components should be placed close to the antenna feedpoint.

3.2.6 RSE Certificate Recommendations

Board-level RF radiation might cause an SoC to fail in passing FCC RSE certificate. Such radiation comes from various sources, including SoC package, wafer, PCB circuit path (major source), and antenna.

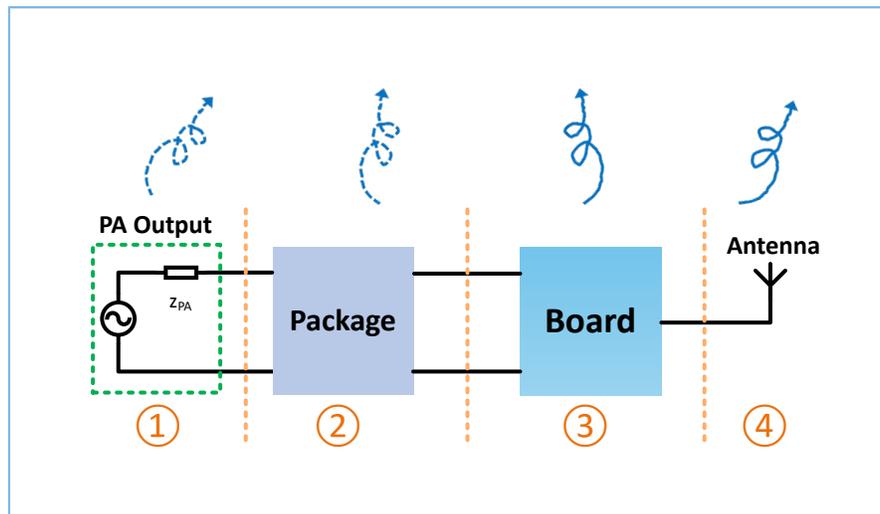


Figure 3-21 RF radiation sources from GR533x

To enhance RF performance and minimize PCB radiation, follow the layout and routing recommendations on RF port below:

- Placing RF matching components on the same line with RF_TX is of high priority, as shown in the blue box in [Figure 3-20](#). Make sure the components are placed by strictly following the RF scheme in [Figure 3-13](#).
- Place the first capacitor to ground and series inductors in the RF path as close to the RF pins as possible, to limit current diffusion and harmonic resonance.
- Place vias at the edge of copper pour area near RF_TX/RX traces (along the return path) with the spacing of 1.5 mm or below.
- Place two vias close to the ground point of the first capacitor to ground, to curb current diffusion in the copper area on the top layer.
- Place the GND pads of the matching components in the same direction if possible. It is recommended to place the pads facing the RF_TX pin.
- Place the decoupling capacitors in VBAT_RF/VDD_RF networks as close to the corresponding chip pins as possible, which helps reduce radiation.
- Make sure no trace is routed on the reference ground beneath the VBAT_RF/VDD_RF/RF_TX/RF_RX networks near the RF port, as shown in [Figure 3-20](#). A complete and clean reference ground helps reduce radiation.
- Avoid connecting the VREG network to the VDD_RF pin by routing through the RF routing reference layer. Instead, it is recommended to pass through the E-PAD projection area, as shown in [Figure 3-17](#).

- Route out from the GPIOs close to RF_TX for a certain distance before drilling vias and routing the GPIOs to other layers. Avoid placing vias by the GPIOs at the edge of the SoC package. It is recommended to place the filter capacitors reserved for GPIO0/1 on the same layer as the SoC.
- The traces connecting matching components are not transmission lines, because they are far shorter than the wavelength. Make sure the traces are of the same width with the component pads if possible.
50 Ω impedance should be guaranteed for the RF transmission lines after conversion through the RF matching network.
- VSS_RF and PA_GND should be connected with EPAD on the same layer.
- To reduce radiation, in the recommended four-layer PCB layout, make sure the RF reference ground (Layer 2) is complete; place GPIO traces and power traces on Layer 3 if possible.
For a two-layer PCB structure, board thickness equal to or lower than 0.8 mm is recommended. Make sure the EPAD and the reference ground of RF routing are cleared from routing and complete. Reserve a shielding case used for RSE certificate on the top layer.
- Place GND vias along the clearance zone by the PCB edge at the spacing (normally between 40 mil and 50 mil) no shorter than 1/10 of the wavelength of the tenth-order harmonics.
- For GR5331/GR5330, using a 0.3 pF capacitor (C5) in the RF matching circuit can effectively suppress seventh-order harmonics. Place the capacitor as close to the RF_TX pin as possible. GRM0335C1HR30WA01 is recommended, which features the lowest impedance around the seventh-order harmonics, as shown in [Figure 3-22](#).

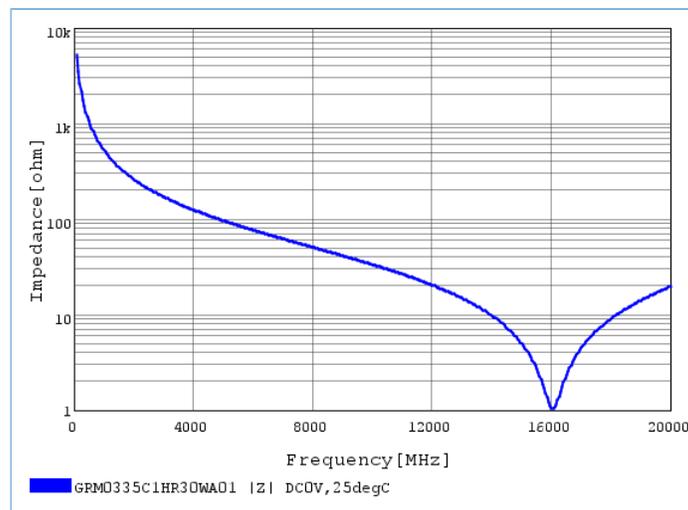


Figure 3-22 Impedance/frequency characteristics of GRM0335C1HR30WA01

3.3 ESD Protection Design

3.3.1 System-level ESD Design

System efficient electrostatic discharge (ESD) design is crucial for any circuits, and requires users to follow the design guidelines (including schematic diagrams, PCB layout, and product structural designs) provided in the sections below.

3.3.1.1 ESD Schematic Design

GR533x SoC is powered by an independent external LDO regulator (see “Section 3.1.1 Power Supply” for details). To suppress static electricity, it is recommended to connect a ferrite bead to each of the two charging pads (CHAR+ and CHAR-) in series, and connect a proper transient voltage suppressor (TVS) diode between the two ferrite beads to enhance ESD protection, as shown in the figure below.

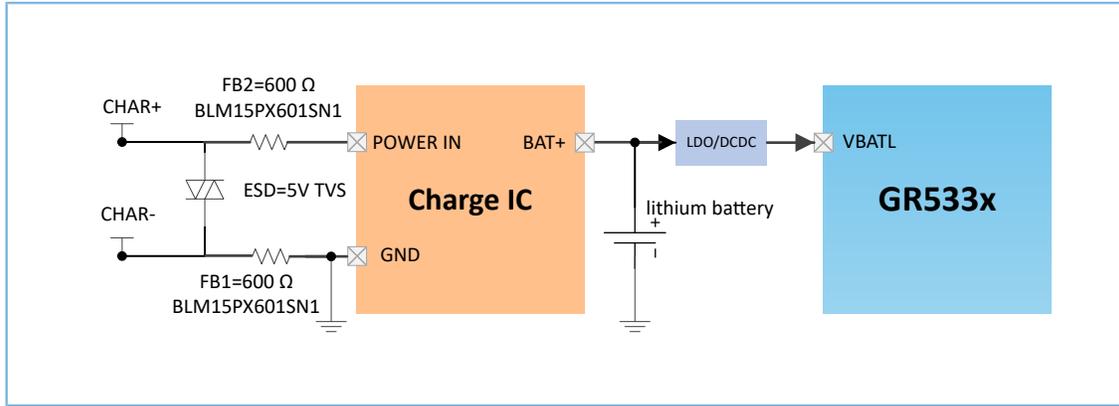


Figure 3-23 ESD protection scheme at charging pads

Recommended models of TVS diodes and ferrite beads, as well as model selection requirements, are listed in the tables below.

Table 3-12 Model selection for TVS diodes

Parameters	Description	Min.	Typ.	Max.
V_{RWM} (V)	Reverse stand-off voltage	-	5 V	-
V_{BR} (V)	Breakdown voltage	-	7 V	-
V_{clamp} (V)	Clamp voltage	-	6 V	-
V_{ESD} (kV)	ESD prevention performance	<ul style="list-style-type: none"> Contact discharge: ± 10 kV Air discharge: ± 12 kV 		-

Table 3-13 Model selection for ferrite beads

Parameters	Description	Min.	Typ.	Max.
Impedance @ 100 MHz (Ω)	Impedance @ 100 MHz	-	600 Ω	-
I_R (mA)	Rated operating current	-	900 mA	-
$R_{DC Max.}$ (m Ω)	Maximum DC resistance	-	230 m Ω	-

Table 3-14 Recommended TVS diodes

Part Number	V_{RWM} (V)	V_{BR} (V)	V_{clamp} (V)	Operating Temperature	V_{ESD} (kV)	Package	Manufacturer
AZ5C25-01B	5	9	6	-55°C to 85°C	<ul style="list-style-type: none"> Contact discharge: ± 13 kV 	0201	Amazing Micro.

Part Number	V _{RWM} (V)	V _{BR} (V)	V _{clamp} (V)	Operating Temperature	V _{ESD} (kV)	Package	Manufacturer
					<ul style="list-style-type: none"> Air discharge: ±16 kV 		
OVE38E32S1M	6.5	7	10	-55°C to 85°C	<ul style="list-style-type: none"> Contact discharge: ±25 kV Air discharge: ±25 kV 	0402	OVREG

Table 3-15 Recommended ferrite beads

Part Number	Impedance @ 100 MHz	Rated Current	Max. DC Resistance	Operating Temperature	Package	Manufacturer
BLM15PX601SN1	600 Ω	900 mA	230 mΩ	-55°C to 125°C	0402	Murata
WLBD1005HCU601TL	600 Ω	900 mA	230 mΩ	-55°C to 125°C	0402	Walsin

To protect products with metal shell against ESD, connect ferrite beads between metal shell GND and the GND on motherboard.

3.3.1.2 PCB Layout Design

- Live by the following rules for GR533x PCB grounding:
 - It is recommended to use PCB with four layers or above, and place GR533x SoC on the layer adjacent to the GND layer. Make sure the GND layer is solid and complete, to effectively prevent static from setting in.
 - Make sure the GND pin of the input capacitor (10 μF) is placed as close to the VSS_BUCK pin as possible, and is connected to EPAD on other layers through at least two vias near VSS_BUCK. The trace from VSS_BUCK to the GND should be 0.25 mm wide or above, to reduce power/GND loop impedance.
 - Avoid routing XO and VDD_RF along PCB edges, because the areas near XO and VDD_RF are ESD susceptible. It is recommended to wrap XO and VDD_RF routing with ground traces. The decoupling capacitors and ferrite bead connected to VDD_RF should be placed as close to chip pins as possible.
- To design the layout for charging pads,
 - It is not recommended to place charging pads (CHAR+ and CHAR-) and GR533x SoC on the same layer. However, if the charging pads and GR533x SoC are on the same layer, the spacing between the charging pads and the SoC should be at least 4 mm.



Figure 3-24 Charging pads layout

- Do not place charging pads close to ESD-sensitive signals (including clock, reset, and communication signals) and the crystal oscillator. Those signals should also be wrapped with ground traces.
- Place decoupling capacitors as close to the power pins of GR533x as possible, to keep the power return path the shortest, so as to enhance filtering performance.

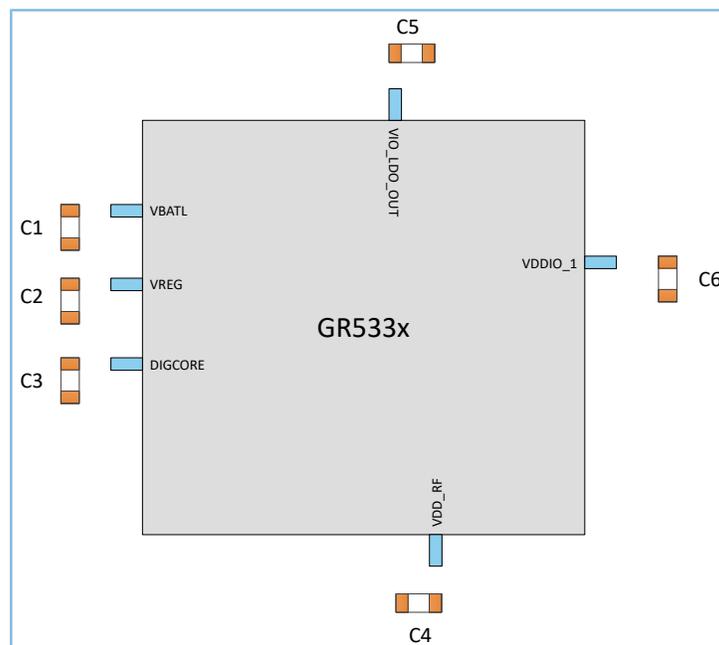


Figure 3-25 Decoupling capacitor layout for power supply

- It is recommended to place communication signals neither on the top layer nor the bottom layer in the PCB stack-up, due to the ESD susceptibility of I/O pins. Avoid routing signals susceptible to ESD events (such as clocks and reset pins) at the edge of the board. It is recommended to wrap the I/O pins and ESD susceptible signals with GND traces.

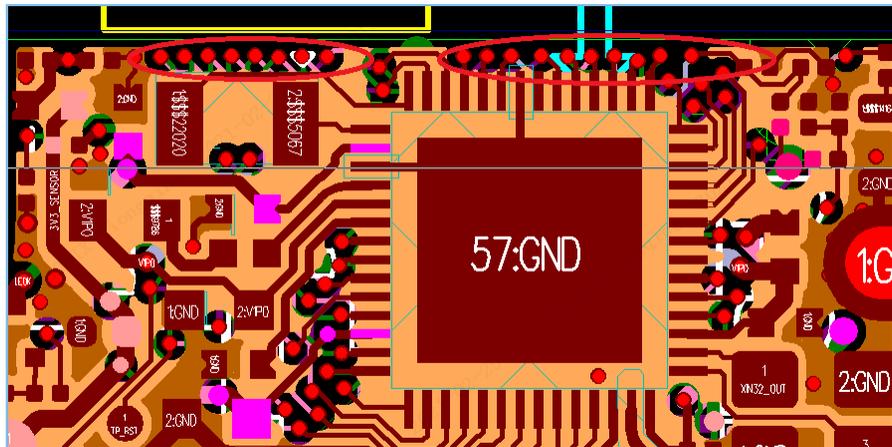


Figure 3-26 Improper I/O routing at board edge (not shielded by GND traces)

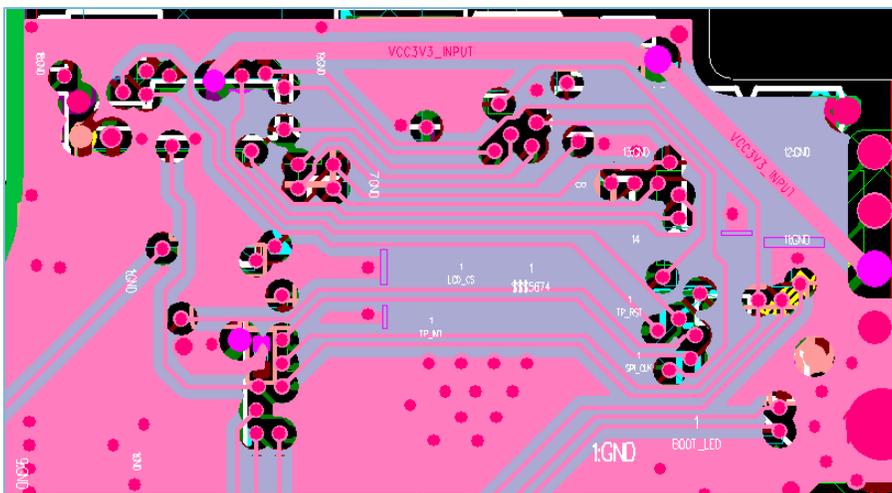


Figure 3-27 Proper routing of I/O pins

- The capacitors or ESD protection devices should be routed through the pad. Avoid using long traces to connect the capacitors/ESD protection devices to pad, which undermines filtering/protection performance.

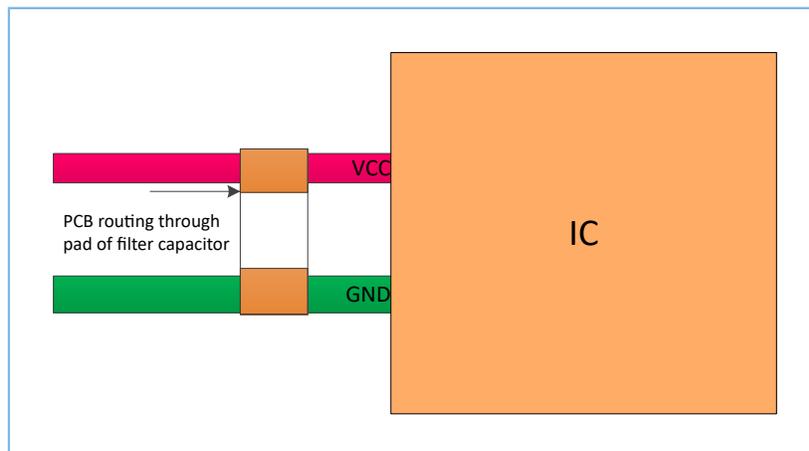


Figure 3-28 Proper routing for a capacitor (as an example)

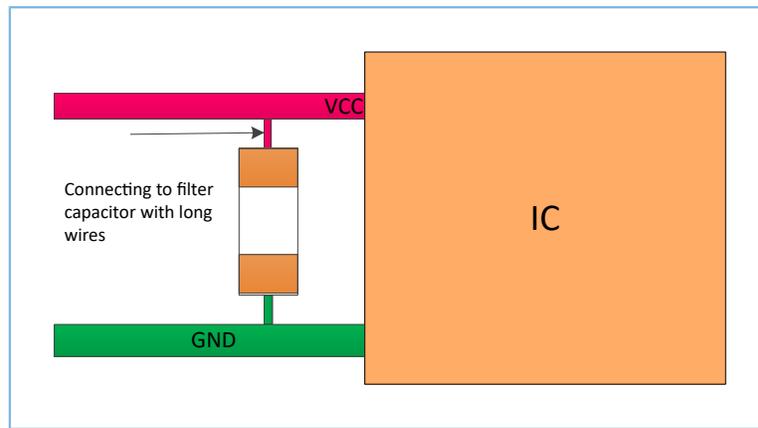


Figure 3-29 Improper routing for a capacitor (as an example)

3.3.1.3 Product Structural Design

- Make sure the shell gaps are sealed to prevent static electricity from setting in.
- Connect ferrite beads in series to the GND pins on the metal shell, and connect the GND pins to the GND circuit on the motherboard, to protect the motherboard from static electricity transmitted through the metal shell.
- Suspended metal structure is not allowed. The steel stiffener of sensors (such as touch/display sensors) should be grounded.
- Try to avoid close contact with the overlapped area between the FPC on the motherboard and the FPC on touch/display sensor module. It is recommended to apply heat resistant adhesives on the exposed area of motherboard connectors, to prevent short circuit or static electricity from setting in.

3.3.2 ESD Considerations in Production, Transport, and Debugging

To steer away from ESD events, stringent ESD control is also required during production, transport, debugging, and other relevant phases.

- Wear antistatic wrist strap in these processes. Touching the SoC with bare hands or using metal tweezers is forbidden.
- Use an antistatic bag/tray to hold the SoC.
- Countermeasures against ESD are essential for soldering irons, welding tables, and test instruments.
- Strictly comply with ESD preventive requirements for the production line during production and transport.

3.4 Reference Design

Taking GR5332CENE in QFN48 package as an example, the reference schematic is shown below.

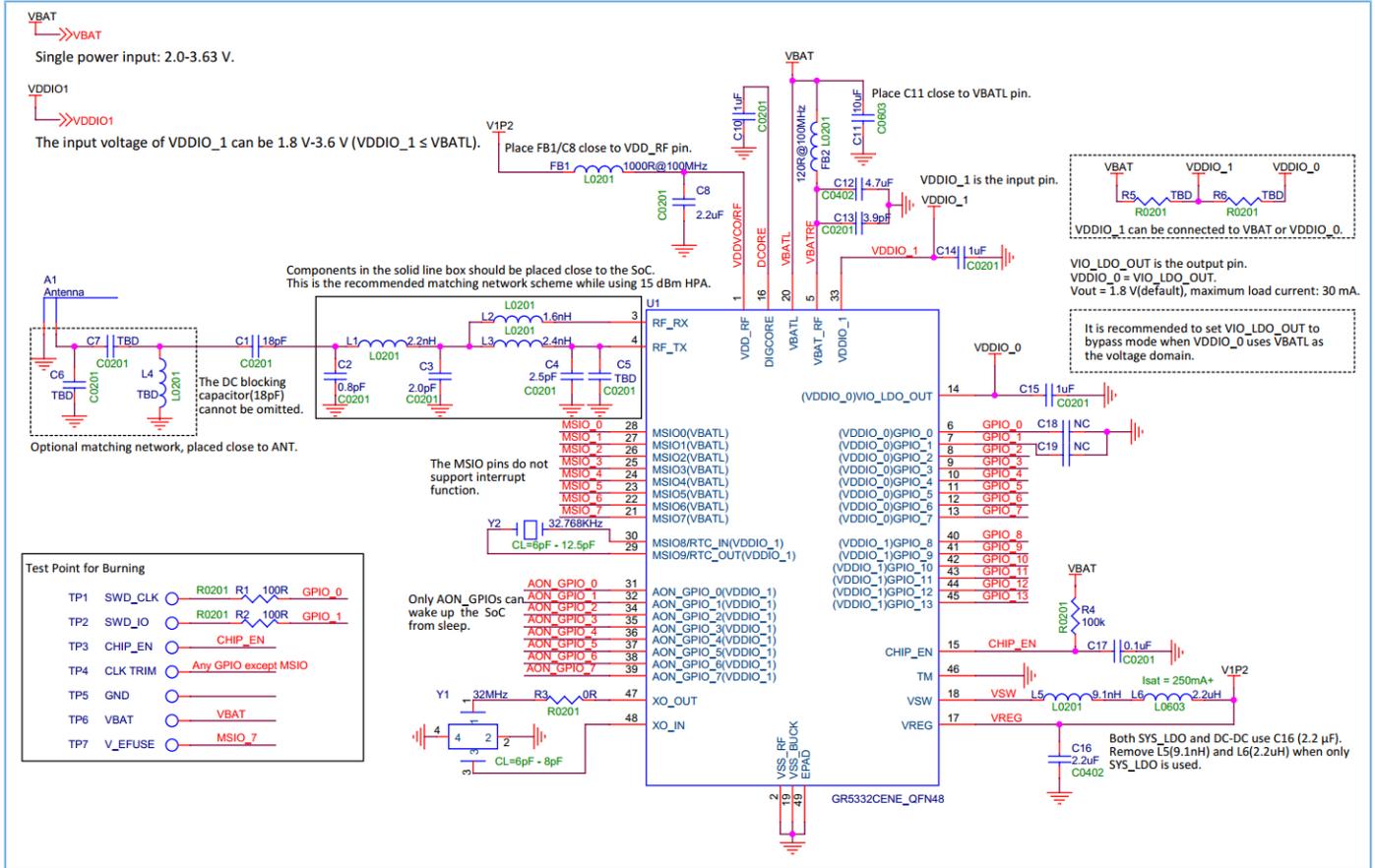


Figure 3-30 Reference schematic for GR5332CENE QFN48

Note:

For the reference schematic specific to each part number of GR533x, see the corresponding reference design in the GR533x Reference Design package.

4 FAQ

4.1 Why Is the Power Consumption in Sleep Modes High?

- Description

In power consumption tests, the power consumption in sleep mode varies depending on different I/O pin configurations. How to properly configure I/O pins before the SoC goes to sleep?

- Issue Analysis

The power consumption in sleep mode is high, and it may be because I/O pins are not properly configured.

- I/O pins are at floating state.
- I/O pins are configured in improper pull-up or pull-down state.

Above incorrect configurations can cause system leakage, so you need to properly configure the state of I/Os before the SoC enters sleep mode.

- Solution

Configure the state of I/O pins before the SoC enters sleep mode.

- If an I/O pin is in pull-up/pull-down state or used as a driver output, it needs no pull-up/pull-down configuration.
- If an I/O pin is not used or works in input mode without pull-up or pull-down, it needs to be configured to internal pull-down.

4.2 Can the RF Matching Circuits Be Simplified or Removed?

- Description

In designing a PCB, can I modify the recommended RF matching circuit layout due to limited space?

- Issue Analysis

GR533x recommends two matching circuits for RF: a matching circuit close to GR533x and a matching circuit close to the antenna. Whether these two matching circuits can be simplified or removed needs to be treated differently.

- Solution

The matching circuit close to GR533x is used to match GR533x internal PA and cannot be removed.

The matching circuit close to the antenna end is used to match the antenna, and its circuit can be changed according to the antenna you use. For the matching of the antenna, you can complete simple matching adjustment by the S11 parameter or the Smith chart from the vector network analyzer. However, for matching of other indicators (such as antenna gain and directionality), you are recommended to seek help from professional antenna factories.

5 Glossary

Table 5-1 Glossary

Name	Description
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AMS	Analog Mix Signal
BB	Baseband
Bluetooth LE	Bluetooth Low Energy
BUCK	Type of DC-DC Converter
CGU	Clock Generation Unit
DC-DC	DC-to-DC Converter
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
GPIO	General-purpose Input/Output
LDO	Low-dropout
LFXO	Low-frequency Crystal Oscillator
LNA	Low Noise Amplifier
LO	Local Oscillator
HFXO	High-frequency Crystal Oscillator
HPA	High Power Amplifier
PCB	Printed Circuit Board
PLL	Phase-locked Loop
PMU	Power Management Unit
PPM	Power Path Management
QFN	Quad Flat No-Lead Package
QSPI	Queued Serial Peripheral Interface
RoHS	Restriction of Hazardous Substances Directive
SiP	System-in-Package
SNSADC	Sense Analog-to-digital Converter
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SVHC	Substance of Very High Concern
SWD	Serial Wire Debug
Tg	Glass Transition Temperature

Name	Description
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter

6 Appendix: Assembly Guideline

The GR533x devices in QFN32 and QFN48 packages are qualified to MSL3 and are RoHS/green compliant. RoHS is the abbreviation of *Restriction of Hazardous Substances Directive*, which puts a limit on the amount of harmful substances in electronic devices, published by European Union in February 2003. MSL3 represents Moisture Sensitivity Level 3 which indicates that a moisture sensitive plastic device, once removed from a dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH before the solder reflow process.

GR533x storage conditions:

- Temperature: < 40°C
- Humidity: < 90% RH
- Period: 12 months

After opening the package: go through reflow for board assembly within 48 hours.

- Temperature: < 30°C
- Humidity: < 60% RH
- Stored at: < 10% RH

Both lead-free solder and Sn/Pb solder applications use the same rules for the general PCB design. Only the board surface finish and the board material have to be considered for lead-free application due to the higher reflow temperature and lead-free solder compatibility. A number of factors may have a significant effect on mounting QFN packages on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in exposed ground/thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow temperature profile.

Note:

It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort may be needed to optimize the process as per users' surface mount practices and requirements.

In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

Typically, the PCB pad pattern for an existing package is designed based on guidelines developed within a company or by following industry standards such as IPC-SM-782. For the purpose of this document, methodology of Association Connecting Electronics Industries (IPC) is used here for designing PCB pad pattern. However, because of exposed die paddle and the package lands on the bottom side of the package of GR533x, certain constraints are added to IPC's methodology. The pad pattern developed here includes considerations for lead and package tolerances.

6.1 Package Information

This section provides comprehensive details on mechanical packaging information.

6.1.1 QFN32

The following table illustrates the dimensions of a device in QFN32 package, which is qualified to MSL3.

Table 6-1 QFN32 package information

Parameter	Value	Unit	Tolerance
Package Size	4.0 x 4.0	mm	±0.05 mm
QFN Pad Count	32		
Total Thickness	0.75	mm	±0.05 mm
QFN Pad Pitch	0.4		
Pad Width	0.2		±0.05 mm
Exposed Pad Size	2.8 x 2.8		±0.1 mm

The figure below shows the QFN32 package outlines.

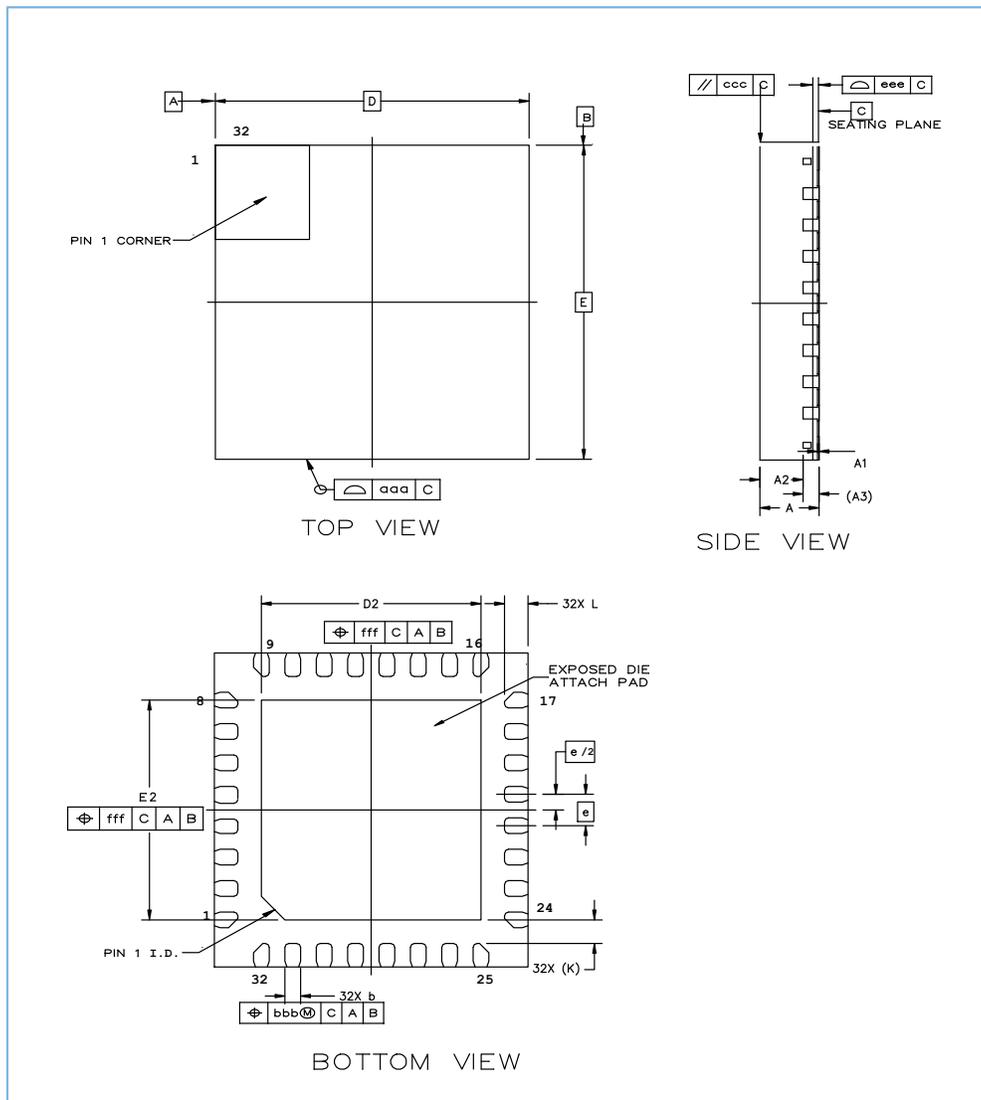


Figure 6-1 QFN32 package outlines

Note:

Drawing is not to scale.

Table 6-2 QFN32 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.550	-	-	0.022	-
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010

Symbol	Dimensions in mm			Dimensions in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
D	4.000 BSC.			0.157 BSC.		
E	4.000 BSC.			0.157 BSC.		
e	0.400 BSC.			0.016 BSC.		
D2	2.700	2.800	2.900	0.106	0.110	0.114
E2	2.700	2.800	2.900	0.106	0.110	0.114
L	0.200	0.300	0.400	0.008	0.012	0.016
K	0.300 REF.			0.012 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

 **Note:**

Values in inches are converted from values in millimeters and rounded to three decimal digits.

6.1.2 QFN48

The following table illustrates the dimensions of a device in QFN48 package, which is qualified to MSL3.

Table 6-3 QFN48 package information

Parameter	Value	Unit	Tolerance
Package Size	6.0 x 6.0	mm	± 0.1 mm
QFN Pad Count	48		
Total Thickness	0.75	mm	± 0.05 mm
QFN Pad Pitch	0.40		
Pad Width	0.20		
Exposed Pad Size	4.6 x 4.6		± 0.01 mm

The figure below shows the QFN48 package outlines.

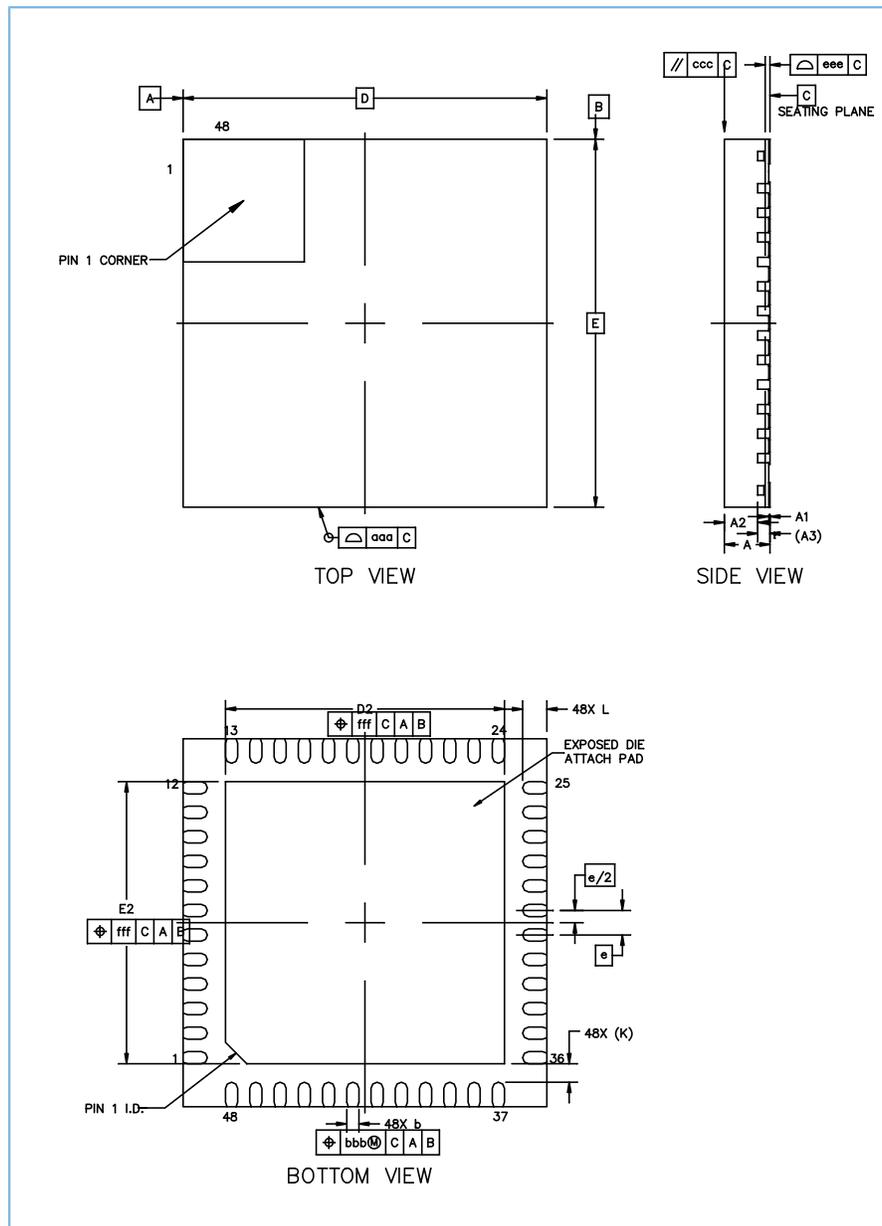


Figure 6-2 QFN48 package outlines

Note:

Drawing is not to scale.

Table 6-4 QFN48 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.550	-	-	0.022	-

Symbol	Dimensions in mm			Dimensions in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	6.000 BSC.			0.236 BSC.		
E	6.000 BSC.			0.236 BSC.		
e	0.400 BSC.			0.016 BSC.		
D2	4.500	4.600	4.700	0.177	0.181	0.185
E2	4.500	4.600	4.700	0.177	0.181	0.185
L	0.300	0.400	0.500	0.012	0.016	0.020
K	0.300 REF.			0.012 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeters and rounded to three decimal digits.

6.2 Board Mounting Guideline

Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for QFN packages. This is further complicated by the large grounding die pad underneath QFN packages and the proximity to the inner edges of the leads.

Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Because surface mount process varies from company to company, careful process development is recommended.

6.2.1 Stencil Design for Perimeter Pads

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 mils to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement.

The first step in achieving reliable solder joints is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

- Area ratio = area of aperture opening/aperture wall area

- Aspect ratio = aperture width/stencil thickness

For rectangular aperture openings, as required for chip packages, these ratios are given as:

- Area ratio = $LW/2T(L + W)$
- Aspect ratio = W/T

L and W are the aperture length and width, and T is stencil thickness. For optimum paste release, the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release.

It is also recommended that the stencil aperture tolerances should be tightly controlled, as these tolerances can effectively reduce the aperture size. It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the center exposed pad region. See [Figure 6-3](#) for reference solder mask design in the center of the package.

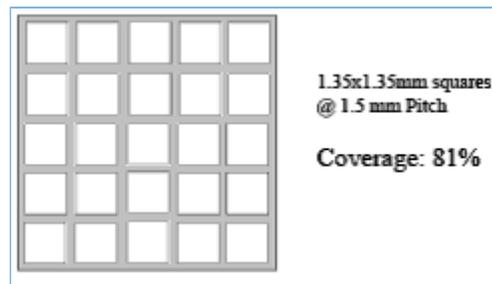


Figure 6-3 Exposed/Ground pad stencil design recommendation for QFN packages

6.2.2 Via Types and Solder Voiding

Voids within solder joints under the exposed grounding pad can have an adverse effect on high-speed and RF applications. Voids within this ground plane can increase the current path of the circuit.

The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any one via would not be rendered ineffectual based on any one void increasing the current path beyond the distance to the next available via.

6.2.2.1 Stencil Thickness and Solder Paste

The stencil thickness of 0.125 mm is recommended for 0.35 mm pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 paste (IPC standard J-STD-005) be used for mounting QFN packages. Nitrogen purge is also recommended during reflow.

The most common surface finishes that are compatible with lead-free surface mount technology (SMT) process are:

- Organic solderability preservatives (OSP)
- Electroless nickel/Immersion gold (ENIG)

- Immersion silver
- Immersion gold

Selection of a suitable finish will depend on end users' requirements for board design, assembly process, handling/storage, and cost.

6.2.2.2 PCB Materials

Due to the higher reflow temperature requirement of the lead-free material set, the board material with higher glass transition temperature T_g ($> 170^\circ\text{C}$) is recommended.

6.2.3 SMT Printing

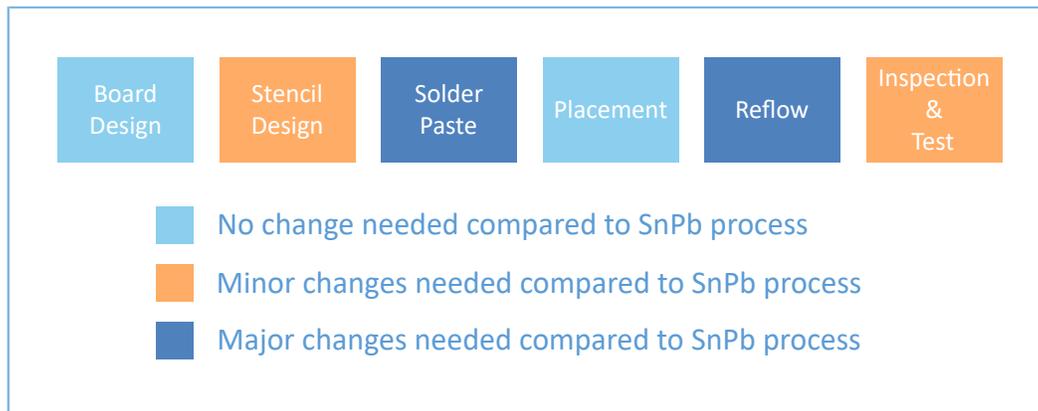


Figure 6-4 SMT printing process

- **Solder Paste**
Sn-Ag-Cu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance.
- **Stencil Design**
The recommended stencil is laser-cut, stainless-steel type with thickness of 5 to 7 mils and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 1 mil larger than the top can be utilized. Sn-Ag-Cu solder does not wet as well as Sn-Pb solder.
- **Printing Process**
The printing process requires no significant changes, comparing with that applies Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste deposition.
- **Placement**
With the self-aligning characteristic of the QFN packages during reflow, the placement accuracy is $< 30\%$ of the pad width or as long as the solder pads can touch solder paste.

6.3 SMT Reflow Process

The optimization of the reflow process is the most critical factor to be considered for the lead-free soldering. The development of an optimal profile should take into account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensure successful lead-free assembly, high yield and long-term solder joint reliability.

1. Temperature profiling

Temperature profiling should be performed for all new board designs by attaching thermocouples at the solder joints of QFN packages, on the top surface of the larger components as well as at multiple locations of the boards. This is to ensure that all components are heated to temperature above the minimum reflow temperatures and the smaller components do not exceed maximum temperature limit.

For larger or sophisticated boards with a large number of components, it is also important to minimize the temperature difference across the board to be less than 10 degrees to minimize board warp. Maximum temperature at component body should not exceed the MSL3 qualification specification.

2. Reflow profile guideline

The solder reflow profile should follow the recommendation from paste manufacturers and general standards such as JEDEC/IPC J-STD-20. Figure 6-5 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 6-5.

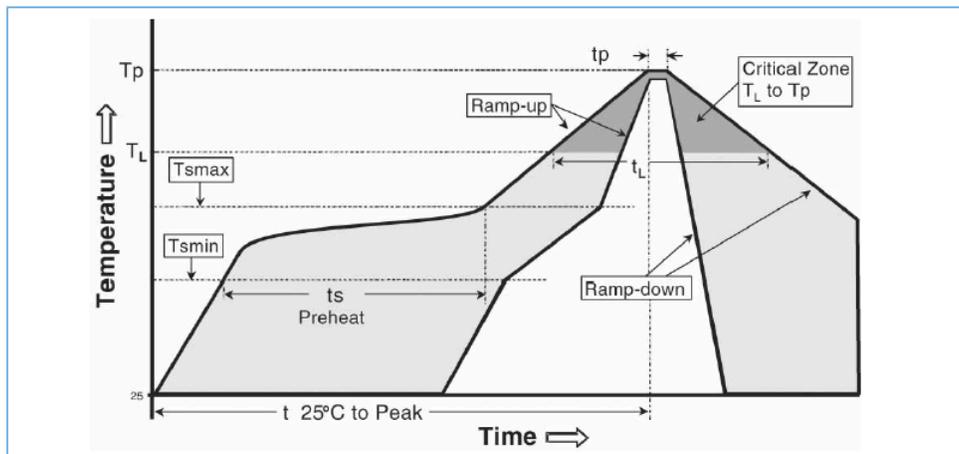


Figure 6-5 JEDEC recommended lead-free reflow profile

The GR533x fulfills the lead-free soldering requirements from IPC/JEDEC, i.e. reflow soldering with a peak temperature up to 260°C.

The lead frame is made of CuAg and has Matte Sn plating. This is 100% Sn and thus Pb-free. Plating thickness is 300 – 600 μin. The Matte Sn CuAg LF can withstand 3x reflow at 260°C.

Table 6-5 Reflow profile parameters

Profile Parameters	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate (T _{max} to T _p)	3°C/second (max)

Profile Parameters	Lead-Free Assembly, Convection, IR/Convection
Preheat temperature (T _{sm} to T _{smax})	150°C – 200°C
Preheat time (t _s)	60 seconds – 180 seconds
Time above TBL, 217°C (T _L)	60 seconds – 150 seconds
Time within 5°C of peak temperature (T _p)	20 seconds – 40 seconds
Ramp-down rate	6°C/second (max)
Time 25°C to peak temperature	8 minutes (max)

Note:

All specified temperatures in Table 6-5 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 6-5 to prevent thermal damage to the package. An example of reflow profile is shown in Figure 6-6.

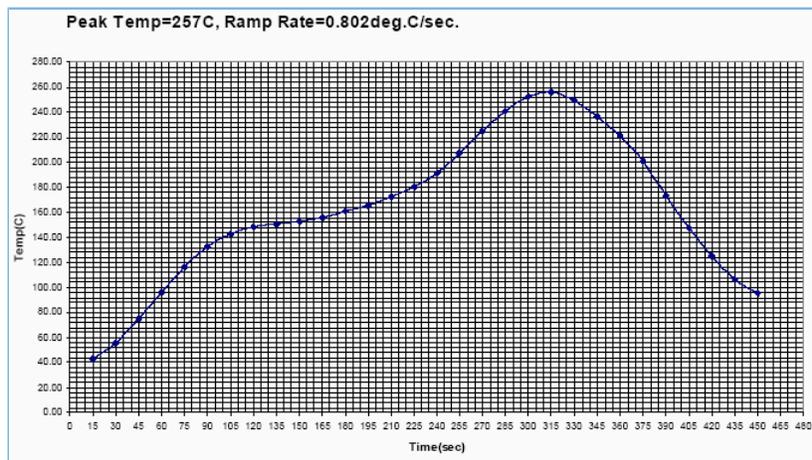


Figure 6-6 Reflow profile example with 257°C peak temperature

3. Reflow oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. An oven with more heating zones offers higher flexibility to optimize the reflow profile for complex and/or larger boards. Nitrogen atmosphere can improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

6.4 Rework Guideline

Because solder joints are not fully exposed for QFN packages, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of QFN packages can be a challenge due to their small size.

In most applications, QFN packages will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Because reflow of adjacent parts is not desirable during rework, the

proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for QFN packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste printing
4. Component placement
5. Component attachment

 **Note:**

Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

6.4.1 Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally, the reflow profile for part removal should be the same as the one used for part attachment. However, the time above the liquidus state can be reduced as long as the reflow is complete.

 **Note:**

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and heated on the top side using hot gas or air.

Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided because this may cause chip scale package (CSP) to skew. Air velocity of 15 – 20 liters per minute is a good starting point. Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cool down.

Because of the small size of GR533x SoCs, the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad lift-off.

6.4.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and de-soldering braid. The width of the blade should match to the maximum width of the footprint and the blade temperature should be low enough to prevent any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.

6.4.3 Solder Paste Printing

Because of their small size and finer pitches, solder paste deposition for QFN packages requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100x magnification.

The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side. A 125 microns thick stencil with aperture size and shape same as the package land should be used.

In addition, no-clean flux should be used, because small standoff of QFN packages does not leave much room for cleaning.

6.4.4 Component Placement

QFN packages are expected to have superior self-centering ability due to their small mass. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The alignment should also be done at 50 to 100x magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

6.4.5 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Because all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

6.5 RoHS Compliant

GR533x is RoHS compliant, as per Directive 2002/95/EC and its subsequent amendments.

6.6 SVHC Materials (REACH)

GR533x is compliant with Substance of Very High Concern (SVHC) list based on the publication by European Chemicals Agency (ECHA) on October 28, 2008 Regulation (EC) No 1907/2006 concerning *Registration, Evaluation, Authorisation and Restriction of Chemicals (REACH)*.

6.7 Halogen Free

GR533x is compliant with BS EN 14582: 2007 in regards to halogens: fluorine, chlorine, bromine, and iodine content.