GR533x RF PA Application Note

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Preface

Purpose

This document introduces the GR533x radio frequency (RF) power amplifier (PA) application design, including PA selection, matching circuit design, and application configuration, to help users quickly get started with GR533x RF application circuits.

Audience

This document is intended for:

- Device user
- Developer
- Test engineer
- Technical support engineer

Release Notes

This document is the third release of *GR533x RF PA Application Note*, corresponding to GR533x System-on-Chip (SoC) series.

Revision History

Version	Date	Description
1.0	2023-10-18	Initial release
1.1	2023-11-08	Updated the RF PA application configuration.
1.2	2024-01-16	• Updated the C4 capacitance in GR5331 SPA/UPA seven-component matching circuit. • Added FCC harmonic suppression method for GR5331 SPA.

Contents

1 GR533x RF Transceiver

The GR533x System-on-Chip (SoC) integrates a 2.4 GHz radio frequency (RF) transceiver with excellent RF performance. It allows users to select an appropriate power amplifier (PA) according to specific part number, providing users with flexible choices to meet different TX power application requirements.

This chapter depicts the system block diagram and the operating mechanism of GR5332 and GR5331 transceivers.

1.1 GR5332 RF Transceiver

The system block diagram of a GR5332 RF transceiver is shown as follows:

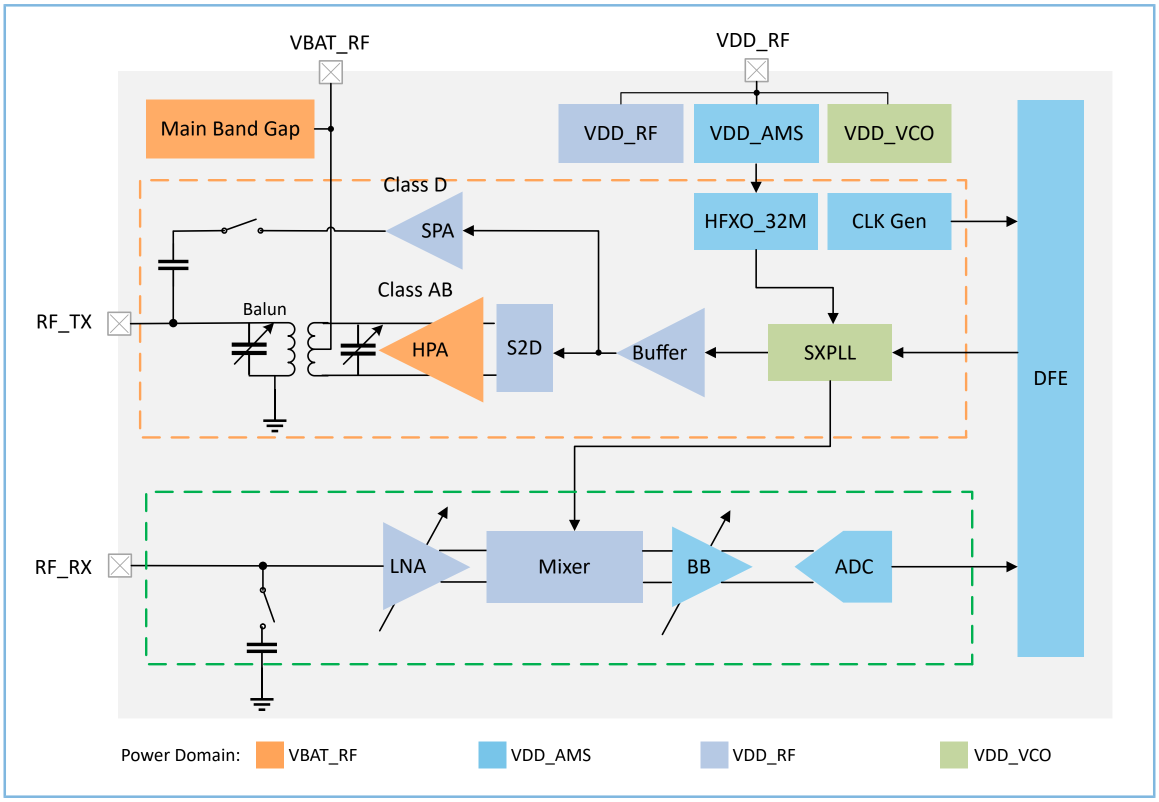

Figure 1-1 Block diagram of GR5332 RF transceiver

- On the receiver side:
  1. After the antenna receives an RF signal, the receiver digitizes the signal in a path: Low noise amplifier (LNA) > Mixer > Baseband (BB) amplifier > analog-to-digital converter (ADC).
  2. The digitized signals are sent to the digital frontend (DFE) for demodulation.
  3. The digital frontend provides Automatic Gain Control (AGC) feedback signals to adjust the gain of the LNA and BB amplifier to maximize the signal-to-noise ratio (SNR) at the demodulation.
- On the transmitter side:
  1. The digital signal from the DFE is transmitted to a simplex phase-locked loop (SXPLL) for Gaussian Frequency Shift Keying (GFSK) modulation.

2. The modulated carrier wave is delivered to a PA (HPA or SPA) through buffer for power amplification, with amplification factor configurable by the digital gain settings.

3. The modulated carrier wave after power amplification is transmitted to the antenna, which then radiates the amplified carrier wave through electromagnetic waves.

Note:

- If an HPA is adopted, the modulated carrier wave needs a single-ended to differential (S2D) conversion before power amplification.
- The SXPLL reference clock is provided by the external 32 MHz crystal oscillator.

- Power supply
  - The main band gap and HPA in the GR5332 SoC are supplied by VBAT_RF.
  - VDD_RF is the RF input power supply, which powers the VDD_RF, VDD_AMS, and VDD_VCO modules. VDD_RF supplies the RF analog circuits, VDD_AMS supplies the clock module and the receiver baseband module, and VDD_VCO supplies SXPLL.

1.2 GR5331 RF Transceiver

The system block diagram of a GR5331 RF transceiver is shown as follows:

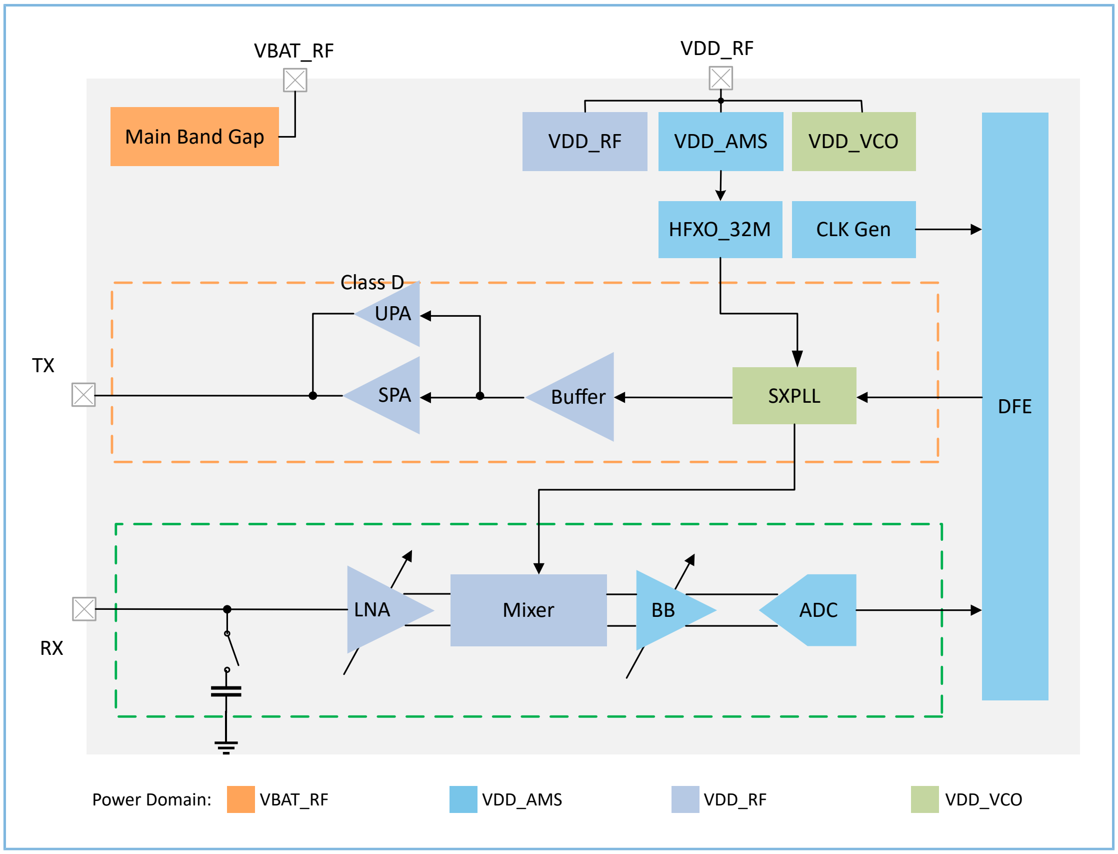

Figure 1-2 Block diagram of GR5331 RF transceiver

The GR5331 RF transceiver is almost the same as that of GR5332, with the only difference that SPA or UPA is adopted in the GR5331 transmitter and UPA contributes to lower power consumption.

2 Introduction to GR533x RF PA

This chapter illustrates the features of GR533x RF PA, to help users select an appropriate one.

Different types of RF PA are suitable for different GR533x SoCs, as shown in the following table:

Table 2-1 RF PAs for GR533x SoCs

PA Type	**SoC Series**	
	GR5331	**GR5332**
HPA	/	√
SPA	√	√
UPA	√	/

Tip:

"√" indicates compatibility, and "/" indicates incompatibility.

2.1 HPA

The High Power Amplifier (HPA) is applicable to GR5332 SoCs only, with the following main features:

Table 2-2 HPA features

GR533x Series	**TX Output Power**	**Power Mode**	**PA Class**	**Quantity of Matching Components**
GR5332	–10 dBm to 15 dBm	SYS_LDO	Class AB	6

Tip:

- GR5332 VBAT_RF supplies the HPA. To ensure optimal RF PHY performance, a 4.7 µF decoupling capacitor should be connected to the VBAT_RF pin. For FCC harmonic suppression, an additional 3.9 pF capacitor needs to be connected in parallel. Moreover, ensure that this pF capacitor is placed near the VBAT_RF pin during PCB layout.
- When an HPA is adopted in applications, the system power mode must be switched to SYS_LDO. If supplied by DC-DC, the HPA cannot be driven for proper operation.

2.2 SPA

The Small Power Amplifier (SPA) is applicable to GR533x SoCs, with the following main features:

Table 2-3 SPA features

GR533x Series	**TX Output Power**	**Power Mode**	**PA Class**	**Quantity of Matching Components**
GR5332	–20 dBm to 5 dBm	SYS_LDO/DC-DC	Class D	6
GR5331	–20 dBm to 6 dBm	SYS_LDO/DC-DC	Class D	7

Tip:

- When an SPA is adopted in applications, the system power mode can be either SYS_LDO or DC-DC. If the system is supplied only by SYS_LDO, it can reduce the DC-DC inductor BOM, but will increase power consumption. For detailed power consumption differences, refer to "Radio Current Consumption" in *GR533x Datasheet*.
- For FCC harmonic suppression of GR5331 SPA, it is necessary to connect a 2.0 pF capacitor to the VBAT_RF pin. Additionally, place this pF capacitor as close to the VBAT_RF pin as possible during PCB layout.

2.3 UPA

The Ultra-low Power Amplifier (UPA) is applicable to GR5331 SoCs only, with the following main features:

Table 2-4 UPA features

GR533x Series	TX Output Power	Power Mode	Supply Voltage	PA Class	Quantity of Matching Components
GR5331	–15 dBm to 2 dBm	SYS_LDO/DC-DC	VDD_RF ≤ 1.2 V Typ.: 1.05 V	Class D	4

Tip:

In applications where the TX output power is 0 dBm, it is recommended to use UPA for achieving lower power consumption.

3 GR533x RF PA Matching Circuit

This chapter details GR533x RF PA matching circuits, including reference schematic diagrams and recommended BOMs.

3.1 GR5332 RF PA Matching Circuit

3.1.1 HPA/SPA Six-component Matching Circuit

When an HPA or SPA is adopted for GR5332 SoCs, the same matching parameters can be used. The six-component matching circuit consisting of three inductors and three capacitors is recommended for GR5332 RF PA, and the reference schematic diagram is shown as follows:

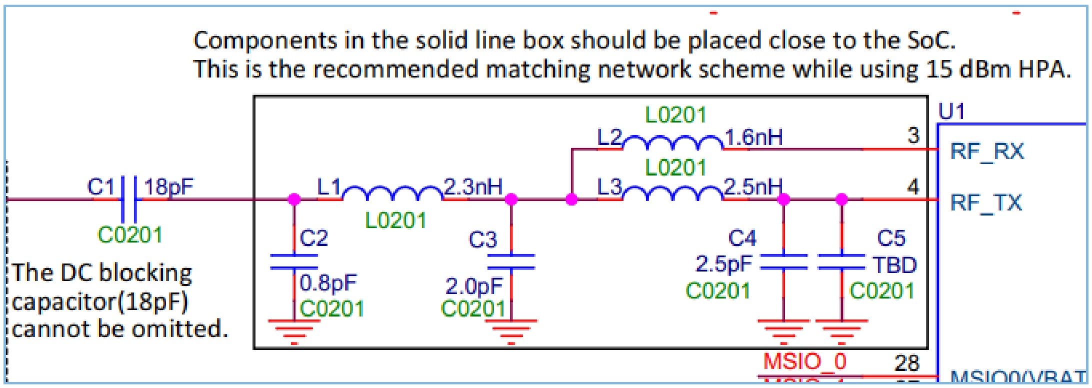

Figure 3-1 Six-component matching circuit for GR5332 SoCs

The recommended matching components are as below:

Table 3-1 Recommended matching components (inductors and capacitors)

Symbol	Description	Value	Package (Imperial)	Manufacturer/Model
C1	CAP, CER, 18 pF, +/–5%, NPO, 0201, 50 V, –55°C to +125°C	18 pF	0201	Murata GRM0335C1H180JA01
C2	CAP, CER, 0.8 pF, +/–0.05 pF, NPO, 0201, 50 V, –55°C to +125°C	0.8 pF	0201	Murata GRM0335C1HR80WA01
C3	CAP, CER, 2.0 pF, +/–0.1 pF, NPO, 0201, 50 V, –55°C to +125°C	2.0 pF	0201	Murata GRM0335C1H2R0BA01
C4	CAP, CER, 2.5 pF, +/–0.1 pF, NPO, 0201, 50 V, –55°C to +125°C	2.5 pF	0201	Murata GRM0335C1H2R5BA01
L1	Inductor, CHIP, 2.3 nH, ±0.1 nH, 200 mohms, Q = 14@ 250 MHz, –55°C to +125°C, 0201	2.3 nH	0201	Murata LQP03TN2N3B02
L2	Inductor, CHIP, 1.6 nH, ±0.1 nH, 150 mohms, Q = 14@ 250 MHz, –55°C to +125°C, 0201	1.6 nH	0201	Murata LQP03TN1N6B02

Symbol	Description	Value	Package (Imperial)	Manufacturer/Model
L3	Inductor, CHIP, 2.5 nH, ±0.1 nH, 200 mohms, Q = 14@ 250 MHz, –55°C to +125°C, 0201	2.5 nH	0201	Murata LQP03TN2N5B02

Note:

C1 (18 pF) is a blocking capacitor and cannot be omitted. It is used to connect to the antenna matching network and the RF PA matching network.

With the above mentioned six-component matching circuit, the GR5332 RF performance parameters are as follows:

Table 3-2 GR5332 RF performance parameters

PA Type	Power Mode	TX Output Power (Typ.)	RX Sensitivity (Typ.)	TX Current Consumption (mA) @ VBAT 3.3 V	RX Current Consumption (mA) @ VBAT 3.3 V	Conducted Harmonics
HPA	SYS_LDO = 1.15 V	15 dBm	–99 dBm	95 @15 dBm TX output power	12	≤ –40 dBm
SPA	DC-DC = 1.15 V	5 dBm	–98.5 dBm	10.9 @ 5 dBm TX output power	4.9	≤ –40 dBm
SPA	DC-DC = 1.05 V	4 dBm	–98.5 dBm	7.7 @ 4 dBm TX output power	4.9	≤ –40 dBm

Tip:

- Compared to the DC-DC power mode, the full-band RX sensitivity can be improved by 0.5 dBm to 1 dBm when SYS_LDO is adopted.
- When SPA and DC-DC power mode are used, increasing the DC-DC voltage from 1.05 V to 1.15 V will increase the typical output power of SPA by 1 dBm.

3.2 GR5331 RF PA Matching Circuit

3.2.1 SPA/UPA Seven-component Matching Circuit

When an SPA or UPA is adopted for GR5331 SoCs, the same matching parameters can be used. The seven-component matching circuit consisting of three inductors and four capacitors is recommended for GR5331 RF PA, and the reference schematic diagram is shown as follows:

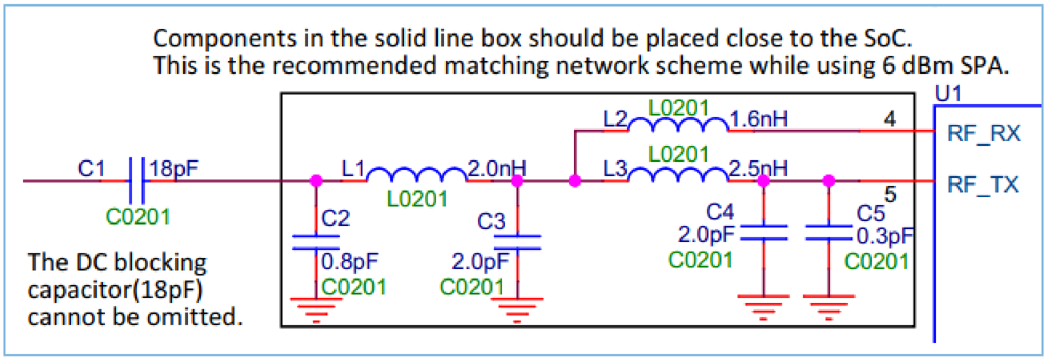

Figure 3-2 Seven-component matching circuit for GR5331 SoCs

The recommended matching components are as below:

Table 3-3 Recommended matching components (inductors and capacitors)

Symbol	Description	Value	Package (Imperial)	Manufacturer/Model
C1	CAP, CER, 18 pF, +/–5%, NPO, 0201, 50 V, –55°C to +125°C	18 pF	0201	Murata GRM0335C1H180JA01
C2	CAP, CER, 0.8 pF, +/–0.05 pF, NPO, 0201, 50 V, –55°C to +125°C	0.8 pF	0201	Murata GRM0335C1HR80WA01
C3, C4	CAP, CER, 2.0 pF, +/–0.1 pF, NPO, 0201, 50V, –55°C to +125°C	2.0 pF	0201	Murata GRM0335C1H2R0BA01
C5	CAP, CER, 0.3 pF, +/–0.05 pF, NPO, 0201, 50 V, –55°C to +125°C	0.3 pF	0201	Murata GRM0335C1HR30WA01
L1	Inductor, CHIP, 2.0 nH, ±0.1 nH, 200 mohms, Q = 14@ 250 MHz, –55°C to +125°C, 0201	2.0 nH	0201	Murata LQP03TN2N0B02
L2	Inductor, CHIP, 1.6 nH, ±0.1 nH, 150 mohms, Q = 14@ 250 MHz, –55°C to +125°C, 0201	1.6 nH	0201	Murata LQP03TN1N6B02
L3	Inductor, CHIP, 2.5 nH, ±0.1 nH, 200 mohms, Q = 14@ 250 MHz, –55°C to +125°C, 0201	2.5 nH	0201	Murata LQP03TN2N5B02

Note:

C1 (18 pF) is a blocking capacitor and cannot be omitted. It is used to connect to the antenna matching network and the RF PA matching network.

With the above mentioned seven-component matching circuit, the GR5331 RF performance parameters are as follows:

Table 3-4 GR5331 RF performance parameters

PA Type	Power Mode	TX Output Power (Typ.)	RX Sensitivity (Typ.)	TX Current Consumption (mA) @ VBAT 3.3 V	RX Current Consumption (mA) @ VBAT 3.3 V	Conducted Harmonics
SPA	DC-DC = 1.15 V	6 dBm	–97.5 dBm	9.7 @ 6 dBm TX output power	5.0	≤ –40 dBm
SPA	DC-DC = 1.05 V	5 dBm	–97.5 dBm	7.9 @ 5 dBm TX output power	5.0	≤ –40 dBm
UPA	DC-DC = 1.05 V	2 dBm	–97.5 dBm	4.6 @ 0 dBm TX output power	5.0	≤ –40 dBm

3.2.2 UPA Four-component Matching Circuit

In applications with TX output power of 0 dBm, a UPA is recommended for GR5331 SoCs, and the four-component matching circuit consisting of two inductors and two capacitors is recommended for GR5331 RF PA to achieve lower power consumption. The reference schematic diagram is shown as follows:

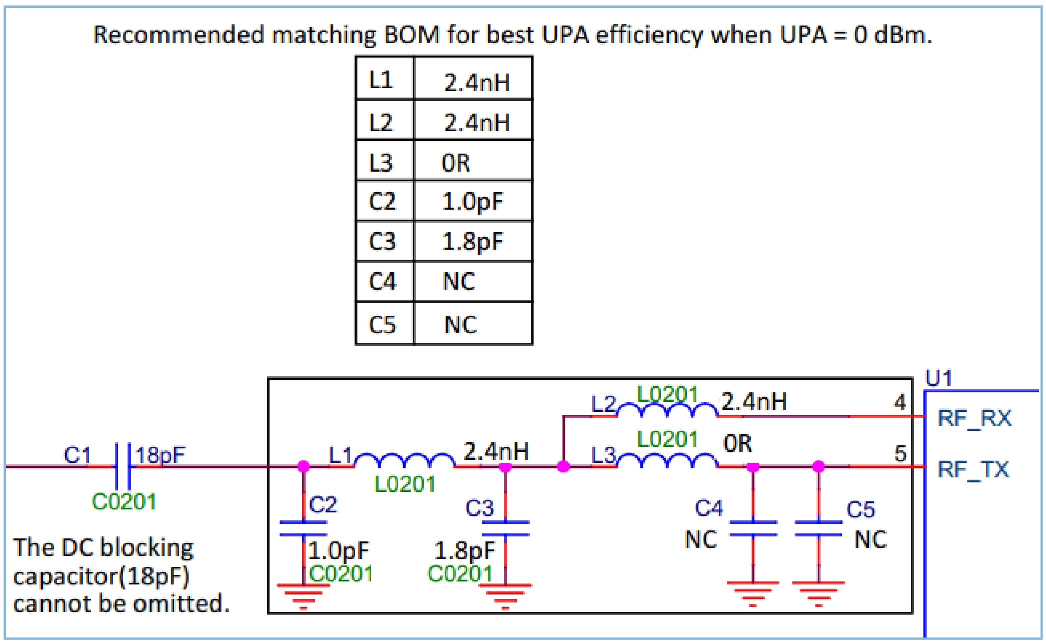

Figure 3-3 Four-component matching circuit for GR5331 SoCs

The recommended matching components are as below:

Table 3-5 Recommended matching components (inductors and capacitors)

Symbol	Description	Value	Package (Imperial)	Manufacturer/Model
C1	CAP, CER, 18 pF, +/–5%, NPO, 0201, 50 V, –55°C to +125°C	18 pF	0201	Murata GRM0335C1H180JA01

Symbol	Description	Value	Package (Imperial)	Manufacturer/Model
C2	CAP, CER, 0.8 pF, +/–0.1 pF, NPO, 0201, 50 V, –55°C to +125°C	1.0 pF	0201	Murata GRM0335C1H1R0BA01
C3	CAP, CER, 2.0 pF, +/–0.1 pF, NPO, 0201, 50V, –55°C to +125°C	1.8 pF	0201	Murata GRM0335C1H1R8BA01
L1/L2	Inductor, CHIP, 2.4 nH, +/–0.1 nH, 200 mohms, Q = 14@250 MHz, –55°C to +125°C, 0201	2.4 nH	0201	Murata LQP03TN2N4B02

Note:

C1 (18 pF) is a blocking capacitor and cannot be omitted. It is used to connect to the antenna matching network and the RF PA matching network.

With the above mentioned four-component matching circuit, the GR5331 RF performance parameters are as follows:

Table 3-6 GR5331 RF performance parameters

PA Type	Power Mode	TX Output Power (Typ.)	RX Sensitivity (Typ.)	TX Current Consumption (mA) @ VBAT 3.3 V	RX Current Consumption (mA) @ VBAT 3.3 V	Conducted Harmonics
UPA	DC-DC = 1.05 V	2 dBm	–97.5 dBm	4.2 @ 0 dBm TX output power	5.0	≤ –40 dBm

4 GR533x RF PA Application Configuration

This chapter illustrates the application scenarios and software configuration of GR533x RF PA.

4.1 Application Scenarios

Different RF PA matching circuit parameters can be used for GR533x SoCs in different application scenarios, to achieve a perfect balance between performance and power consumption.

Table 4-1 GR533x RF PA application scenarios

Max. Power in Applications	15 dBm	6 dBm	2 dBm
SoC Series	GR5332	GR5331	GR5331
PA Type	HPA	SPA	UPA
Quantity of Matching Components	6	7	4

4.2 Software Configuration

When using the GR533x RF PA, you need to configure relevant parameters in the application project according to application needs, including SoC series, PA type, and power mode.

Table 4-2 Application project configuration parameters

PA Type	HPA	SPA		UPA
SoC Series	GR5332	GR5332/GR5331		GR5331
Power Mode	SYS_LDO	DC-DC/SYS_LDO		DC-DC/SYS_LDO
Supply Voltage (V)	1.15	1.05	1.15	1.05
Power Range (dBm)	[–10, 15]	GR5332: [–20, 4] GR5331: [–20, 5]	GR5332: [–20, 5] GR5331: [–20, 6]	[–15, 2]

Tip:

You can configure related parameters in custom_config.h of the application project.

4.2.1 SoC Series Configuration

Configure the CHIP_TYPE macro according to the specific SoC in use.

```
// <o> Chip version
#ifndef SOC_GR533X
#define SOC_GR533X
#endif
// <o> Select chip type
// <0=> GR5330ACNI
// <1=> GR5331AENI
// <2=> GR5331CENI
// <3=> GR5332AENE
```



```
// <4=> GR5332CENE
#ifndef CHIP_TYPE
#define CHIP_TYPE                        2
#endif
```

4.2.2 PA Configuration

Select an appropriate PA and configure the RF_TX_PA_SELECT macro according to the TX output power requirements in applications.

```
// <o> RF TX PA select
// <1=> BLE_RF_TX_MODE_SPA_MODE  (-20~6 dBm TX power for GR5331/GR5330, -20~5 dBm TX power
 for GR5332)
// <2=> BLE_RF_TX_MODE_UPA_MODE  (-15~2 dBm TX power for GR5331/GR5330)
// <3=> BLE_RF_TX_MODE_HPA_MODE  (-10~15 dBm TX power for GR5332)
#ifndef RF_TX_PA_SELECT
#define RF_TX_PA_SELECT                  1
#endif
```

4.2.3 System Power Configuration

Configure the SYSTEM_POWER_MODE macro according to the specific system power mode in use.

```
// <ol.0..2> System power mode
// <0=> DCDC MODE
// <1=> SYSLDO MODE
#ifndef SYSTEM_POWER_MODE
#define SYSTEM_POWER_MODE                0
#endif
```

Tip:

When an HPA is adopted in applications, the system power mode must be switched to SYS_LDO.

