GR5515I0NDA Flash Selection Guide

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Preface

Purpose

This document introduces the electrical characteristics and functional requirements of external Flash memories of GR5515I0NDA. It also lists configuration considerations and FAQ for GR5515I0NDA Flash, aiming to help users quickly choose suitable external Flash memories when developing Bluetooth products based on GR5515I0NDA.

Audience

This document is intended for:

- GR551x user
- GR551x developer
- GR551x tester
- Hobbyist developer

Release Notes

This document is the fourth release of *GR5515I0NDA Flash Selection Guide*, corresponding to GR5515I0NDA.

Revision History

Version	Date	Description
1.0	2021-01-07	Initial release
1.1	2021-06-30	• Added "Configuration Considerations" and "FAQ". • Updated "Recommended GR5515I0ND Flash Candidates".
1.2	2021-09-06	Introduced GR5515I0NDA.
1.3	2023-01-19	Deleted the GR5515I0ND SoC.

Contents

1 Introduction

In GR551x System-on-Chip (SoC) series, GR5515I0NDA requires external Flash memories. The Flash functionalities and usage vary depending on Flash manufacturer and model. This document depicts the electrical characteristics and functional requirements of GR5515I0NDA external Flash memories, providing a reference for users in selecting external Flash memories.

Table 1-1 lists pins connecting GR5515I0NDA to external Flash.

Table 1-1 Pins connecting GR5515I0NDA to external Flash

GR5515I0NDA GPIO Pin	External Flash QSPI Pin
GPIO_18	QSPI_CS_N
GPIO_19	QSPI_IO_3
GPIO_20	QSPI_CLK
GPIO_21	QSPI_IO_2
GPIO_22	QSPI_IO_1
GPIO_23	QSPI_IO_0

The figure below shows a pin connection diagram for GR5515I0NDA and external Flash memories connected via QSPI pins.

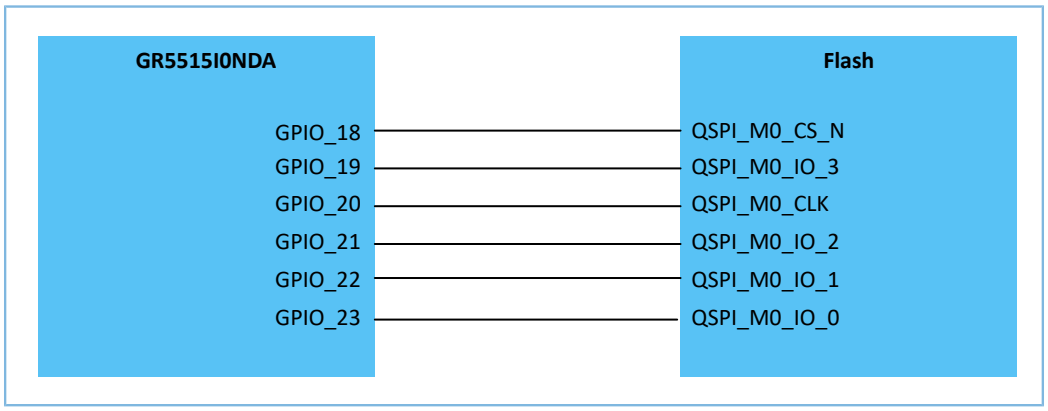

Figure 1-1 QSPI pin connection between GR5515I0NDA and external Flash

2 Electrical Characteristics

2.1 General Electrical Characteristics

The table below presents general electrical characteristics of GR5515I0NDA Flash.

Table 2-1 General electrical characteristics of GR5515I0NDA Flash

Parameter	Min.	Typ.	Max.	Unit
Operating voltage	1.7	3.3	3.6	V
Operating temperature	–40	-	85	°C
Storage temperature	–65	-	150	°C
Memory size	256	-	-	KB

2.2 AC Characteristics

The table below contains AC characteristics of GR5515I0NDA Flash.

Table 2-2 AC characteristics of GR5515I0NDA Flash

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	VDDIO x 0.7	-	VDDIO	V
V_{IL}	Input low voltage	VSSIO	-	VDDIO x 0.3	V
$V_{OH,H}$	Output high voltage @ 2.5 mA, VDD ≥ 3 V	VDDIO – 0.4	-	VDDIO	V
$V_{OL,H}$	Output low voltage @ 2.5 mA, VDD ≥ 3 V	VSSIO	-	VSS + 0.4	V
f_{sck}	Clock frequency	64	-	-	MHz
t_{CH}	Serial clock high time	4.5	-	-	ns
t_{CL}	Serial clock low time	4.5	-	-	ns
t_{CLCH}	Clock rising time (valley to peak)	0.1	-	-	V/ns
t_{CHCL}	Clock falling time (peak to valley)	0.1	-	-	V/ns
t_{DVCH}	Data in setup time	2	-	-	ns
t_{CHDX}	Data in hold time	3	-	-	ns
t_{SLCH}	Chip select to clock active setup time	5	-	-	ns
$T_{clqv(TV)}$	Clock low to output valid time @ loading 30 pF	-	-	7	ns
C_{in}	Pin input capacitance @ VIN = 0	-	-	6	pF
C_{out}	Pin output capacitance @ VIN = 0	-	-	8	pF
Temperature	Operating temperature	–40	-	85	°C

Figure 2-1 and Figure 2-2 show the timing for serial output and input of Flash respectively.

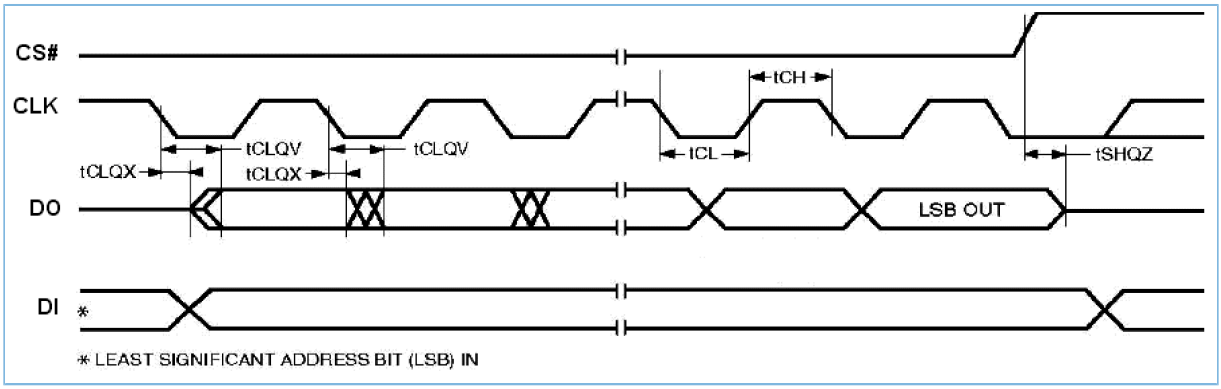

Figure 2-1 Serial output timing diagram

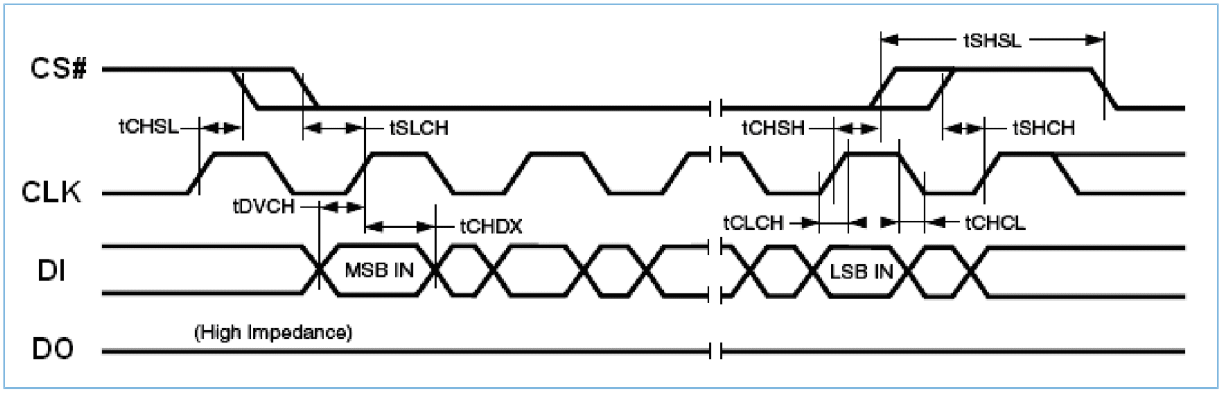

Figure 2-2 Serial input timing diagram

3 Functional Requirements

3.1 Basic Functional Requirements

The GR5515I0NDA Flash is required to support three SPI communication modes: Standard SPI, Dual SPI, and Quad SPI with a maximum transfer rate of higher than 64 MHz. The table below contains basic functional requirements of GR5515I0NDA Flash.

Table 3-1 Basic functional requirements of GR5515I0NDA Flash

Symbol	Min.	Typ.	Max.	Unit
Erase time	10	-	-	10,000
Erase duration	-	< 8	< 20	ms
Page program duration	-	< 2	< 4	ms

3.2 Command Compatibility

The GR5515I0NDA Flash candidates shall support the following commands.

Table 3-2 Commands supported by GR5515I0NDA Flash

Commands		Code
Read	Read Array (fast)	0x0B
	Read Array (low power)	0x03
	Read Dual Output	0x3B
	Read 2x I/O	0xBB
	Read Quad Output	0x6B
	Read 4x I/O	0xEB
Program and Erase	Sector Erase (4 Kbytes)	0x20
	Chip Erase	0x60
	Page Program	0x02
	Program/Erase Suspend	0x75
	Program/Erase Resume	0x7A
Status Register	Read Status Register	0x05
	Read Status Register 1	0x35
	Write Status Register	0x01
Others	Reset Enable	0x66
	Reset	0x99
	Read Manufacturer/Device ID	0x9F
	Deep Power-down	0xB9

Commands		Code
	Release Deep Power-down/Read Electronic ID	0xAB

4 Recommended GR5515I0NDA Flash Candidates

GR5515I0NDA supports both low-voltage (typical: 1.8 V) and high-voltage (typical: 3.3 V) Flash. According to the previous electrical characteristics and functional requirements, Goodix recommends the following GR5515I0NDA Flash candidates. GR5515I0NDA applies to both Table 4-1 and Table 4-2.

Table 4-1 Recommended GR5515I0NDA Flash candidates (high voltage)

Flash Model	Manufacturer	Flash Size	Voltage Range (V)
P25Q128H	Puya Semiconductor	128 Mb	2.30–3.60
W25Q64JV	Winbond	64 Mb	2.70–3.60
XM25QH64A	XMC	64 Mb	2.30–3.60
XT25F64B	XTX	64 Mb	2.70–3.60

Table 4-2 Recommended GR5515I0NDA Flash candidates (low voltage)

Flash Model	Manufacturer	Flash Size	Voltage Range (V)
P25Q128L	Puya Semiconductor	128 Mb	1.65–2.00
XT25Q64D	XTX	64 Mb	1.65–2.10

Note:

- GR551x SDK V1.6.11 and later versions support low-voltage Flash memories (typical: 1.8 V). For GR5515I0NDA equipped with high-voltage external Flash, you should utilize GRPLT, a test tool in the production line, to complete eFuse configurations.
- Flash memories vary in access speeds. For Flash memories that cannot support data reads at 64 MHz, decrease the QSPI communications rate according to the specific Flash access speeds.

5 Configuration Considerations

5.1 Configuring tRES1

tRES1, representing the time when users should wait for a Flash memory switching from Deep Power-down Mode to Stand-by Mode. The tRES1 values vary among Flash memory models; therefore, users should modify the EXFLASH_WAKEUP_DELAY macro in *custom_config.h* based on the tRES1 of the specific Flash memory you choose. This ensures that tRES1 meets different requirements of Flash operation timing under diverse conditions. An incorrect tRES1 value may lead to internal Flash data error.

5.2 Enabling QSPI Mode

The method to enable QSPI mode varies depending on Flash memory models. The method applicable to recommended Flash memories listed in Table 4-1 and Table 4-2 may be incompatible with Flash memories beyond the table.

Bit 9 in status register serves as the default QE bit (QSPI enable control bit) for a GR5515I0NDA Flash. In scenarios when QE bit is not set to bit 9, users should implement QE bit enable code on their own to enable QSPI mode.

For details, see "Section 5.3 Implementing Special Flash Operation Commands". In addition, you should re-implement the weak function, hal_status_t platform_exflash_enable_quad(exflash_handle_t *p_exflash). Afterwards, platform_flash_enable_quad in *platfor_gr55xx.c* will automatically call the strong function that has been implemented by users.

5.3 Implementing Special Flash Operation Commands

When users need to implement special Flash commands, pay attention to the switch between XIP and QSPI status. You can implement such commands by referring to the example code in SDK`\components\libraries\hal_flash\hal_exflash_user_operation.c`. Code execution during Flash operations is not allowed, so add the SECTION_RAM_CODE macro to the code before implementing a custom function. This ensures that the function is executed on SRAM.

6 FAQ

This chapter describes possible problems, reasons, and solutions when choosing and using a GR5515I0NDA Flash.

6.1 Why Do I Fail to Erase All Flash Data after Executing a Flash Erasing Command?

- Description

  It is impossible to erase all Flash data by executing a Flash erase command.

- Analysis

  The failure may be caused by the following reasons:

  - Unstable supply voltage
  - Interrupted data erasing

- Solution

  - For unstable supply voltage, improve relevant circuit designs.
  - For data erasing interrupted in the middle of the erasing process, perform the following:

    1. Prior to executing an erase command, disable the general interrupt; after executing the erase command, enable the general interrupt.
    2. Check whether the chosen Flash memory supports `Program/Erase Suspend` and `Program/Erase Resume` commands. If not, modify the value of the FLASH_PROTECT_PRIORITY macro to 0 in the *custom_config.h* file.

6.2 Why Does Flash Data Error Occur due to Flash Voltage or Operation Timing Mismatch?

- Description

  Flash data error occurs due to flash voltage or operation timing mismatch, resulting in GR5515I0NDA boot failures.

- Analysis

  When Flash data error occurs, the data read by GR5515I0NDA is inconsistent with that for Flash programming. This may often happen when the power-on timing or wake-up timing of the chosen Flash memory does not meet GR5515I0ND Series Flash requirements. For example, if power supply is unstable when battery is soldered on the PCB, the power-on timing may be abnormal.

- Solution

  Usually, the GR5515I0NDA is in XIP mode. You can use tools such as J-Link Commander to directly access the Flash data, and compare the data with firmware data for Flash programming to check whether the data matches with each other. If mismatch is found out, perform the following:

1. Power off the Flash only. Short-circuit all the Flash pins to ground to discharge all electricity, ensuring that the Flash is powered off and reset.
2. Power on the Flash to read the Flash data again, and check whether all the data has been restored. Successful data restoration indicates that the Flash data error is caused by voltage or operation timing mismatch. In this case, check whether the Flash supply voltage and EXFLASH_WAKEUP_DELAY value in *custom_config.h* meet the Flash operation timing requirements under different conditions.