GR551x Hardware Design Guidelines

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Preface

Purpose

This document is to present the necessary circuit required for proper operation of GR551x Bluetooth System-on-Chips (SoCs). Recommended schematic, chip interfaces, peripherals, schematic diagram, and PCB layout guidelines of the GR551x SoC family are provided.

This *Hardware Design Guidelines* intends to help system designers build minimal Bluetooth Low Energy (Bluetooth LE) hardware circuits and develop products.

Audience

This document is intended for:

- GR551x user
- GR551x tester
- Bluetooth product engineer
- Bluetooth LE system designer

Release Notes

This document is the eleventh release of *GR551x Hardware Design Guidelines*, corresponding to GR551x SoC series.

Revision History

Version	Date	Description
1.0	2019-12-08	Initial release
1.3	2020-03-16	Updated the package pinout diagrams to the top views in “Pinout”.
1.5	2020-05-30	• Updated chip model numbers and pinout diagrams, package size diagrams, and reference schematic diagrams; • Changed power supplies and RF and explained by taking a QFN56 circuit as an example; • Added “PCB Layout Reference Design”; updated “ESD Considerations”.
1.6	2020-06-30	• Updated the package layouts and data in the Appendix; • Changed the maximum supply voltage from 4.38 V to 3.8 V; changed I/O voltage from 3.6 V to 3.3 V (typical value). • Added “Solutions for Improving ESD Protection Level on Products” by introducing the hardware watchdog timer; added “Two-layer PCBs in QFN56”.
1.7	2020-08-30	Introduced the GR5515I0ND SoC: • Added “GR5515I0ND” for pinout details; • Added “External Flash” for recommended external Flash for GR5515I0ND; • Added the reference schematic for GR5515I0ND in “Reference Design”;

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Version	Date	Description
		• Added “External Flash Connection for GR5515I0ND” as reference design.
1.8	2020-11-27	Polished descriptions in "GR551x Overview" and "Pinout".
1.9	2021-03-03	• Updated description on the TEST_MODE pin; introduced the number of I/O pins in “GR551x Overview”; • Added description on PWM configuration in "I/O Pins"; • Updated the recommended Flash models for GR5515I0ND in "External Flash"; • Updated description on I/O voltage of GR5515I0ND; • Changed the previous “ESD Considerations” into “ESD Protection Design” and updated contents in this section.
2.0	2021-04-29	• Updated description on I/O voltage of GR5515I0ND in “Power Supply”. • Updated descriptions in “Power Supply Scheme”, “Power Supply”, “Clock”, “ESD Schematic Design”, “PCB Layout Design” and “Two-layer PCBs in QFN Packages”.
2.1	2021-06-15	• Added a note for classifying GR5515RGBD as NRND. • Updated the recommended Flash models for GR5515I0ND series in "External Flash".
2.2	2021-08-20	• Introduced GR5515IENDU and GR5515I0NDA and updated relevant chapters/sections (“GR551x Overview”, “Features”, “Pinout”, “Reference Schematic Diagram”, and “Package Information”) accordingly. • Changed the pins RTC_N, RTC_P, XON, and XOP to RTC_IN, RTC_OUT, XO_OUT, and XO_IN in “Pinout” and “Reference Schematic Design”. • Updated description about sleep mode in “Features”. • Updated the section “External Flash”.
2.3	2022-02-20	Introduced GR5513BENDU, a wide-voltage SoC.

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1 GR551x Overview

The Goodix GR551x family is a single-mode, low-power Bluetooth 5.1 System-on-Chip (SoC). It can be configured as a Broadcaster, an Observer, a Central, or a Peripheral and supports the combination of all the above roles, making it an ideal choice for Internet of Things (IoT) and smart wearable devices.

Based on ARM® Cortex®-M4F CPU core, the GR551x integrates Bluetooth 5.1 Protocol Stack, a 2.4 GHz RF transceiver, on-chip programmable Flash memory, RAM, and multiple peripherals.

GR551x SoCs are available in multiple packages (see Table 1-1) that meet your diverse project demands.

Table 1-1 GR551x series

GR551x Series	GR5515IGND	GR5515IENDU	GR5515I0ND	GR5515I0NDA	GR5515RGBD	GR5515GGBD	GR5513BEND	GR5513BENDU
CPU	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F
RAM	256 KB	256 KB	256 KB	256 KB	256 KB	256 KB	128 KB	128 KB
Flash	1 MB	512 KB	N/A	N/A	1 MB	1 MB	512 KB	512 KB
Package (mm)	QFN56 (7 x 7 x 0.75)	QFN56 (7 x 7 x 0.75)	QFN56 (7 x 7 x 0.75)	QFN56 (7 x 7 x 0.75)	BGA68 (5.3 x 5.3 x 0.88)	BGA55 (3.5 x 3.5 x 0.60)	QFN40 (5 x 5 x 0.75)	QFN40 (5 x 5 x 0.75)
I/O Number	39	39	39	39	39	29	22	22

Note:

- GR5515RGBD is not recommended for new designs.
- GR5515IENDU and GR5513BENDU are embedded with wide-voltage Flash, with Flash power supply from 1.65 V to 3.6 V.
- GR5515I0ND supports external high-voltage Flash (typical: 3.3 V); GR5515I0NDA supports external wide-voltage Flash (range: 1.65 V–3.6 V).

1.1 Features

- A Bluetooth Low Energy (Bluetooth LE) 5.1 transceiver integrates Controller and Host layers
  - Supported data rates: 1 Mbps, 2 Mbps, Long Range 500 kbps, Long Range 125 kbps
  - TX power: -20 dBm to +7 dBm
  - -97 dBm sensitivity (in 1 Mbps mode)
  - -93 dBm sensitivity (in 2 Mbps mode)
  - -99.5 dBm sensitivity (in Long Range 500 kbps mode)
  - -103 dBm sensitivity (in Long Range 125 kbps mode)

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- TX current: 3.05 mA @ 0 dBm, 1 Mbps
- RX current: 3.9 mA @ 1 Mbps

- ARM® Cortex®-M4F 32-bit micro-processor with floating point support
  - Maximum frequency: 64 MHz
  - Power consumption: 30 µA/MHz
- Memory
  - 256 KB RAM with retention (four 8 KB RAM blocks and seven 32 KB RAM blocks) for GR5515 series SoCs, and 128 KB RAM with retention (four 8 KB RAM blocks and three 32 KB RAM blocks) for the GR5513 SoC
  - 1 MB Flash for GR5515 series SoCs and 512 KB Flash for the GR5513 SoC (exceptions: GR5515I0ND/GR5515I0NDA requiring external QSPI Flash and GR5515IENDU requiring 512 KB embedded Flash)
- Power management
  - On-chip DC-DC Converter
  - On-chip I/O LDO to provide I/O voltage and supply external components
  - Supply voltage: 1.7 V to 3.8 V. The supply voltage of GR5515I0ND/GR5515I0NDA (when the external Flash of GR5515I0NDA supplied by high voltage) shall equal the working voltage of external QSPI Flash
  - I/O voltage: 1.8 V to 3.3 V (Typical) (for GR5515I0ND/GR5515I0NDA/GR5515IENDU/GR5513BENDU Flash using high voltage, the VIO_LDO_OUT shall be connected to VBATL in schematic circuit.)
  - OFF mode: 0.15 µA (Typical); nothing is on except VBAT, chip in reset mode
  - Ultra deep sleep mode: 0.65 µA (Typical); I/O LDO off, no memory retention; woken up by AON GPIO or AON Timer
  - Sleep mode: 1.3 µA (Typical) when I/O LDO and BOD/BOD2 turned off, lowest voltage level for memory retention, and 32 KB memory retention; woken up by AON_RTC, AON GPIO, or Bluetooth LE Event
- Peripherals
  - 2 x QSPI interfaces, up to 32 MHz
  - 2 x SPI interfaces (1 SPI Master Interface with 2 slave CS pins + 1 SPI Slave Interface), up to 32 MHz
  - 2 x I2C interfaces at 100 kHz, 400 kHz, 1 MHz, 2 MHz
  - 2 x I2S interfaces (1 I2S Master Interface + 1 I2S Slave Interface)
  - 2 x UART interfaces, one with DMA channel.
  - 13-bit ADC, up to 1 Msps, 8 channels (5 external test channels and 3 internal signal channels), supporting both single-ended and differential inputs
  - ISO 7816 interface
  - 6-channel PWM

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  - Built-in temperature and voltage sensors
  - 4 x Hardware timers
  - 1 x AON hardware timer
  - 2 watchdog timers (one for the system and one is always-on)
  - Calendar timer
  - Wake-up comparator
  - Up to 39 multiplexed GPIO pins
- Security
  - Complete secure computing engine:
    - AES 128-bit/192-bit/256-bit symmetric encryption (ECB, CBC)
    - Keyed Hash Message Authentication Code (HMAC)
    - PKC
    - TRNG
  - Comprehensive security operation mechanism:
    - Secure boot
    - Encrypted firmware runs directly from Flash
    - eFuse for encrypted key storage
    - Differentiate application data key and firmware key, supporting one data key per device/product
- Packages
  - QFN56: 7 mm x 7 mm
  - BGA68: 5.3 mm x 5.3 mm
  - BGA55: 3.5 mm x 3.5 mm
  - QFN40: 5 mm x 5 mm
- Operating temperature range: -40°C to +85°C

1.2 Block Diagram

The block diagram of GR551x is shown in the figure below.

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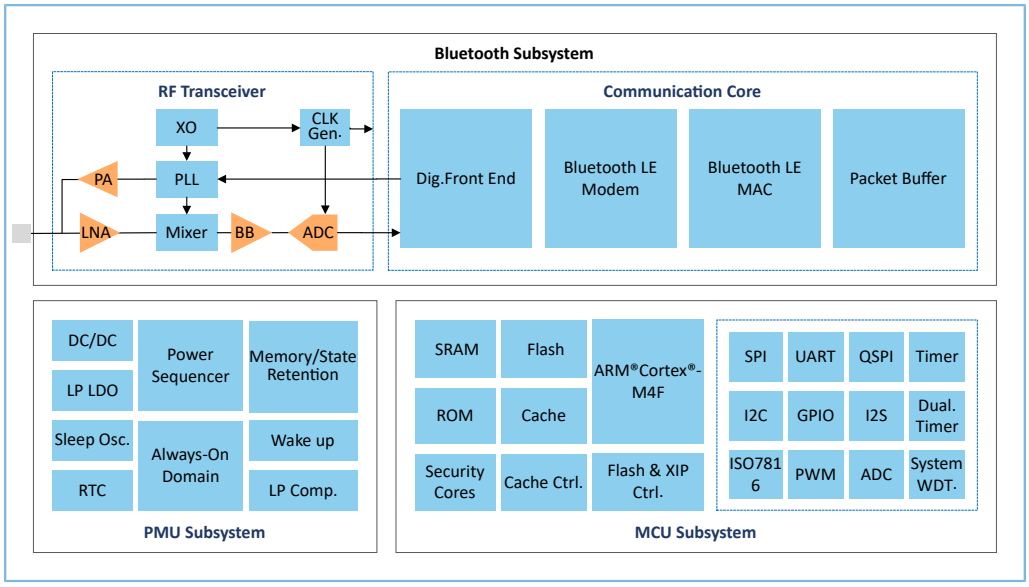


Figure 1-1 GR551x block diagram

Note:

For more details of each module in this block diagram, see *GR551x Datasheet.*

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2 Pinout

This chapter introduces GR551x pinout available in multiple packages and provides detailed descriptions.

2.1 GR5515IGND/GR5515IENDU QFN56

Figure 2-1 shows the pin assignments of GR5515IGND/GR5515IENDU QFN56 package (top view).

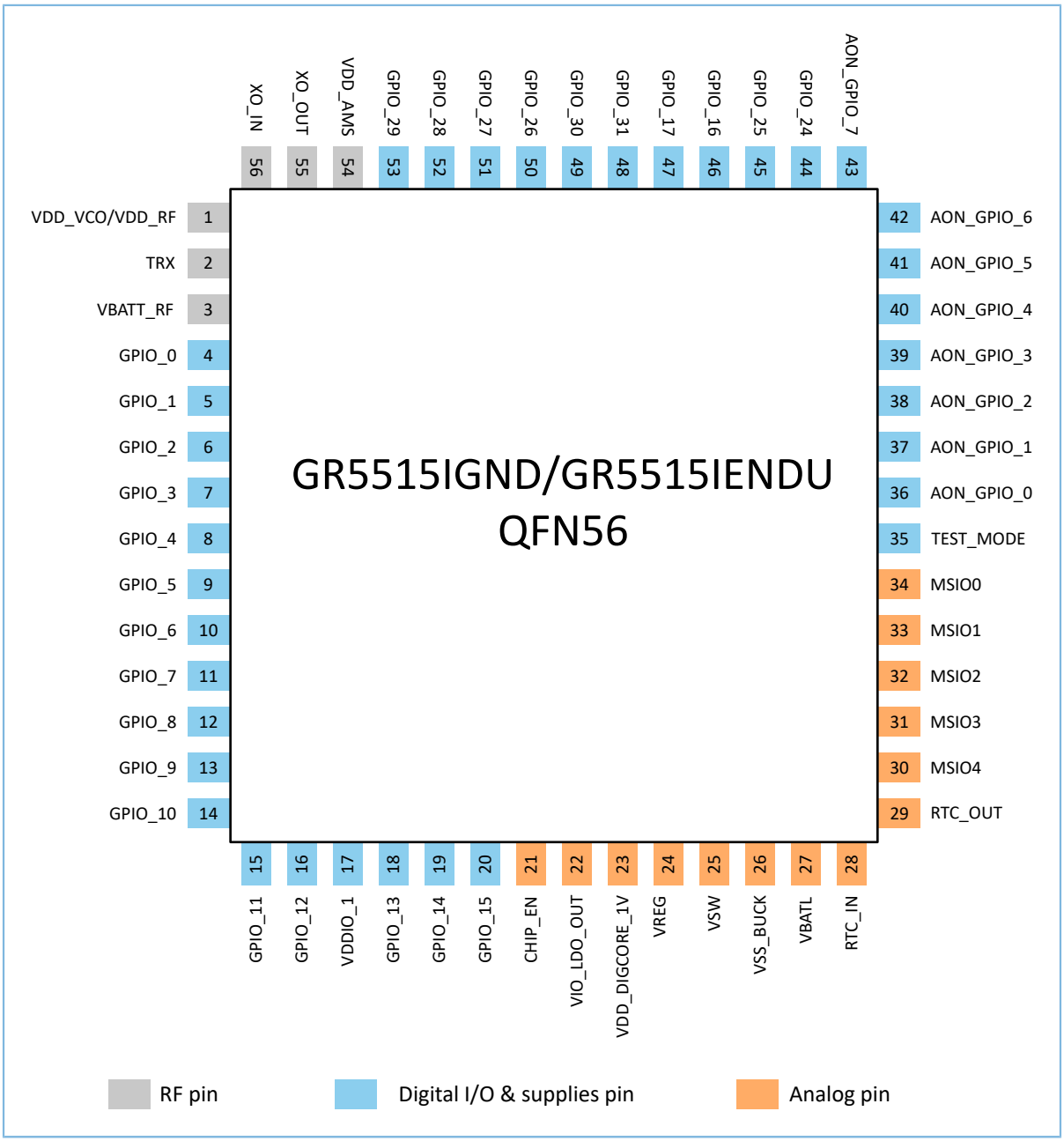


Figure 2-1 GR5515IGND/GR5515IENDU QFN56 package pinout

Table 2-1 shows pin descriptions of GR5515IGND/GR5515IENDU QFN56 package.

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Table 2-1 GR5515IGND/GR5515IENDU QFN56 pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply. RF supply. Connect to VREG.	
2	TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF Supply	Connect to VBATL.	
4	GPIO_0	Digital I/O	SWDCLK	VDDIO1
5	GPIO_1	Digital I/O	SWDIO	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O	VDDIO1
12	GPIO_8	Digital I/O	General purpose I/O	VDDIO1
13	GPIO_9	Digital I/O	General purpose I/O	VDDIO1
14	GPIO_10	Digital I/O	General purpose I/O	VDDIO1
15	GPIO_11	Digital I/O	General purpose I/O	VDDIO1
16	GPIO_12	Digital I/O	General purpose I/O	VDDIO1
17	VDDIO_1	Digital I/O supply	Digital I/O supply input	VDDIO1
18	GPIO_13	Digital I/O	General purpose I/O	VDDIO1
19	GPIO_14	Digital I/O	General purpose I/O	VDDIO1
20	GPIO_15	Digital I/O	General purpose I/O	VDDIO1
21	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. Minimum value of high level for CHIP_EN is 1 V.	
22	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator When GR5515IENDU is used and the Flash is supplied at a high voltage, the pin is used as the power input pin of VDDIO0 digital I/O domain by being connected to VBATL	Connected internally to VDDIO0
23	VDD_DIGCORE_1V	PMU	Output of on-chip LDO for digital core. Connect to a 1 µF capacitor.	
24	VREG	PMU	Feedback pin from switching regulator	
25	VSW	PMU	DC-DC converter switching node	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
26	VSS_BUCK	PMU	DC-DC converter supply and general battery GND	
27	VBATL	PMU	Power supply input	
28	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
29	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
30	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
31	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
32	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
33	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
34	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
35	TEST_MODE	Digital I/O	Input pin, used to set test mode for FT or CP factory test. In the application phase, the value is set to 0 by default. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	VDDIO0
36	AON_GPIO_0	Digital I/O	Always-on GPIO	VDDIO0
37	AON_GPIO_1	Digital I/O	Always-on GPIO	VDDIO0
38	AON_GPIO_2	Digital I/O	Always-on GPIO	VDDIO0
39	AON_GPIO_3	Digital I/O	Always-on GPIO	VDDIO0
40	AON_GPIO_4	Digital I/O	Always-on GPIO	VDDIO0
41	AON_GPIO_5	Digital I/O	Always-on GPIO	VDDIO0
42	AON_GPIO_6	Digital I/O	Always-on GPIO	VDDIO0
43	AON_GPIO_7	Digital I/O	Always-on GPIO	VDDIO0
44	GPIO_24	Digital I/O	General purpose I/O	VDDIO0
45	GPIO_25	Digital I/O	General purpose I/O	VDDIO0
46	GPIO_16	Digital I/O	General purpose I/O	VDDIO0

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
47	GPIO_17	Digital I/O	General purpose I/O	VDDIO0
48	GPIO_31	Digital I/O	General purpose I/O	VDDIO0
49	GPIO_30	Digital I/O	General purpose I/O	VDDIO0
50	GPIO_26	Digital I/O	General purpose I/O	VDDIO0
51	GPIO_27	Digital I/O	General purpose I/O	VDDIO0
52	GPIO_28	Digital I/O	General purpose I/O	VDDIO0
53	GPIO_29	Digital I/O	General purpose I/O	VDDIO0
54	VDD_AMS	Analog/RF Supply	AMS supply. Connect to VREG.	
55	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
56	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

2.2 GR5515I0ND/GR5515I0NDA QFN56

Figure 2-2 shows the pin assignments of GR5515I0ND/GR5515I0NDA QFN56 package (top view).

The pins (Pin 43 to Pin 53) of GR5515I0ND/GR5515I0NDA QFN56 package are different from those of GR5515IGND/GR5515IENDU QFN56 package.

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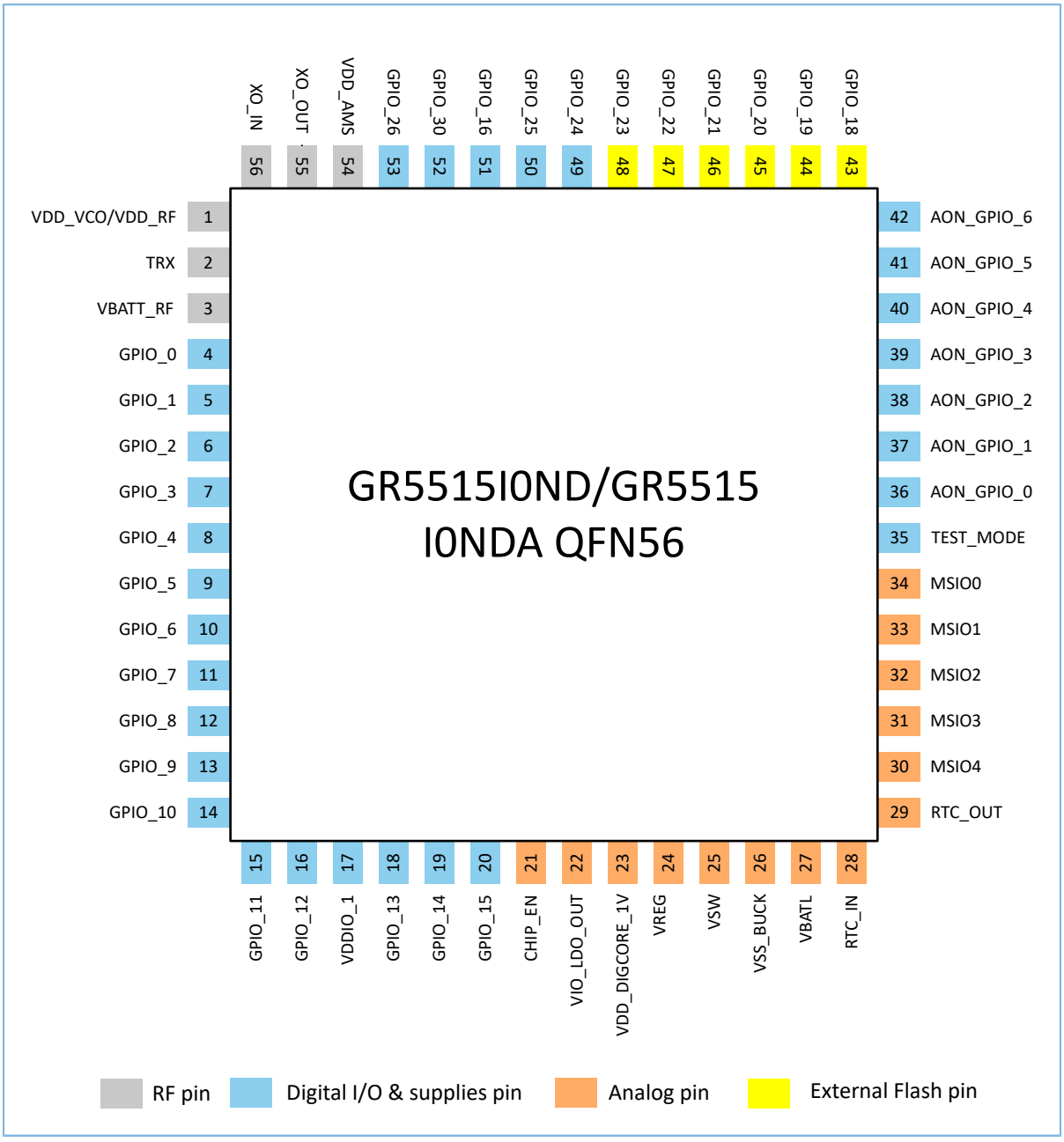


Figure 2-2 GR5515I0ND/GR5515I0NDA QFN56 package pinout

Table 2-2 shows pin descriptions of GR5515I0ND/GR5515I0NDA QFN56 package.

Table 2-2 GR5515I0ND/GR5515I0NDA QFN56 pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply. RF supply. Connect to VREG.	
2	TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF Supply	Connect to VBATL.	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
4	GPIO_0	Digital I/O	SWDCLK	VDDIO1
5	GPIO_1	Digital I/O	SWDIO	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O	VDDIO1
12	GPIO_8	Digital I/O	General purpose I/O	VDDIO1
13	GPIO_9	Digital I/O	General purpose I/O	VDDIO1
14	GPIO_10	Digital I/O	General purpose I/O	VDDIO1
15	GPIO_11	Digital I/O	General purpose I/O	VDDIO1
16	GPIO_12	Digital I/O	General purpose I/O	VDDIO1
17	VDDIO_1	Digital I/O supply	Digital I/O supply input	VDDIO1
18	GPIO_13	Digital I/O	General purpose I/O	VDDIO1
19	GPIO_14	Digital I/O	General purpose I/O	VDDIO1
20	GPIO_15	Digital I/O	General purpose I/O	VDDIO1
21	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. Minimum value of high level for CHIP_EN is 1 V.	
22	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator; when GR5515I0ND/GR5515I0NDA is used (high Flash supply voltage for GR5515I0NDA), the pin is used as power input pin of VDDIO0 digital IO domain by being connected to VBATL	Connected internally to VDDIO0
23	VDD_DIGCORE_1V	PMU	Output of on-chip LDO for digital core. Connect to a 1 µF capacitor.	
24	VREG	PMU	Feedback pin from switching regulator	
25	VSW	PMU	DC-DC converter switching node	
26	VSS_BUCK	PMU	DC-DC converter supply and general battery GND	
27	VBATL	PMU	Power supply input	
28	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
29	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
30	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
31	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
32	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
33	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
34	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
35	TEST_MODE	Digital I/O	Input pin, used to set test mode for FT or CP factory test. In the application phase, the value is set to 0 by default. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	VDDIO0
36	AON_GPIO_0	Digital I/O	Always-on GPIO	VDDIO0
37	AON_GPIO_1	Digital I/O	Always-on GPIO	VDDIO0
38	AON_GPIO_2	Digital I/O	Always-on GPIO	VDDIO0
39	AON_GPIO_3	Digital I/O	Always-on GPIO	VDDIO0
40	AON_GPIO_4	Digital I/O	Always-on GPIO	VDDIO0
41	AON_GPIO_5	Digital I/O	Always-on GPIO	VDDIO0
42	AON_GPIO_6	Digital I/O	Always-on GPIO	VDDIO0
43	GPIO_18	Digital I/O	Connect to an external Flash	VDDIO0
44	GPIO_19	Digital I/O	Connect to an external Flash	VDDIO0
45	GPIO_20	Digital I/O	Connect to an external Flash	VDDIO0
46	GPIO_21	Digital I/O	Connect to an external Flash	VDDIO0
47	GPIO_22	Digital I/O	Connect to an external Flash	VDDIO0
48	GPIO_23	Digital I/O	Connect to an external Flash	VDDIO0
49	GPIO_24	Digital I/O	General purpose I/O	VDDIO0
50	GPIO_25	Digital I/O	General purpose I/O	VDDIO0
51	GPIO_16	Digital I/O	General purpose I/O	VDDIO0
52	GPIO_30	Digital I/O	General purpose I/O	VDDIO0
53	GPIO_26	Digital I/O	General purpose I/O	VDDIO0

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
54	VDD_AMS	Analog/RF Supply	AMS supply. Connect to VREG.	
55	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
56	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

2.3 GR5515RGBD BGA68 (NRND)

Figure 2-3 shows the pin assignments of GR5515RGBD BGA68 package (top view).

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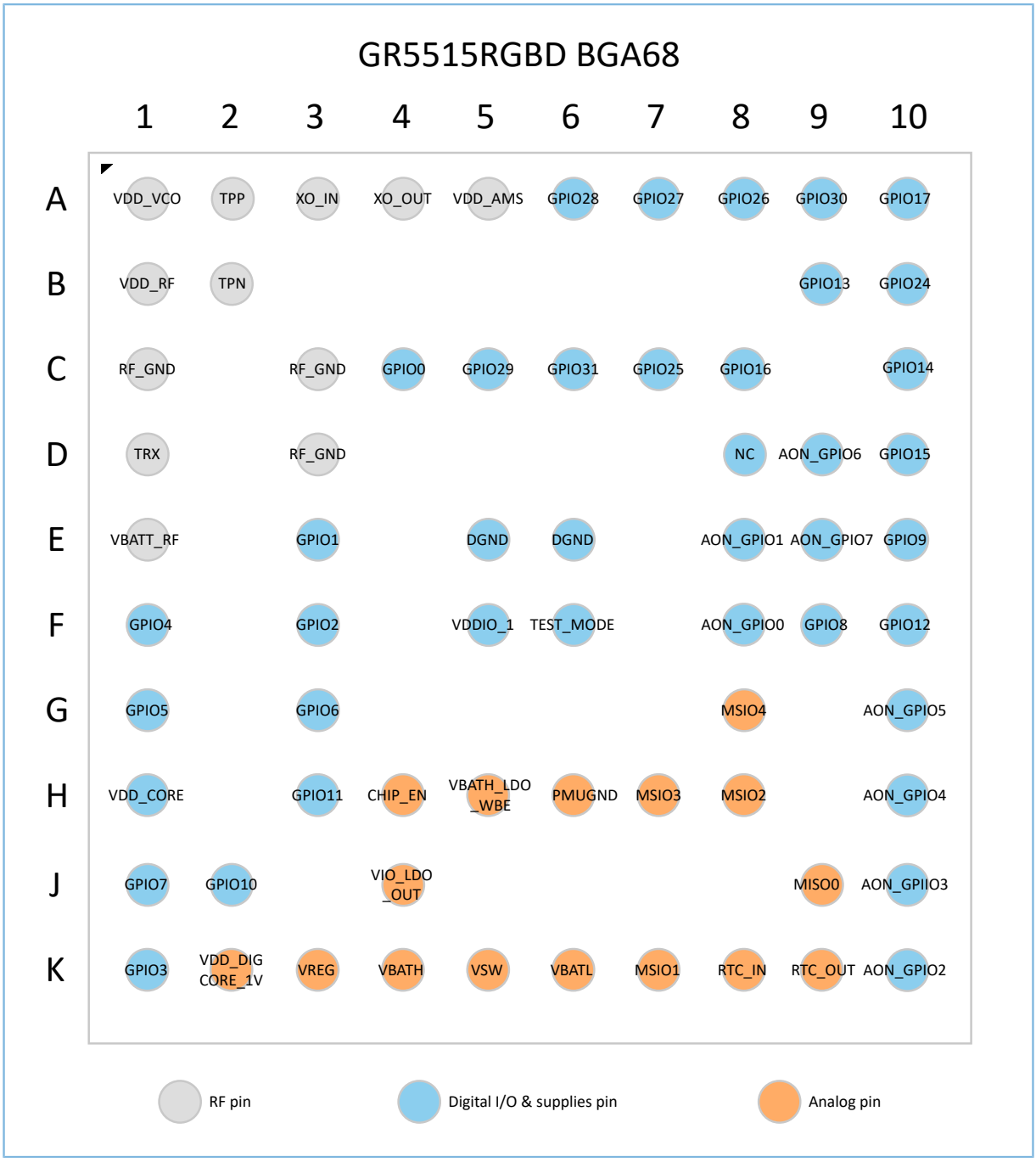


Figure 2-3 GR5515RGBD BGA68 package pinout

Table 2-3 shows pin descriptions of GR5515RGBD BGA68 package.

Table 2-3 GR5515RGBD BGA68 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A1	VDD_VCO	Analog/RF supply	Synthesizer VCO supply: 1.1 V	
A2	TPP	Analog/RF	Test Mux +output	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A3	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
A4	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
A5	VDD_AMS	Analog/RF	AMS supply 1.1 V	
A6	GPIO28	Digital I/O	General purpose I/O	VDDIO0
A7	GPIO27	Digital I/O	General purpose I/O	VDDIO0
A8	GPIO26	Digital I/O	General purpose I/O	VDDIO0
A9	GPIO30	Digital I/O	General purpose I/O	VDDIO0
A10	GPIO17	Digital I/O	General purpose I/O	VDDIO0
B1	VDD_RF	Analog/RF	RF supply 1.1 V	
B2	TPN	Analog/RF	Test Mux - output	
B9	GPIO13	Digital I/O	General purpose I/O	VDDIO1
B10	GPIO24	Digital I/O	General purpose I/O	VDDIO0
C1	RF_GND	Analog/RF	RF ground	
C3	RF_GND	Analog/RF	RF ground	
C4	GPIO0	Digital I/O	General purpose I/O, default SWDCLK	VDDIO1
C5	GPIO29	Digital I/O	General purpose I/O	VDDIO0
C6	GPIO31	Digital I/O	General purpose I/O	VDDIO0
C7	GPIO25	Digital I/O	General purpose I/O	VDDIO0
C8	GPIO16	Digital I/O	General purpose I/O	VDDIO0
C10	GPIO14	Digital I/O	General purpose I/O	VDDIO1
D1	TRX	Analog/RF	RX input and TX output	
D3	RF_GND	Analog/RF	RF ground	
D8	NC	-	-	
D9	AON_GPIO6	Digital I/O	Always-on General purpose I/O	VDDIO0
D10	GPIO15	Digital I/O	General purpose I/O	VDDIO1
E1	VBATT_RF	Analog/RF	Connect to VBATL	
E3	GPIO1	Digital I/O	General purpose I/O, default SWDIO	VDDIO1
E5	DGND	Digital GND	Digital Ground	
E6	DGND	Digital GND	Digital Ground	
E8	AON_GPIO1	Digital I/O	Always-on general purpose I/O	VDDIO0
E9	AON_GPIO7	Digital I/O	Always-on general purpose I/O	VDDIO0
E10	GPIO9	Digital I/O	General purpose I/O	VDDIO1

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
F1	GPIO4	Digital I/O	General purpose I/O	VDDIO1
F3	GPIO2	Digital I/O	General purpose I/O	VDDIO1
F5	VDDIO_1	Digital Supply	I/O supply voltage input	VDDIO1
F6	TEST_MODE	Digital I/O	Input pin, used to set test mode for FT or CP factory test. In the application phase, the value is set to 0 by default. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	VDDIO0
F8	AON_GPIO0	Digital I/O	Always-on general purpose I/O	VDDIO0
F9	GPIO8	Digital I/O	General purpose I/O	VDDIO1
F10	GPIO12	Digital I/O	General purpose I/O	VDDIO1
G1	GPIO5	Digital I/O	General purpose I/O	VDDIO1
G3	GPIO6	Digital I/O	General purpose I/O	VDDIO1
G8	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
G10	AON_GPIO5	Digital I/O	Always-on general purpose I/O	VDDIO0
H1	VDD_CORE	Digital Supply	Digital core supply	
H3	GPIO11	Digital I/O	General purpose I/O	VDDIO1
H4	CHIP_EN	Analog/PMU	Master Enable for chip reset pin. Minimum value of high level for CHIP_EN is 1 V.	
H5	VBATH_LDO_WBE	Analog/PMU	Connect to GND.	
H6	PMUGND	Analog/PMU	DC-DC converter supply & general battery GND	
H7	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
H8	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
H10	AON_GPIO4	Digital I/O	Always-on general purpose I/O	VDDIO0
J1	GPIO7	Digital I/O	General purpose I/O	VDDIO1
J2	GPIO10	Digital I/O	General purpose I/O	VDDIO1
J4	VIO_LDO_OUT	Analog/PMU	Output of On-Chip I/O supply regulator.	Connected internally to VDDIO0
J9	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
J10	AON_GPIO3	Digital I/O	Always-on general purpose I/O	VDDIO0
K1	GPIO3	Digital I/O	General purpose I/O	VDDIO1
K2	VDD_DIGCORE_1V	Analog/PMU	LDO output of On-Chip of digital core, connected to 1 µF capacitor	
K3	VREG	Analog/PMU	Feedback pin of switch regulator	
K4	VBATH	Analog/PMU	Connect to VBATL	
K5	VSW	Analog/PMU	DC-DC Converter Switching Node	
K6	VBATL	Analog/PMU	Input from battery	
K7	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
K8	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
K9	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
K10	AON_GPIO2	Digital I/O	Always-on general purpose I/O	VDDIO0

2.4 GR5515GGBD BGA55

Figure 2-4 shows the pin assignments of GR5515GGBD BGA55 package (top view).

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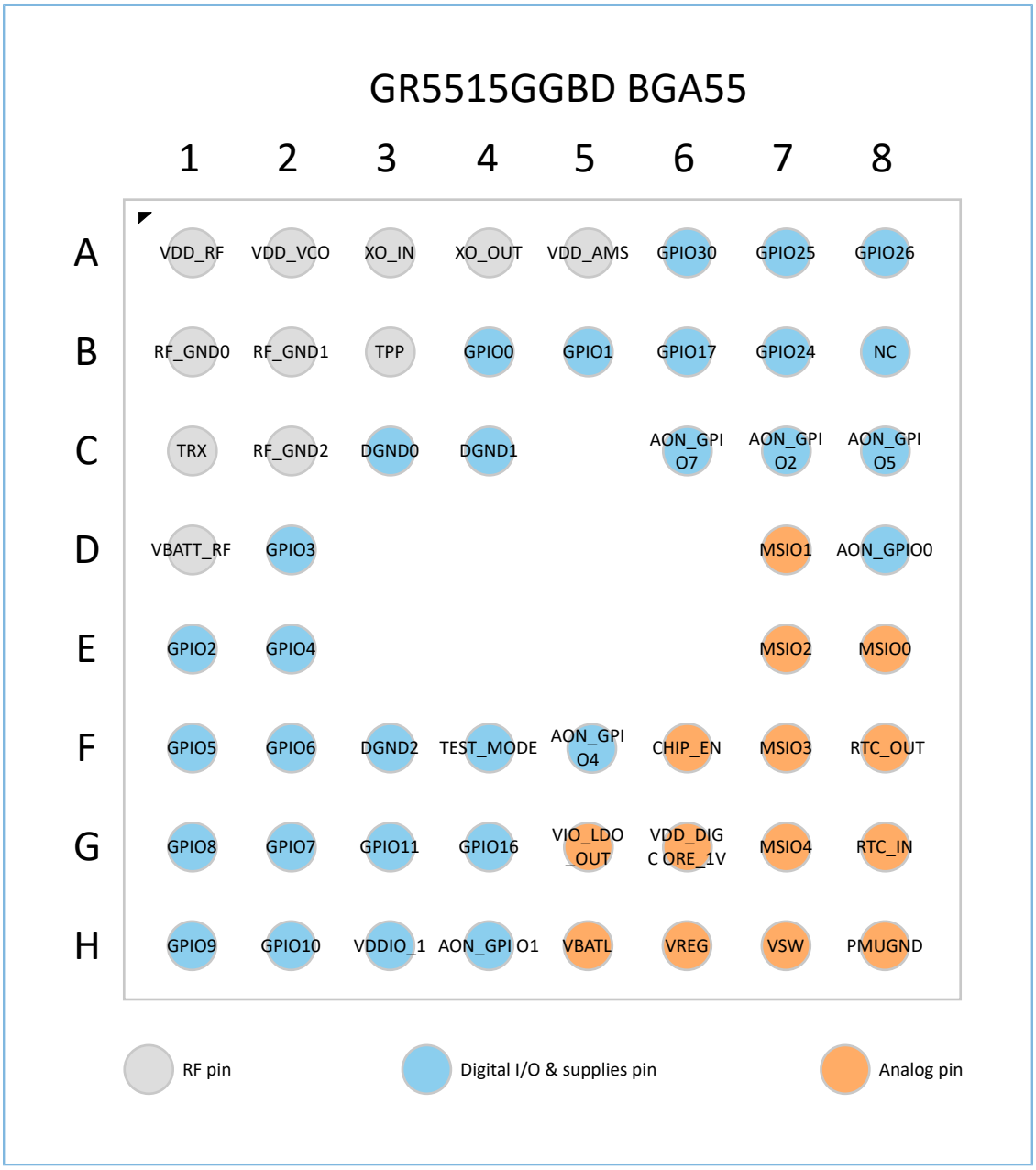


Figure 2-4 GR5515GGBD BGA55 package pinout

Table 2-4 shows pin descriptions of GR5515GGBD BGA55 package.

Table 2-4 GR5515GGBD BGA55 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A1	VDD_RF	Analog/RF supply	RF supply: 1.1 V	
A2	VDD_VCO	Analog/RF supply	Synthesizer VCO supply: 1.1 V	
A3	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A4	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
A5	VDD_AMS	Analog/RF supply	AMS supply 1.1 V	
A6	GPIO30	Digital I/O	General purpose I/O	VDDIO0
A7	GPIO25	Digital I/O	General purpose I/O	VDDIO0
A8	GPIO26	Digital I/O	General purpose I/O	VDDIO0
B1	RF_GND0	Analog/RF	RF ground	
B2	RF_GND1	Analog/RF	RF ground	
B3	TPP	Analog/RF	Test Mux + output	
B4	GPIO0	Digital I/O	General purpose I/O, default SWDCLK	VDDIO1
B5	GPIO1	Digital I/O	General purpose I/O, default SWDIO	VDDIO1
B6	GPIO17	Digital I/O	General purpose I/O	VDDIO0
B7	GPIO24	Digital I/O	General purpose I/O	VDDIO0
B8	NC	-	-	
C1	TRX	Analog/RF	RX input and TX output	
C2	RF_GND2	Analog/RF	RF ground	
C3	DGND0	Digital GND	Digital ground	
C4	DGND1	Digital GND	Digital ground	
C6	AON_GPIO7	Digital I/O	Always-on general purpose I/O	VDDIO0
C7	AON_GPIO2	Digital I/O	Always-on general purpose I/O	VDDIO0
C8	AON_GPIO5	Digital I/O	Always-on general purpose I/O	VDDIO0
D1	VBATT_RF	Analog/RF supply	Connect to VBATL	
D2	GPIO3	Digital I/O	General purpose I/O	VDDIO1
D7	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
D8	AON_GPIO0	Digital I/O	Always-on general purpose I/O	VDDIO0
E1	GPIO2	Digital I/O	General purpose I/O	VDDIO1
E2	GPIO4	Digital I/O	General purpose I/O	VDDIO1
E7	MSIO2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
E8	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
F1	GPIO5	Digital I/O	General purpose I/O	VDDIO1
F2	GPIO6	Digital I/O	General purpose I/O	VDDIO1

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
F3	DGND2	Digital GND	Digital ground	
F4	TEST_MODE	Digital I/O	Input pin, used to set test mode for FT or CP factory test. In the application phase, the value is set to 0 by default. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	VDDIO0
F5	AON_GPIO4	Digital I/O	Always-on general purpose I/O	VDDIO0
F6	CHIP_EN	Analog/PMU	Master Enable for chip reset pin Minimum value of high level for CHIP_EN is 1 V	
F7	MSIO3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
F8	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
G1	GPIO8	Digital I/O	General purpose I/O	VDDIO1
G2	GPIO7	Digital I/O	General purpose I/O	VDDIO1
G3	GPIO11	Digital I/O	General purpose I/O	VDDIO1
G4	GPIO16	Digital I/O	General purpose I/O	VDDIO0
G5	VIO_LDO_OUT	Analog/PMU	Output of On-Chip I/O supply regulator	Connected internally to VDDIO0
G6	VDD_DIGCORE_1V	Analog/PMU	LDO output of On-Chip of digital core, connected to 1 µF capacitor	
G7	MSIO4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
G8	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
H1	GPIO9	Digital I/O	General purpose I/O	VDDIO1
H2	GPIO10	Digital I/O	General purpose I/O	VDDIO1
H3	VDDIO_1	Digital I/O supply	I/O supply voltage input	VDDIO1
H4	AON_GPIO1	Digital I/O	Always-on general purpose I/O	VDDIO0
H5	VBATL	Analog/PMU	Input from battery	
H6	VREG	Analog/PMU	Feedback pin of switch regulator	
H7	VSW	Analog/PMU	DC-DC converter switching node	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
H8	PMUGND	Analog/PMU	DC-DC converter & general battery GND pin	

2.5 GR5513BEND/GR5513BENDU QFN40

Figure 2-5 shows the pinout of GR5513BEND/GR5513BENDU QFN40 package (top view).

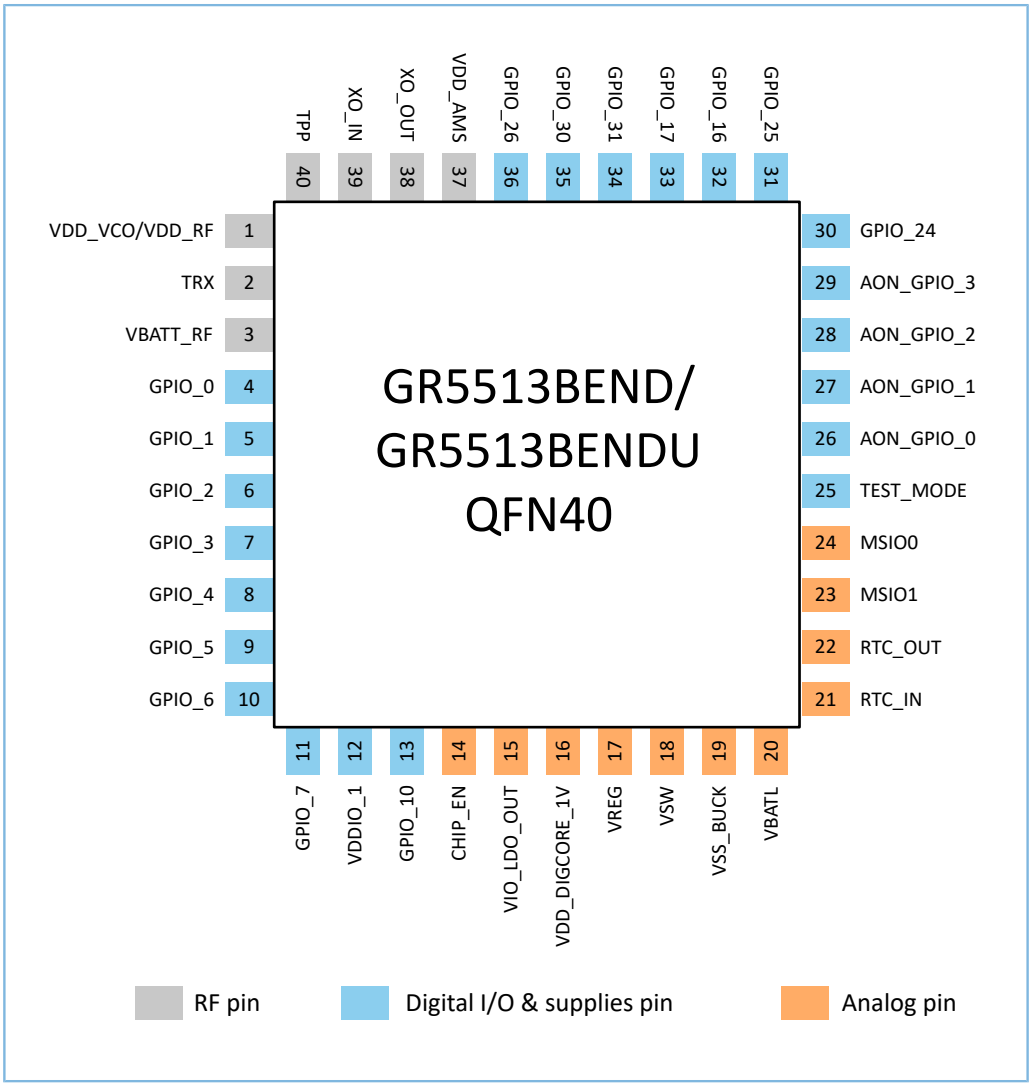


Figure 2-5 GR5513BEND/GR5513BENDU QFN40 package pinout

Table 2-5 shows pin descriptions of GR5513BEND/GR5513BENDU QFN40 package.

Table 2-5 GR5513BEND/GR5513BENDU QFN40 pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply. RF supply. Connect to VREG.	
2	TRX	Analog/RF	RX input and TX output	

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
3	VBATT_RF	Analog/RF	Connect to VBATL.	
4	GPIO_0	Digital I/O	General purpose I/O, default SWDCLK	VDDIO1
5	GPIO_1	Digital I/O	General purpose I/O, default SWDIO	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O	VDDIO1
12	VDDIO_1	Digital I/O Supply	Digital I/O supply input	VDDIO1
13	GPIO_10	Digital I/O	General purpose I/O	VDDIO1
14	CHIP_EN	Analog/PMU	Master Enable for chip reset pin. Minimum value of high level for CHIP_EN is 1 V.	
15	VIO_LDO_OUT	Analog/PMU	Output of on-chip I/O supply regulator. For GR5513BENDU, power input pin of VDDIO0 digital IO domain. When VDDIO0 is set to 3.3 V/VBATL, VIO_LDO_OUT should be connected to 3.3 V/VBATL.	Connected internally to VDDIO0
16	VDD_DIGCORE_1V	Analog/PMU	Output of on-chip LDO for digital core. Connect to a 1 µF capacitor.	
17	VREG	Analog/PMU	Feedback pin from switching regulator	
18	VSW	Analog/PMU	DC/DC converter switching node	
19	VSS_BUCK	Analog/PMU	DC/DC converter supply and general battery GND	
20	VBATL	Analog/PMU	Input from Battery	
21	RTC_IN	Analog/PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
22	RTC_OUT	Analog/PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
23	MSIO1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL
24	MSIO0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (ADC interface)	VBATL

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Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
25	TEST_MODE	Digital I/O	Input pin, used to set test mode for FT or CP factory test. In the application phase, the value is set to 0 by default. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	VDDIO0
26	AON_GPIO_0	Digital I/O	Always-on general purpose I/O	VDDIO0
27	AON_GPIO_1	Digital I/O	Always-on general purpose I/O	VDDIO0
28	AON_GPIO_2	Digital I/O	Always-on general purpose I/O	VDDIO0
29	AON_GPIO_3	Digital I/O	Always-on general purpose I/O	VDDIO0
30	GPIO_24	Digital I/O	General purpose I/O	VDDIO0
31	GPIO_25	Digital I/O	General purpose I/O	VDDIO0
32	GPIO_16	Digital I/O	General purpose I/O	VDDIO0
33	GPIO_17	Digital I/O	General purpose I/O	VDDIO0
34	GPIO_31	Digital I/O	General purpose I/O	VDDIO0
35	GPIO_30	Digital I/O	General purpose I/O	VDDIO0
36	GPIO_26	Digital I/O	General purpose I/O	VDDIO0
37	VDD_AMS	Analog/RF	AMS supply. Connect to VREG.	
38	XO_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
39	XO_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
40	TPP	Analog/RF	Test Mux + output	

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3 Minimal Design for GR551x SoC

The absolute necessary sections required for the GR551x SoC minimal system operation include

- Power supply
- Clock
- RF
- I/O pins
- SWD interfaces
- External Flash

To ensure the proper operation of a GR551x SoC, the design guidelines for the schematic diagram and the PCB layout are illustrated in the following sections.

3.1 Schematic Design Guideline

For the minimal schematic for a GR551x SoC, see "Section 4.1 Reference Schematic Diagram".

3.1.1 Power Supply

3.1.1.1 Introduction

GR551x SoCs are powered by external power sources through VBATL (voltage range: 1.7 V to 3.8 V).

To optimize battery utilization, it is recommended to supply a GR551x SoC with an external LDO regulator with low quiescent current (Ig) (lower than the product current when product is in standby mode) (output voltage: ≤ 3.3 V, output current: > 100 mA, load regulation (Iout: 10% – 120%) ≤ 10 mA).

When the maximum input level of the LDO regulator is higher than 5.5 V, connect a resistor (0.39 Ω – 1 Ω) in series to the input end of the LDO regulator to avoid overshoot when powering on the GR551x SoC in operation.

Figure 3-1 shows the power management unit in a GR551x.

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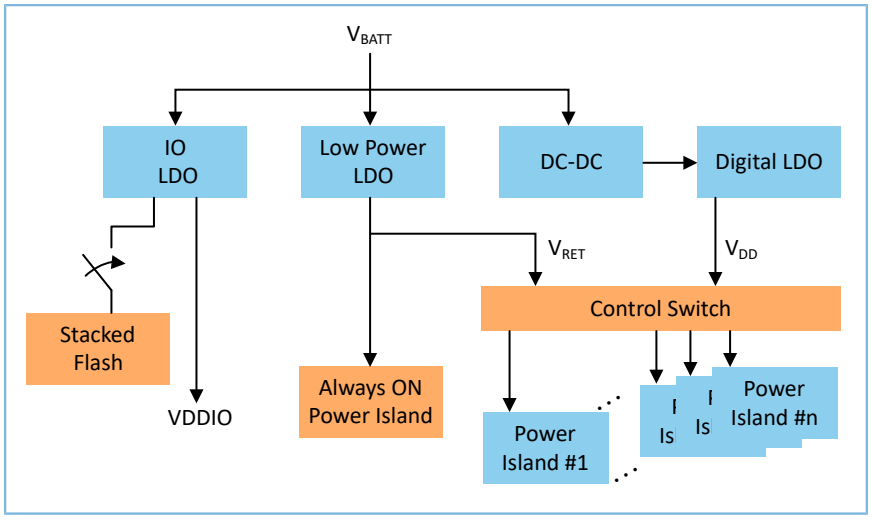


Figure 3-1 Power management block diagram

Power Management Unit (PMU) is responsible for generating all required voltages for different blocks in a GR551x.

- I/O LDO supplies on-chip Flash (except for GR5515I0ND and GR5515I0NDA) and I/O pins. For more information, see "Section 3.1.1.3 I/O LDO".
- For active mode, a DC-DC converter generates the voltage for the transceiver and an LDO regulator generates the voltage for digital blocks.
- GR551x uses an LDO regulator to supply its Always-ON (AON) modules that stay ON when both the MCU subsystem and the Bluetooth LE subsystem are OFF. The LDO regulator also generates a lower voltage for content retention to the memories where their content is needed after wake-up.
- Both the retention voltage and the digital voltage are connected to all power islands through a control switch matrix on the chip.

3.1.1.2 Power Supply Scheme

GR551x SoCs are equipped with a complete set of power management modules, which guarantee the smooth and secure functioning of the GR551x SoCs. This section introduces the GR551x reference circuit design by taking a GR551x SoC mounting BGA68 package as an example (see Figure 3-2).

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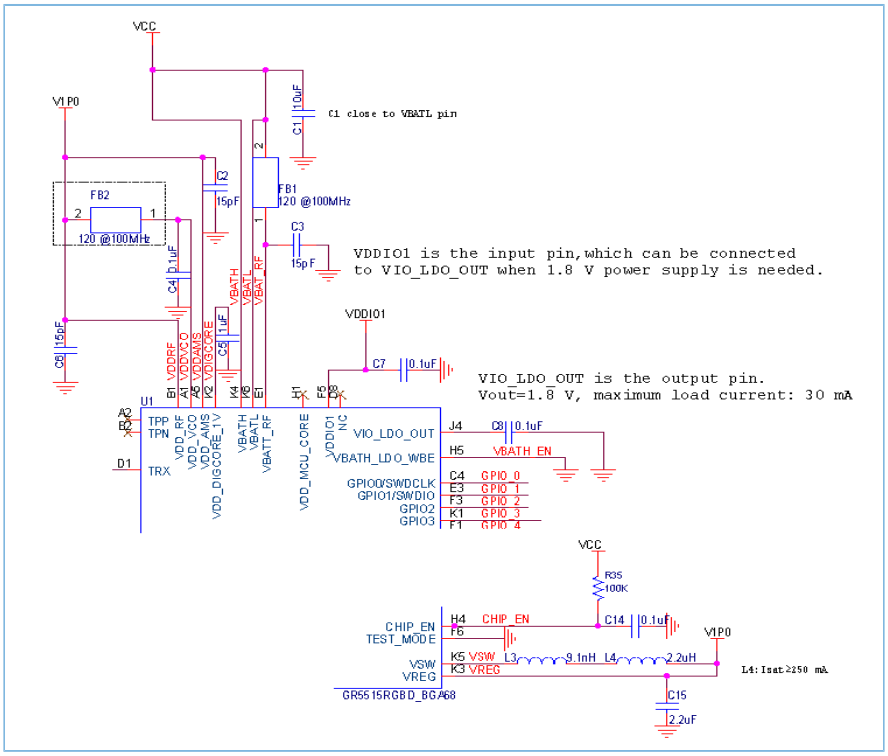


Figure 3-2 Power section of GR551x

The detailed pin descriptions and connection guidance are as follows:

- **VDD_VCO/RF:** internal RF block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 0.1 µF filter capacitor
- **VDD_AMS:** internal RF block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 15 pF filter capacitor
- **VDD_DIGCORE_1V:** output of digital LDO, which supplies the digital core logic. Place a 1 µF filter capacitor on this pin.
- **VBATL:** input supply for chip – ranging from 1.7 V to 3.8 V; connected to a 10 µF filter capacitor
- **VBATH:** connected to VBATL, which is only relevant to BGA68 package
- **VBATH_LDO_WBE:** connected to GND by default
- **VDD_MCU_CORE:** connected to the power of the digital core internally. The pin is left unconnected externally by default. It is only relevant to BGA68 package.
- **VBATT_RF:** connected to VBATL
- **VIO_LDO_OUT:** output of the on-chip VDDIO LDO regulator (connected to VDDIO0 internally by default), which is used to supply the on-chip Flash. It can also supply the VDDIO pins and external sensors with up to 30 mA load current. Connected to a 0.1 µF decoupling capacitor

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Note:

The external Flash of GR5515I0ND/GR5515I0NDA supports operations in high-voltage scenarios (when VDDIO0 = 3.3 V/VBATL), and the embedded Flash of GR5515IENDU/GR5513BENDU supports wide-voltage scenarios (range: 1.65 V–3.6 V). To use the SoCs in high-voltage scenarios,

- I/O LDO is set to off mode automatically based on eFuse configurations after system startup.
- Use VIO_LDO_OUT as input for the VDDIO0 domain, and connect VIO_LDO_OUT to the external power supply of 3.3 V or VBATL.

- **VSW:** DC-DC switching regulator output, connected to two inductors in series: a 9.1 nH inductor for reducing RF interference caused by switching noise and a 2.2 µH power inductor, as well as a 2.2 µF capacitor, to supply the SoC from V1P0 as a complete DC-DC circuit. The pin is also connected to VDD_RF, VDD_AMS, and VDD_VCO through external circuits.
- **VREG:** feedback pin from the DC-DC switching regulator output, connected to V1P0
- **VDDIO1:** supply pin for I/O1 voltage domain, supplied from VIO_LDO_OUT or external regulator, connected to a 0.1 µF filter capacitor

Recommended capacitors, ferrite beads, and inductors are listed in Table 3-1 and Table 3-2.

Table 3-1 Recommended decoupling capacitors and ferrite beads for the power section

Reference	Description	Value	Package	Mfg Part #
C15	CAP CER X5R 10% 6.3 V	2.2 µF	0603	Murata GRM188R61C225KE15D
C4, C7, C8, C14	CAP CER X7R 10% 10 V	0.1 µF	0402	Murata GRM155R71A104KA01D
C5	CAP CER X5R 10% 6.3 V	1 µF	0402	Samsung CL05A105KO5NNNC
C1	CAP CER X5R 20% 10 V	10 µF	0603	Murata GRM188R61A106ME69
C2, C3, C6	CAP CER NPO ±5% 50 V	15 pF	0603	AVX 04025A150JAT2A
FB1, FB2	Ferrite Bead, 120 Ω @ 100 MHz, 400 mA, 500 mOhm, 0603	120 Ω @ 100 MHz	0603	Murata BLM18AG121SN1

Table 3-2 DC-DC inductors (9.1 nH) recommended for use

Reference	Value	DC Resistance (Max)	Saturation Current	Size L x W x H (mm)	Mfg Part #
L3	9.1 nH	0.32 Ω	300 mA	1.0 x 0.5 x 0.5	Murata LQG15HS9N1J02D

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Table 3-3 DC-DC inductors (2.2 µH) recommended for use

Reference	Value	DC Resistance (Typ)	Saturation Current	Size L x W x H (mm)	Mfg Part #
L4	2.2 µH ± 20%	0.3 Ω	250 mA	1.6 x 0.8 x 0.8	Sunlord MPH160809S2R2
		0.2 Ω	250 mA	1.6 x 0.8 x 0.8	Murata LQM18PN2R2MGH
		0.38 Ω	300 mA	1.6 x 0.8 x 0.8	Murata LQM18PN2R2MFH

The 2.2 µH DC-DC inductors are adopted in DC-DC buck converter circuits in Pulse Skip Mode (PSM) and play a crucial role in these circuits. The saturation current of the circuit shall be higher than 250 mA. To ensure secure operation and to improve the performance of GR551x, inductors with higher saturation current and lower direct current resistance are preferred, because a higher direct current resistance means higher power consumption.

3.1.1.3 I/O LDO

The GR551x has an on-chip linear LDO regulator that is used to supply a nominal 1.8 V (default value) for use in supplying the on-chip Flash (except for GR5515I0ND and GR5515I0NDA) as well as the chip's I/O (the VDDIO0 pins). Additionally, this regulator can supply external components (sensors) which interface to the GR551x. The LDO is capable of supplying up to 30 mA load current.

The output of this regulator is the VIO_LDO_OUT pin. A 0.1 µF decoupling capacitor should be placed close to this pin.

Three I/O voltage domains are provided for GR551x: two digital voltage domains (VDDIO0 and VDDIO1), as well as one mixed signal I/O domain MSIO, corresponding to reference voltage levels at VDDIO0, VDDIO1, and VBATL respectively. Note that VDDIO0 is connected to VIO_LDO_OUT internally, and is not bonded to any package pins. Figure 3-3 is a circuit diagram showing the connection between VIO_LDO_OUT and the I/O domains.

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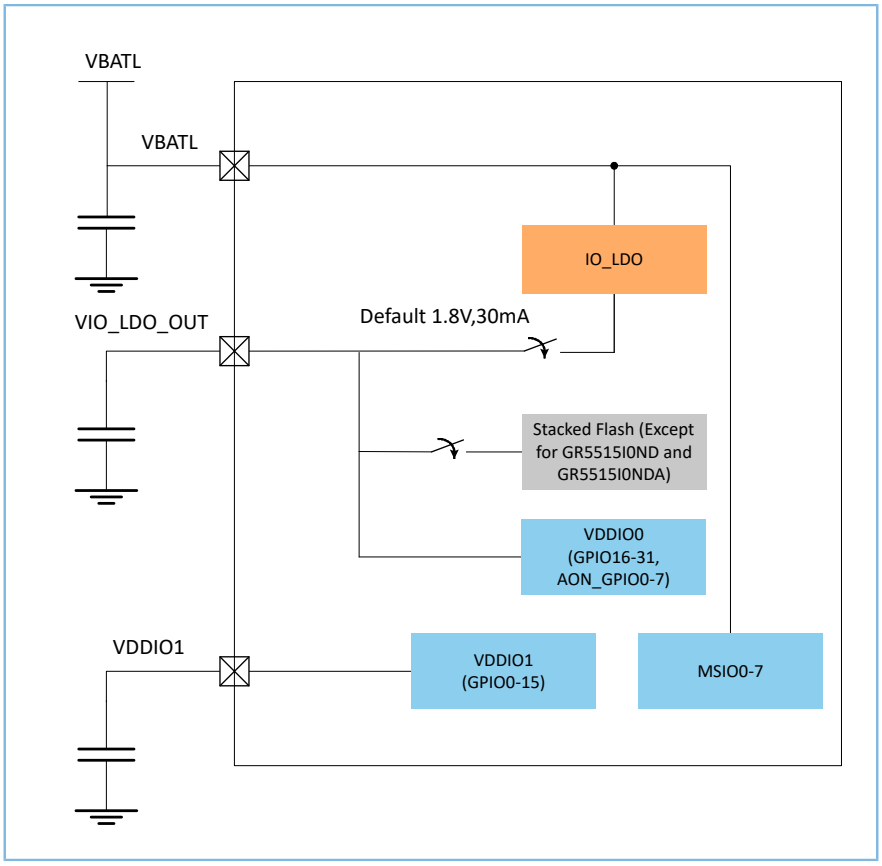


Figure 3-3 Connection between VIO_LDO_OUT and I/O domains

Note:

The leakage current of I/O LDO is approximately 0.7 μA.

VIO_LDO_OUT is connected to the power of Flash on chip. The operating voltage of Flash is 1.8 V (except for the Flash of GR5515I0ND, GR5515I0NDA, GR5515IENDU, and GR5513BENDU), and therefore the default voltage of VIO_LDO_OUT is 1.8 V. When VDDIO1 is connected to VIO_LDO_OUT on an external circuit, the I/O voltage domains of the chip is 1.8 V (except for MSIOs). If you need to change the I/O voltage domain corresponding to VDDIO1, use an external power supply (voltage range: 1.8 V – 3.3 V) for VDDIO1. In this process, the levels of the GPIOs corresponding to VDDIO1 vary, depending on the external input voltage. When the external power supply is connected to VDDIO1, make sure the input voltage at VDDIO1 is not higher than that of the power (VBATL).

The external Flash of GR5515I0ND/GR5515I0NDA supports operations in high-voltage scenarios (when VDDIO0 = 3.3 V/VBATL), and the embedded Flash of GR5515IENDU/GR5513BENDU supports wide-voltage scenarios (range: 1.65 V–3.6 V). To use the SoCs in high-voltage scenarios,

- I/O LDO is set to off mode automatically based on eFuse configurations after system startup.
- Use VIO_LDO_OUT as input for the VDDIO0 domain, and connect VIO_LDO_OUT to the external power supply of 3.3 V or VBATL.

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Note:

The voltage domain VDDIO1 supplies GPIO0 – GPIO15; VDDIO0 is bonded to VIO_LDO_OUT internally and supplies GPIO16 – GPIO31 and AON_GPIO0 – AON_GPIO7.

3.1.2 Clock

3.1.2.1 Introduction

GR551x's clock source is generated by an external 32 MHz crystal oscillator, and the real-time clock (RTC) by an external 32.768 kHz crystal oscillator.

3.1.2.2 32 MHz Clock (XO)

The system clock, or CPU clock, is based on a 32 MHz crystal oscillator. Table 3-4 shows the specification for the crystals that can be used for these applications, and Table 3-5 shows some recommended component examples.

Table 3-4 GR551x crystal specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
Crystal Freq	Crystal oscillator frequency			32		MHz
ESR	Equivalent series resistance				100	Ohm
C_{load}	Load capacitance		6		8	pF
f-Xtal	Crystal frequency initial tolerance				+/-50	ppm
f-Xtal	Crystal frequency tolerance – over temperature				+/-30	ppm
f-Xtal	Crystal frequency tolerance – aging over life of product				+/-10	ppm
P_{DRV}	Max drive power				100	µW

Table 3-5 Recommended 32 MHz crystal examples

Part Number	Abracon ABM10W-32.0000MHZ-6-D1X-T3	TAITIEN G0068-X-006-3	Murata XRCGB32M000F5N10R0	TXC 8Z32000004
Frequency	32 MHz	32 MHz	32 MHz	32 MHz
Initial tolerance	+/-10 ppm	+/-40 ppm	+/-50 ppm	+/-10 ppm
Tolerance over Temp.	+/-20 ppm	+/-30 ppm	+/-30 ppm	+/-20 ppm
Load capacitance	6 pF	6 pF	6 pF	8 pF
ESR	70 ohms	30 ohms	≤ 100 Ω	≤ 60 Ω
Temperature range	–40°C to +85°C	–40°C to +105°C	-40°C to +85°C	-40°C to +85°C
Size (L x W x H, mm)	2.5 x 2.0 x 0.60	2.5 x 2.0 x 0.60	2.0 x 1.6 x 0.60	2.5 x 2.0 x 0.60

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Note:

To ensure system stability and low power consumption, load capacitance of the 32 MHz crystal oscillator shall be within the range from 6 pF to 8 pF. The 32 MHz crystal oscillator does not need to be connected with load capacitors, but it needs to use the production tool for frequency offset calibration. When designing an application circuit, you shall reserve the interface or test points (SWDCLK, SWDIO, CLK_TRIM (any GPIOs except MSIOs), GND, VBAT) required by the mass production tool.

3.1.2.3 32.768 kHz Clock

The GR551x uses a low-power, low-frequency clock in deep sleep modes, which also extends battery lifespan. The utilization of the external 32.768 kHz crystal oscillator provides tighter timing and better accuracy, resulting in lower overall power consumption.

The GR551x integrates an adjustable load capacitance, and typically no external load capacitors are required.

The external crystal must meet the recommended operating conditions as indicated in Table 3-6, and Table 3-7 shows examples of crystals that meet the specifications.

Table 3-6 32.768 kHz crystal oscillator recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
Crystal Freq	Crystal oscillator frequency			32.768		kHz
ESR	Equivalent series resistance				100,000	Ohm
Cload	Load capacitance		6		9	pF
f-Xtal	Crystal frequency initial tolerance				+/-50	ppm
f-Xtal	Crystal frequency tolerance – over temperature and aging				+/-250	ppm
PDRV	Max drive power				0.5	µW

Table 3-7 32.768 kHz crystal oscillator example specifications

Part Number	Abracon ABS05-32.768KHZ-9-T
Frequency	32.768 kHz
Initial tolerance	+/–20 ppm
Tolerance over Temp.	+/–250 ppm
Load capacitance	9 pF
ESR	90,000 ohms
Temperature range	–40°C to +85°C
Size (L x W x H, mm)	1.6 x 1.0 x 0.50

Note:

To ensure system stability and low power consumption, load capacitance of the 32.768 kHz crystal oscillator shall be within the range from 6 pF to 9 pF.

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3.1.3 RF

3.1.3.1 Introduction

Figure 3-4 shows the functional block diagram of a GR551x transceiver.

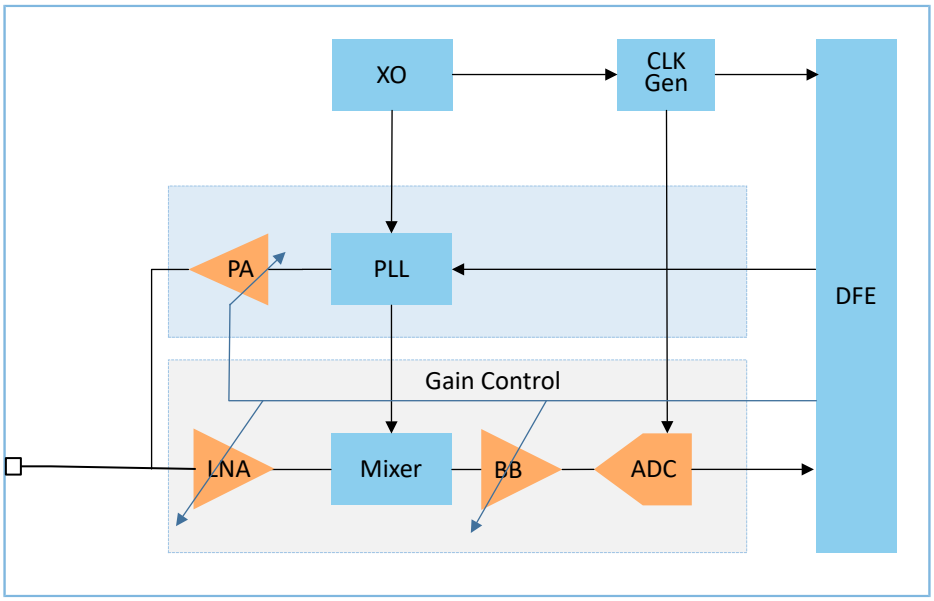


Figure 3-4 GR551x transceiver architecture

Operating mechanisms:

- On the receiver side:
  1. After the antenna receives an RF signal, the receiver digitizes the signal in a path: Low noise amplifier (LNA) > Mixer > Baseband (BB) amplifier > an analog-to-digital converter (ADC).
  2. The digitized signals are sent to the digital frontend (DFE) for demodulation.
  3. The digital frontend provides Automatic Gain Control (AGC) feedback signals to adjust the gain of the LNA and BB amplifier to maximize the signal-to-noise ratio (SNR) at the demodulation.
- On the transmitter side:
  1. The digital signal from the DFE is transmitted to a phase-locked loop (PLL) for modulation.
  2. The modulated carrier wave is delivered to a power amplifier (PA) with amplification factor configurable by the digital gain settings.
  3. The modulated carrier is transmitted to the antenna through a low-power or high-power PA path. The antenna radiates the amplified carrier wave through electromagnetic waves.

Note:

RF and digital clocks are generated from the XO.

3.1.3.2 RF Scheme

The following figure is the recommended RF matching circuit in the GR5551x SoC minimal system.

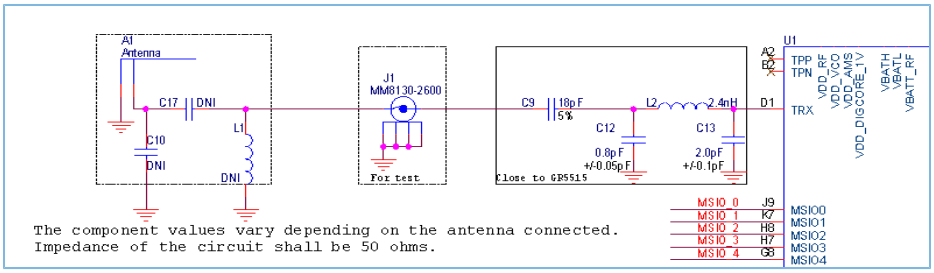


Figure 3-5 RF scheme

In the circuit, the left PI matching network (composed of the inductor L1 plus capacitors C10 and C11) matches the antenna; C9 is a DC blocking capacitor; the right PI type matching network (composed of the inductor L2 plus capacitors C12 and C13) matches the internal PA of GR551x. The network connects to the TRX pin of the chip.

Recommended configurations of capacitors C12, C13, C9, and the inductor L2 are displayed in Table 3-8.

Table 3-8 Recommended devices for the RF section

Reference	Description	Value	Package Size	Mfg Part #
C9	CAP CER NPO 18 pF ±5% pF 50 V	18 pF	0402	Murata GRM1555C1H180JA01D
C12	CAP CER NPO 0.8 pF ±0.05 pF 50 V	0.8 pF	0402	Murata GRM1555C1HR80WA01D
C13	CAP CER NPO 2.0 pF ±0.1 pF 50 V	2.0 pF	0402	Murata GRM1555C1H2R0BA01D
L2	Inductor, Wirewound, 2.4 nH ±0.2 nH, 50 mOhm, Q = 20 @ 250 MHz	2.4 nH	0402	Murata LQW15AN2N4B00

3.1.4 I/O Pins

The GR551x has software-configurable I/O pin assignment where different peripherals can be multiplexed out on different chip pins. When configured to GPIOs, they can be set as input, output, with configurable pull-up or pull-down resistors. I/O pins retain their last state when system enters the sleep or deep sleep mode. Only AON_GPIOs can be used to wake up the system from sleep/deep sleep mode.

Note:

- For more details of pin mux, refer to *GR551x Datasheet*.
- Note that MSIO pins do not support hardware interrupt when allocating I/O functions during designing PCB applications.
- Two PWM modules(PWM0 and PWM1) are provided, with each containing three separate output channels: PWMA, PWMB, and PWMC. Frequencies of the three PWM channels in one group are the same, and individual frequency control is not supported. Phase and duty cycle of each channel can be configured via registers.

3.1.5 SWD Interfaces

GR551x connects to J-Link for modulation by using Serial Wire Debug (SWD) interfaces.

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Table 3-9 shows the pins to which the SWD interfaces connect in QFN and BGA packages.

Table 3-9 Pin matching for SWCLK and SWDIO in QFN and BGA packages

SWD	Pin # (QFN56)	Pin # (BGA68)	Pin # (BGA55)	Pin # (QFN40)
SWCLK	Pin 4	Pin C4	Pin B4	Pin 4
SWDIO	Pin 5	Pin E3	Pin B5	Pin 5

The pins can be multiplexed as GPIOs when the SWD interfaces are not in use.

3.1.6 External Flash

GR5515I0ND/GR5515I0NDA uses an external Flash with various model options provided. GR5515I0NDA supports both low-voltage (typical: 1.8 V) and high-voltage (typical: 3.3 V) Flash whereas GR5515I0ND supports high-voltage Flash (typical: 3.3 V) only. According to the electrical characteristics and functional requirements of the SoCs, Goodix recommends the following GR5515I0ND series Flash candidates. Table 3-10 applies to both GR5515I0ND and GR5515I0NDA, and Table 3-11 applies to GR5515I0NDA only.

Table 3-10 Recommended GR5515I0ND Series Flash candidates (high voltage)

Flash Model	Manufacturer	Flash Size	Voltage Range (V)
P25Q128H	Puya Semiconductor	128 Mb	2.30–3.60
W25Q64JV	Winbond	64 Mb	2.70–3.60
XM25QH64A	XMC	64 Mb	2.30–3.60
XT25F64B	XTX	64 Mb	2.70–3.60

Table 3-11 Recommended GR5515I0ND Series Flash candidates (low voltage)

Flash Model	Manufacturer	Flash Size	Voltage Range (V)
P25Q128L	Puya Semiconductor	128 Mb	1.65–2.00
XT25Q64D	XTX	64 Mb	1.65–2.10

Note:

- Low-voltage supply (Typical: 1.8 V) for Flash is supported in GR551x SDK V1.6.11 and later versions. As GR5515I0NDA supports wide-voltage Flash, when high-voltage Flash is to be used, configure eFuse with the production line tool GRPLT.
- Not all external Flash supports data read at 64 MHz. In such case, lower the Quad SPI data rate based on the actual Flash data transfer rate.
- In practice, the operating frequency of GR5515I0ND Flash varies depending on component package, layout, and routing of the whole system. Therefore, it is recommended that you choose a proper Flash memory that meets the electrical characteristics and functional requirements based on actual project demands.

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For more details about Flash model selection for GR5515I0ND and GR5515I0NDA, see *GR5515I0ND Series Flash Selection Guide*.

3.2 PCB Design and Layout Guideline

3.2.1 PCB Layer Stackup

A 4-layer PCB layout is recommended to be used for all GR551x package options. Figure 3-6 shows the recommended layer stackup (thickness: 1.6 mm) of GR551x.

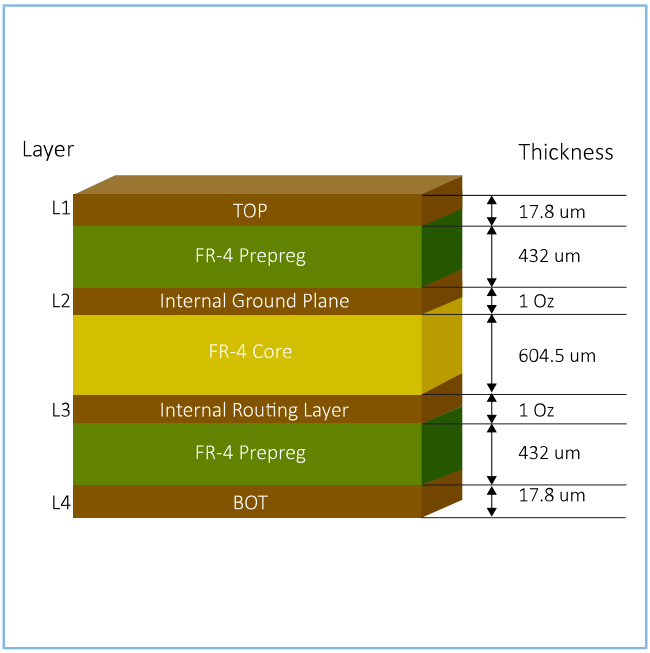


Figure 3-6 GR551x PCB layer stackup

L1: top layer where components, RF transmission lines, and key signal lines are placed

L2: internal ground plane layer, used for both the ground return path and the reference plane for the 50 ohm RF transmission line

L3: internal routing layer, used to split power domains and place a small number of signal lines

L4: bottom layer where components and signal lines are placed

---

Note:

The customer's product design can be adjusted according to the actual situation. Two typical examples for designing 4-layer PCB layouts are provided in "Section 4.2.1 Four-layer PCBs in QFN56 Package" and "Section 4.2.4 Four-layer PCBs in BGA68 Package (NRND)", to help users quickly get started with development and PCB layout design.

For users who need to reduce costs on QFN packages, they shall choose 2-layer PCBs, with special attention to the layout of power filter components, power input, the ground return path for DC-DC buck converters, and completeness of the reference plane for RF route. For details on the layout and routing, see "Section 4.2.2 Two-layer PCBs in QFN Packages".

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3.2.2 Components Layout

All components operating at high frequency should have their layout made as compact as possible. This will prevent the cross-coupling between lines and also minimize the parasitic effects which will have a negative impact on the operating parameters.

When designing the layout, make sure the main chip is as close to the antenna interface as possible, and no other components are under the RF routing if possible (the layout and routing of RF components are of higher priority).

3.2.3 Power Supply

Power supply is essential to ensure proper operation of an SoC, and therefore special attention should be paid on the layout and routing of the key power systems, which are DC-DC switching regulator and RF input power supply. To avoid system-level issues (such as poor performance in ESD protection and radiation off limits) caused by improper power design, abide by the design hints described in the two following sections.

3.2.3.1 DC-DC Switching Regulator

Take GR5515RGBD for example. The chip includes a DC-DC switching regulator. To design the PCB layout involving a DC-DC switching regulator,

1. Components (L3: 9.1 nH inductor, L4: 2.2 µH inductor, and C15: 2.2 µF capacitor) connected to DC-DC switching regulator should be placed as close to VSW and VREG of the chip as possible. A distance within 3 mm is recommended.
2. The net of VSW radiates stronger interference before VSW signals passing through the inductors, and thus should be placed at a minimum distance of 0.2 mm from other power nets and signals, especially V1P0 and DIGCORE.
3. Placing L4 perpendicular to L3 is recommended, to avoid inductive coupling. C15 should be placed behind L4, and VREG network is connected to the power supply after capacitor filtering.
4. GND pin of C15 should be placed as close to VSS_BUCK of the chip as possible. Vias of C15 GND pin should be placed as close to the GND pin as possible. It is recommended to connect the C15 GND pin to VSS_BUCK by using GND Polygon Plane, so that the return path of the power can be kept minimal.

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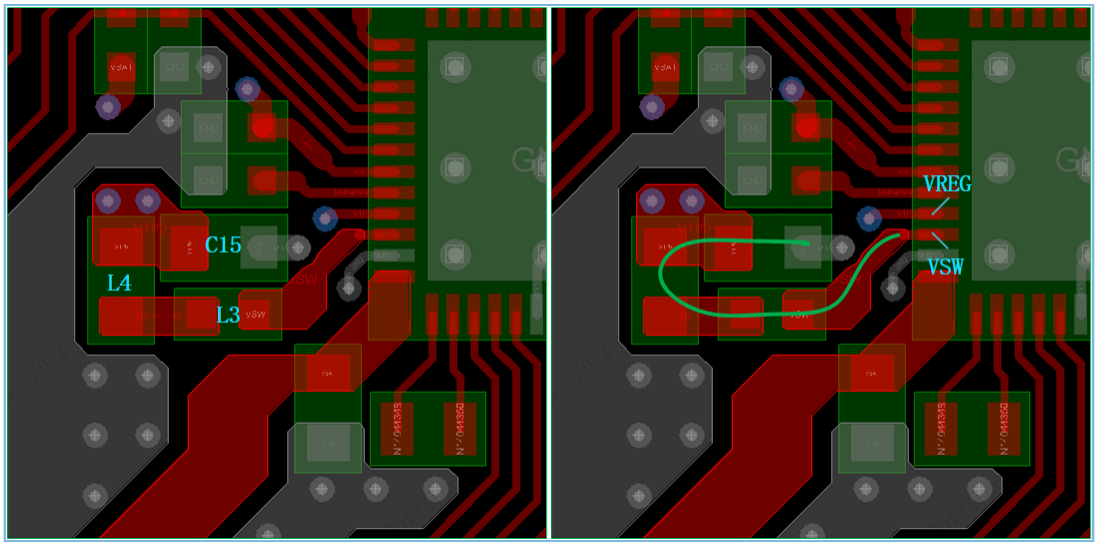


Figure 3-7 Reference layout and routing for DC-DC switching regulator

Note:

The green line in the right figure of Figure 3-7 indicates the power output path.

3.2.3.2 RF Input Power Supply

Make sure the following instructions are met when designing RF input power supply in PCB layout, to ensure optimal performance and to avoid excessively high radiation.

1. Decoupling capacitors (highlighted in yellow rectangles in Figure 3-8) connected to VDD_RF, VDD_VCO, and VDD_AMS should be as close to the corresponding pin as possible (around 1 mm is recommended, and shall not exceed 3 mm). Place the capacitors on the same layer with the pins if possible, and make sure the wiring path goes through the capacitors first and then connected to the chip power pins. In case the capacitors are not placed on the same layer with the pins, the vias should be located close to the decoupling capacitors.
2. The power trace should be as short as possible, and at least 0.2 mm wide. A minimum distance at 0.2 mm from other signals should be guaranteed.

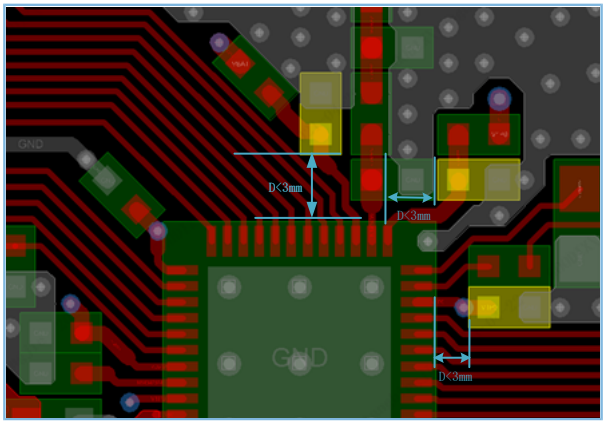


Figure 3-8 Reference layout and routing for RF input power supply

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C1 (10 µF capacitor) is placed close to the VBATL pin; C4, C7, and C8 (0.1 µF capacitors) are placed close to the VDD_VCO, VDDIO1, and VIO_LDO_OUT respectively, and C2, C3, and C6 (15 pF capacitors) close to VDD_AMS, VBATT_RF, and VDD_RF respectively. C5 (1 µF capacitor) is placed close to pin VDD_DIGCORE_1V, as shown in Figure 3-9 below.

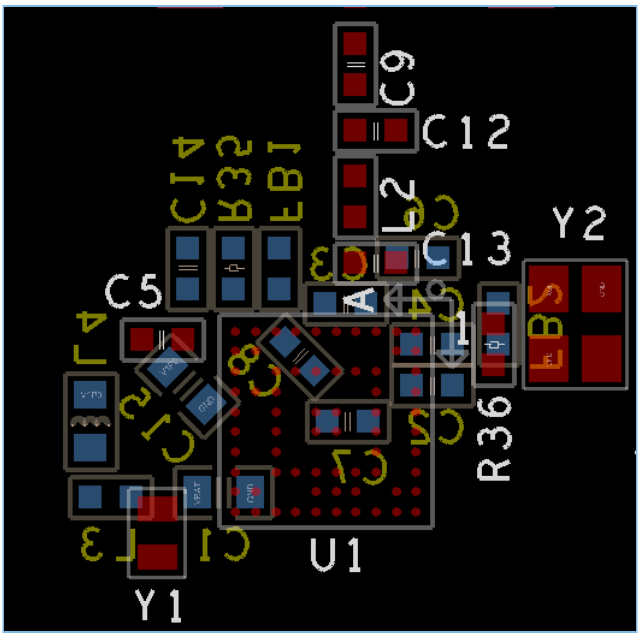


Figure 3-9 Power supply of GR5515RGBD PCB (reference)

3.2.4 Clock

Place the crystal as close as possible to the IC (recommended distance: ≤4 mm). This will minimize any additional capacitive load on the input pins and reduce the chance of crosstalk and interference with other signals on the board. Make sure there is no other trace route next to/under the crystal or the crystal routes.

It is recommended to shield the routes of the 32 MHz crystal. If the ground below the crystal is clean and no crosstalk or interference is involved, provide openings on the pad underneath the crystal (as shown in Figure 3-11), which helps to reduce parasitic capacitance.

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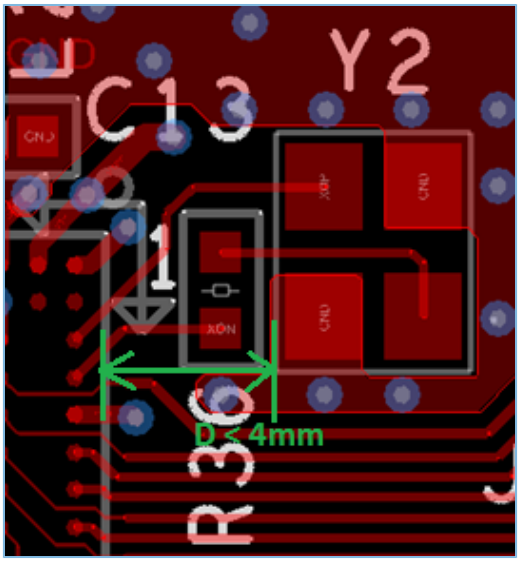


Figure 3-10 Clock PCB Ref of GR5515RGBD (reference)

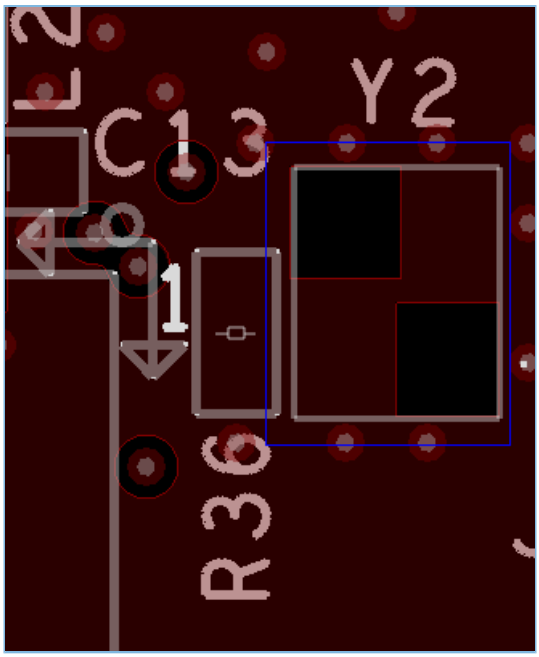


Figure 3-11 Openings on PCB pad for clock crystal of GR5515RGBD

3.2.5 RFIO Port

The GR551x provides a single-ended RFIO port. A copper RFIO trace with a characteristic impedance of 50 Ω interconnects the RF port and the antenna. Because the impedance of RFIO port is not 50 Ω, a matching network is required to match the port impedance between the RF port and the 50 Ω transmission line.

Components in this network must be placed as close as possible to the RFIO pin. Try to place the first component no further than 1 mm from the RFIO pin. Figure 3-12 shows the PCB layout of the RF port.

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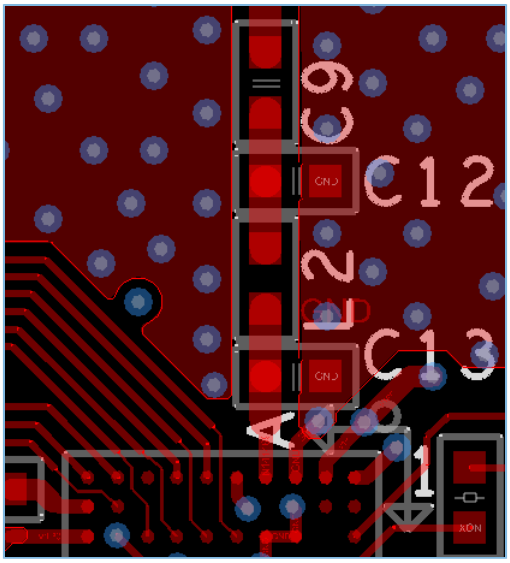


Figure 3-12 GR551x routing on a PCB

Note:

The RF route should be straight and as short as possible. If a curving route is necessary for a specific structure, an inverted arc is required for a turning, and angles at or less than 90◦ are not allowed.

RF routing at the PCB surface (the top layer or the bottom layer) helps avoid using vias or switching layers, and is therefore preferred. Stub routes should be avoided, and the reference ground plane underneath the RF route shall be complete. The RF route shall be of the same width as the component pad. This ensures there will not be discontinuities in the 50 Ω transmission line due to a mismatch between the component pad size and trace size.

Taking the 4-layer PCB layout design as an example, the transmission line is routed as a coplanar waveguide using layer-2 ground as the reference plane. The dimensions are:

- Trace width: 559 µm
- Spacing from trace to top layer: 178 µm
- Spacing from top layer to layer 2: 432 µm

The design uses FR-4 dielectric and 0.5 ounce copper on the outer layer. In actual design, PCB manufacturers are required to provide single-ended RFIO traces with an impedance of 50 Ω (+/–10%).

Ground vias should be placed along the transmission line every 1.25 mm and right next to the ground pads of the matching components.

A PI-network should be placed close to the antenna feedpoint for antenna matching purposes. The matching network value of antenna is adjusted according to the actual antenna used. It is recommended to use mature antenna schemes and recommended values of antenna factories.

3.2.6 Grounding

Always provide a solid grounding for the radio IC of GR551x. Use as many vias as possible to create a solid GND under the IC itself and connect it to inner and bottom GND layers.

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For the center ground paddle (at the package bottom) of QFN packages, use a matrix of 3 x 3, 4 x 4, or other vias to the ground-plane.

The GND of the 10 µF filter capacitor connecting to VBATL shall be close to the main GND pin, and apply copper pouring if possible (see "Section 3.2.3 Power Supply"). The ground return path of the GND pin (VSS_BUCK) of DC-DC power shall be in good condition, which guarantees stable and secure operation of ICs.

Note:

- Make sure the ground-pad shape follows the shape of the paddle on chip, including the exposed paddle parts (for QFN packages).
- Make sure a ground via is placed right next to the TRX pin.
- For the BGA packages, place ground vias as close as possible to the ground balls.

3.2.7 ESD Protection Design

3.2.7.1 System-level ESD Design

System efficient electrostatic discharge (ESD) design is crucial for any circuits, and requires users to follow the design guidelines (including schematic diagrams, PCB layout, and product structural designs) provided in the sections below.

3.2.7.1.1 ESD Schematic Design

1. GR551x series is powered by an independent external LDO regulator (see "Section 3.1.1 Power Supply" for details).
2. To suppress static voltages, connect a ferrite bead to each of the two charging ports (CHAR+ and CHAR-) in series, and apply a proper transient voltage suppressor (TVS) diode at each ferrite bead to found the basis of the ESD protection scheme, as shown in the figure below.

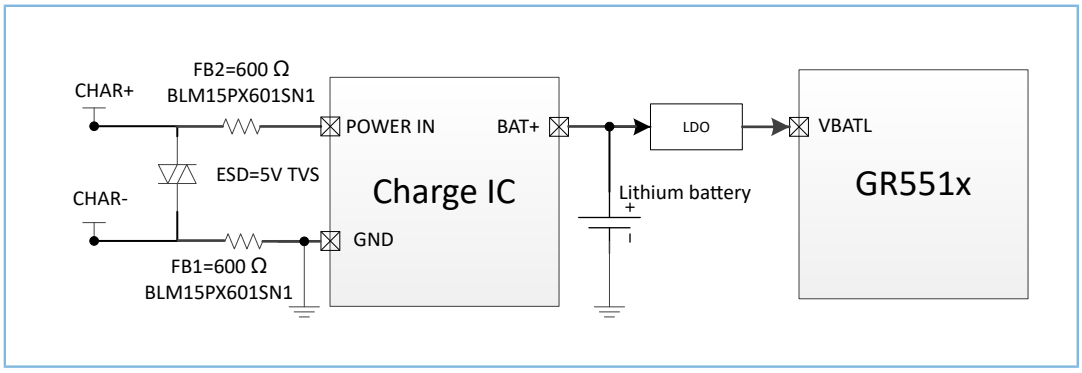


Figure 3-13 ESD protection scheme at charging ports

Recommended models of TVS diodes and ferrite beads, as well as model selection requirements, are listed in the tables below.

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Table 3-12 Model selection for TVS diodes

Parameters	Description	Min.	Typ.	Max.
V_{RwM} (V)	Reverse working maximum voltage	-	5 V	-
V_{BR} (V)	Breakdown voltage	-	7 V	-
V_{clamp} (V)	Clamp voltage	-	6 V	-
V_{ESD} (kV)	ESD prevention performance	• Contact discharge: ±10 kV • Air discharge: ±12 kV	-	-

Table 3-13 Model selection for ferrite beads

Parameters	Description	Min.	Typ.	Max.
Impedance@100 MHz (Ω)	Impedance @ 100 MHz	-	600 Ω	-
I_R (mA)	Rated operating current	-	900 mA	-
R_{DC} Max. (mΩ)	Maximum DC resistance	-	230 mΩ	-

Table 3-14 Recommended TVS diodes

Part Number	V_{RwM} (V)	V_{BR} (V)	V_{clamp} (V)	Operating Temperature	V_{ESD} (kV)	Package	Manufacturer
AZ5C25-01B	5	9	6	–55°C – 85°C	• Contact discharge: ±13 kV • Air discharge: ±16 kV	0201	Amazing Micro.
OVE38E32S1M	6.5	7	10	–55°C – 85°C	• Contact discharge: ±25 kV • Air discharge: ±25 kV	0402	OVREG

Table 3-15 Recommended ferrite beads

Part Number	Impedance @100 MHz	Rated Current	Max. DC Resistance	Operating Temperature	Package	Manufacturer
BLM15PX601SN1	600 Ω	900 mA	230 mΩ	-55°C – 125°C	0402	Murata
WLBD1005HCU601TL	600 Ω	900 mA	230 mΩ	-55°C – 125°C	0402	Walsin

3. To protect products with metal shell against ESD, connect ferrite beads between metal shell GND and the GND on motherboard.
4. To protect products such as smartwatch/wristband against ESD, when the air discharge of the system exceeds ±8 kV and contact discharge is above ±4 kV (as the target products require), additional reset mechanisms (such as watchdog timeout reset) are required to enhance ESD protection.

If an external WDT needs to be included, do not start the WDT before firmware is programmed to the SoC, to avoid inadvertent system reset.

Choose WDT that meets the requirements in Table 3-16. A recommended model series is also provided.

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Table 3-16 WDT requirements and recommended models

ESD Susceptibility	WDT Reset Time t_{WD}	WDT Output Reset Time t_{RST}	Voltage Input Range	Operating Voltage	Operating Temperature	Recommended Model	Manufacturer
HBM > 2000 V CDM > 500 V	Configurable < 10s	> 100 ms	1.6 V – 5 V	Supporting device sleep mode. Up to 5 μA is recommended.	-40°C – 85°C	SGM820A/B-X	SGMICRO

To reset the system by using SGM820 as the external WDT, the WDT timeout period can be set with an external capacitor.

Set WDT countdown value with SGM820A-X (standard):

$$t_{WD_standard}(\text{ms}) = 3.33 \times C_{CWD}(\text{nF}) + 0.28(\text{ms}) \quad (1)$$

Set WDT countdown value with SGM820B-X (extended):

$$t_{WD_extended}(\text{ms}) = 78.3 \times C_{CWD}(\text{nF}) + 51(\text{ms}) \quad (2)$$

During the reset period t_{WD}, after a feeding-dog pulse signal output (> 50 ns) occurs, the WDT is cleared and the system will not be reset; when an ESD occurs and leads to software failure, the WDT cannot be cleared during t_{WD}. In this case, the WDT generates a reset signal (200 ms) to reset the system.

A reference schematic design of the WDT is shown in Figure 3-14. Connect nRESET to GR551x Chip_EN, so that the WDT can send reset signals to reboot the system in the case of software failure; connect WDI_820 to any GPIO to feed the dog.

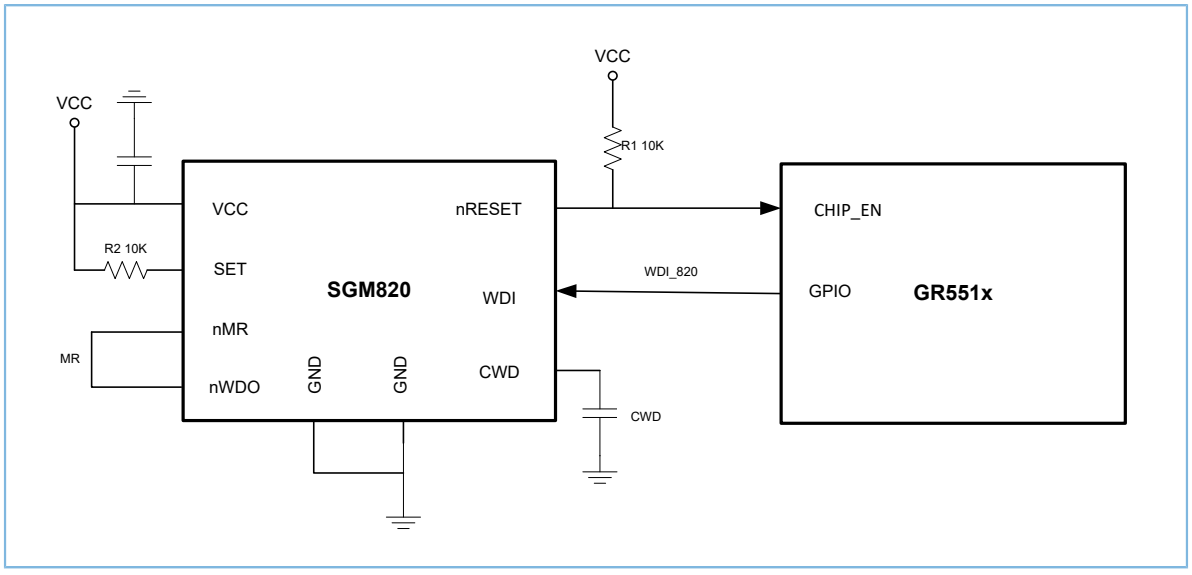


Figure 3-14 Hardware WDT schematic design (reference)

3.2.7.1.2 PCB Layout Design

1. Live by the following rules for GR551x PCB grounding:
   - PCB with four layers or above is recommended. A GR551x SoC is adjacent to the GND layer. The GND layer shall be solid and complete, so as to effectively prevent static from setting in.
   - Connect GR551x GND pin to the GND pin on the top layer, and then connect the GR551x SoC GND pin to the GND pins on the other layers through vias.
   - For GR551x in QFN packages, VSS_BUCK shall be placed close to the GND pin of the input capacitor (10 µF), and be connected to EPAD on other layers through at least two vias near VSS_BUCK. The trace from VSS_BUCK to the input capacitor should be 0.25 mm wide or above, so as to reduce power/GND loop impedance.
2. To design the layout for charging port pads,
   - It is recommended not to place pads of charging ports (CHAR+ and CHAR-) and GR551x SoC on the same layer. However, if the pads and GR551x SoC are on the same layer, a minimum distance between the two at 5 mm shall be guaranteed.
   - Pads of the charging ports shall not be placed close to ESD sensitive signals (including clock, reset, and communication signals). Those signals shall also be shielded with ground traces.
3. Place filter capacitors as close to the power pins of GR551x as possible, to keep the power return path minimal, so as to enhance filtering performance.

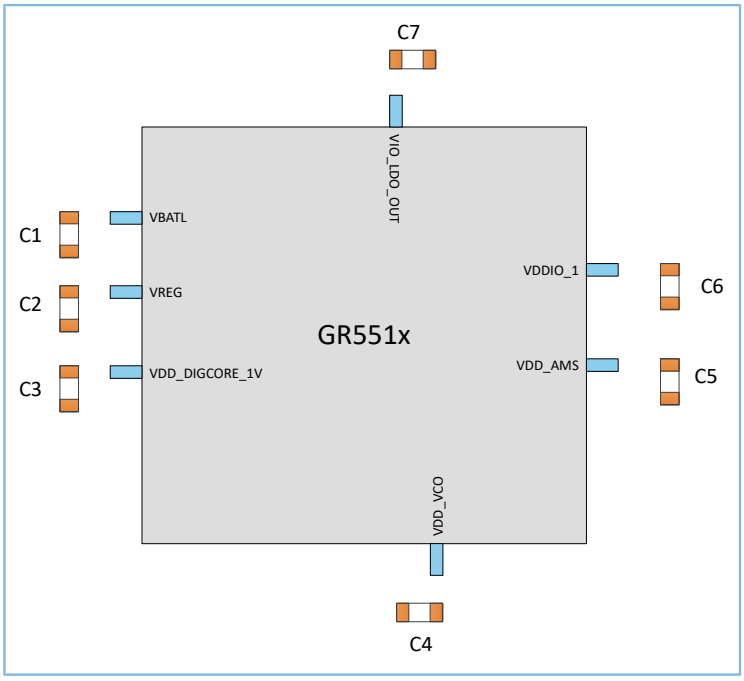


Figure 3-15 Filter capacitor layout for power supply

4. It is recommended to place communication signals neither on the top layer nor the bottom layer in the PCB stack-up, due to the ESD susceptibility of I/O pins. Avoid routing signals susceptible to ESD events (such as clocks and reset pins) at the edge of the board. It is recommended to shield the I/O pins and ESD susceptible signals with GND traces.

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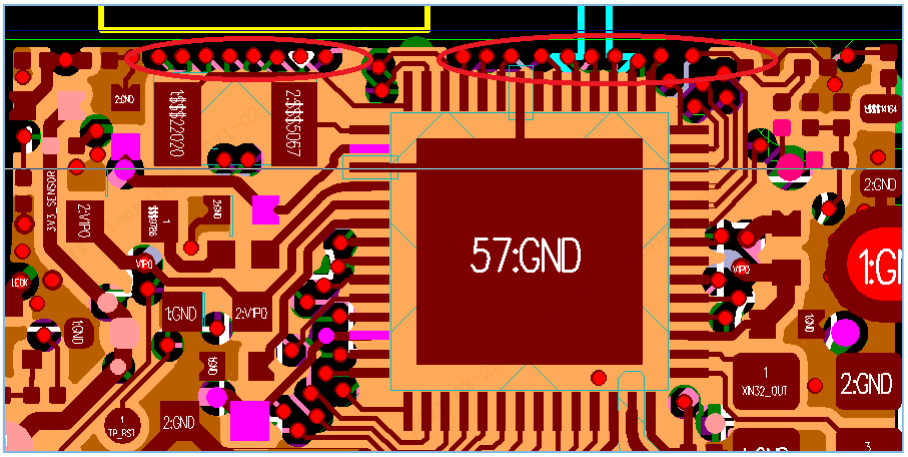


Figure 3-16 Improper I/O routing at board edge (not shielded by GND traces)

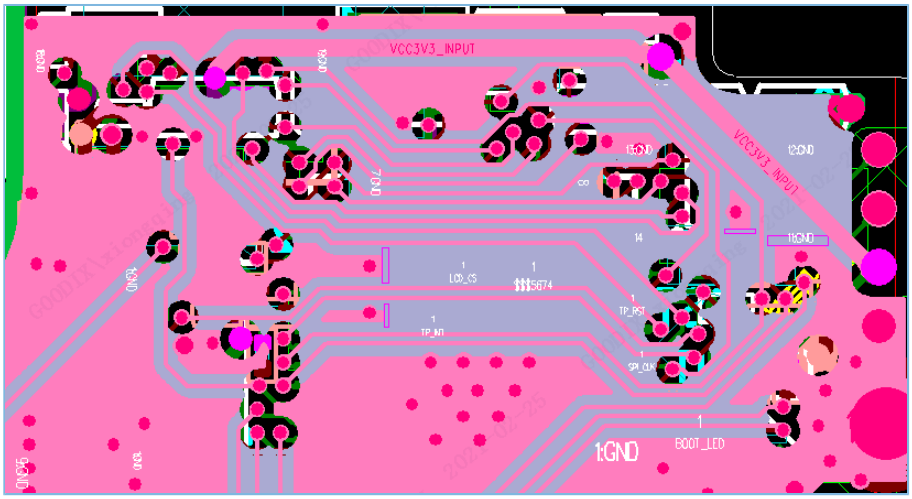


Figure 3-17 Proper routing of I/O pins

5. The capacitors or ESD protection devices should be routed through the pad. Using long wires to connect the capacitors/ESD protection devices to pad undermines filtering/protection performance, and is therefore not recommended.

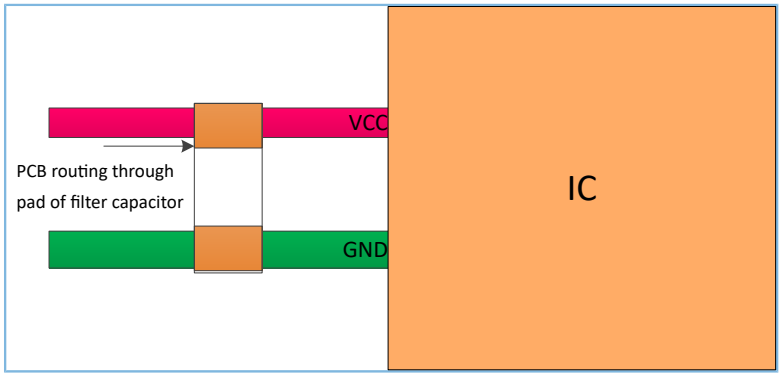


Figure 3-18 Proper routing for a capacitor (as an example)

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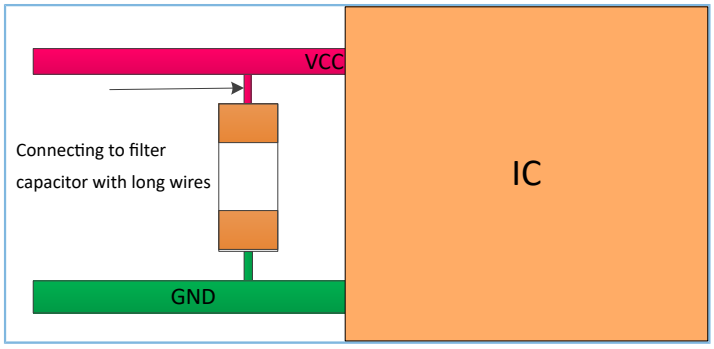


Figure 3-19 Improper routing for a capacitor (as an example)

3.2.7.1.3 Product Structural Design

- Shell gaps shall be sealed to prevent static electricity from setting in.
- Connect ferrite beads in series to the GND pins on the metal shell, and connect the GND pins to the GND circuit on the motherboard, to protect the motherboard from static electricity transmitted through the metal shell.
- Suspended metal structure is not allowed. The steel stiffener of sensors (such as touch/display sensors) shall be grounded.
- Try to avoid close contact between the overlapped area between the FPC on the motherboard and the FPC on touch/display sensor module. It is recommended to apply heat resistant adhesives on the exposed area of motherboard connectors, to prevent short circuit or static electricity from setting in.

3.2.7.2 ESD Considerations in Production, Transport, and Debugging

To steer away from ESD events, stringent ESD control is also required during production, transport, debugging, and other relevant phases.

- Wear antistatic wrist strap in these processes. Touching the SoC with bare hands or using metal tweezers is forbidden.
- Use an antistatic bag/tray to hold the SoC.
- Countermeasures against ESD are essential for soldering irons, welding tables, and test instruments.
- Strictly comply with ESD preventive requirements for the production line during production and transport.

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4 Reference Design

4.1 Reference Schematic Diagram

Figure 4-1 is the reference schematic for GR5515IGND QFN56 package.

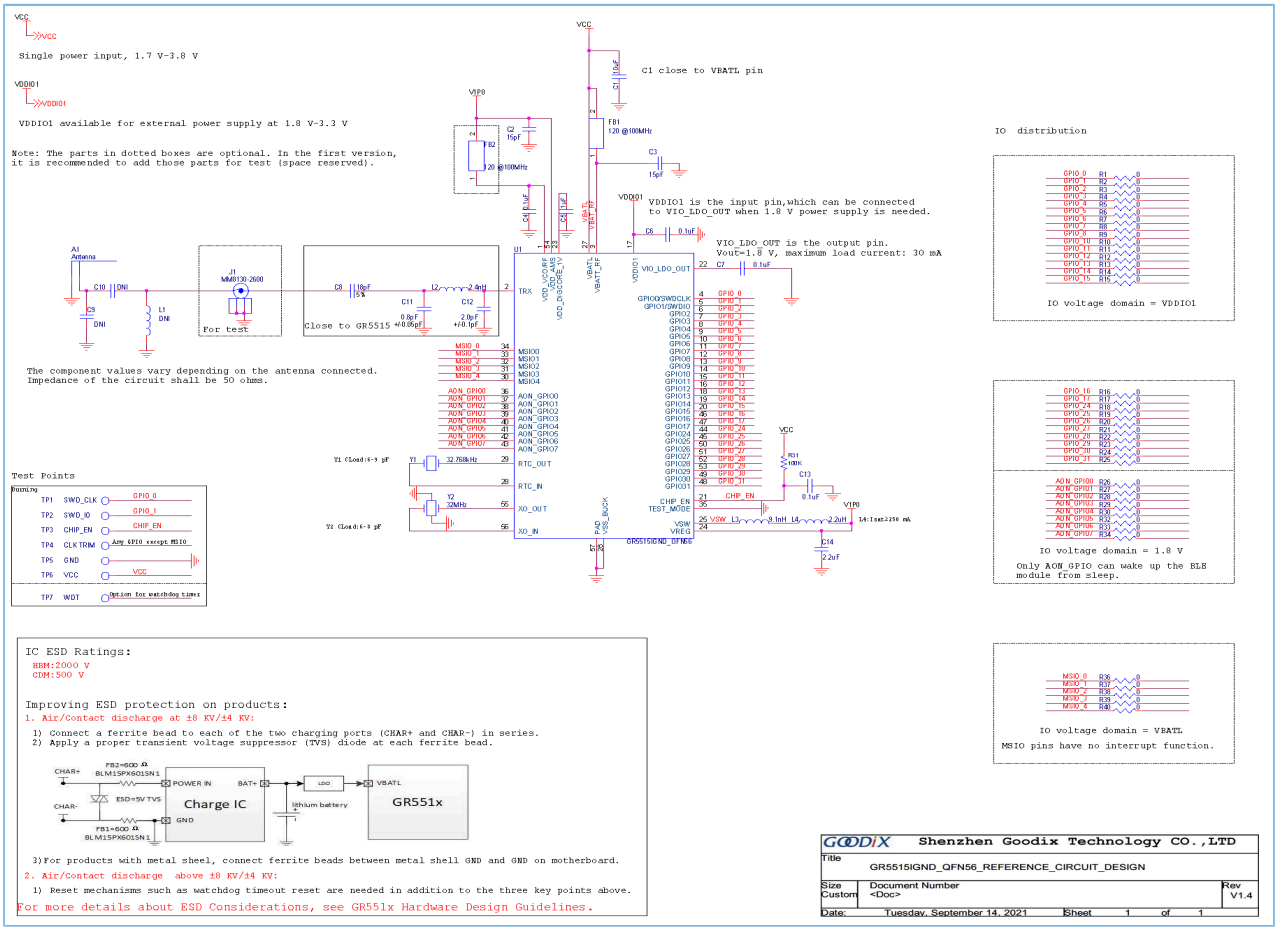


Figure 4-1 Reference schematic for GR5515IGND QFN56 package

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Figure 4-2 is the reference schematic for GR5515IENDU QFN56 package.

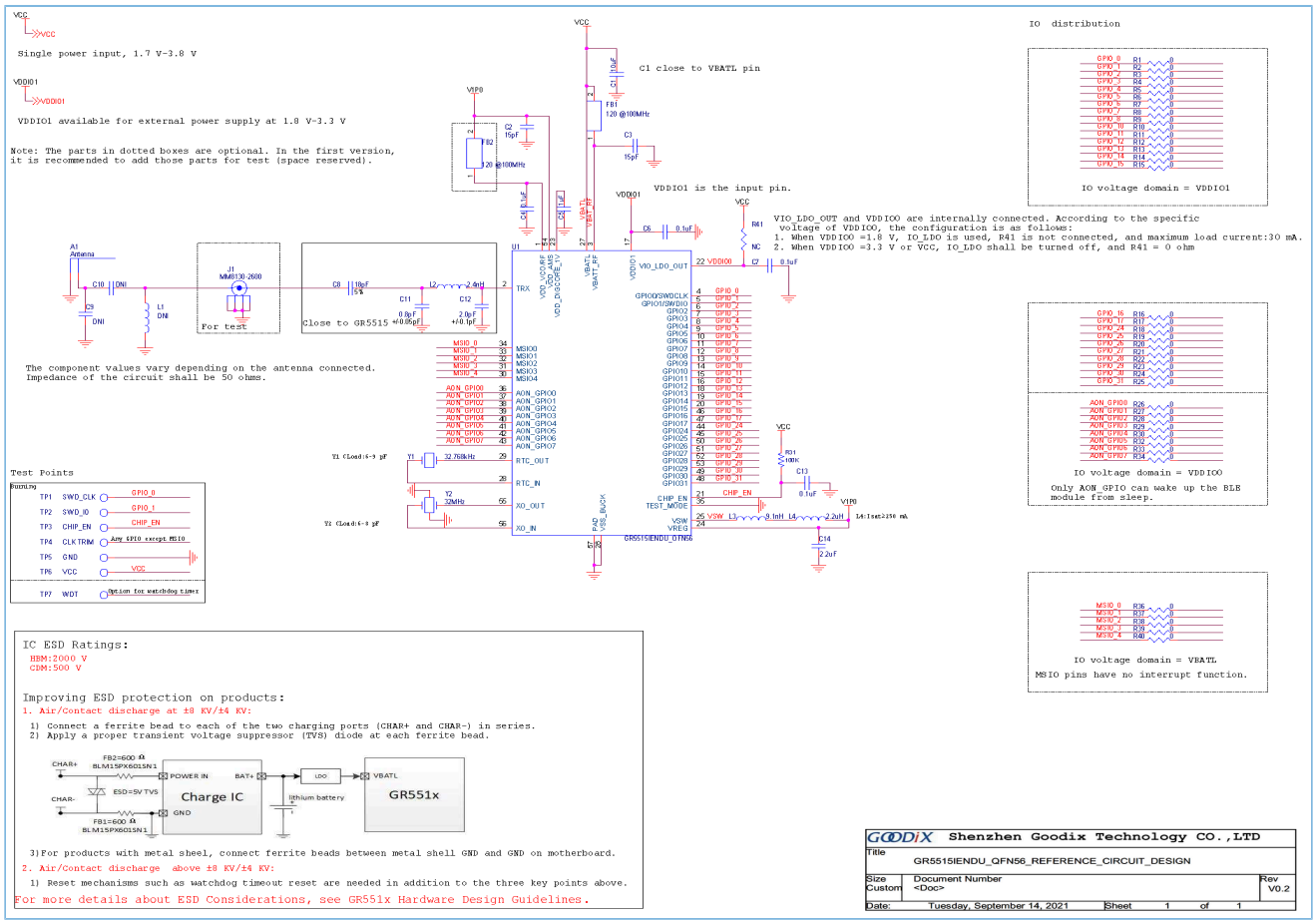


Figure 4-2 Reference schematic for GR5515IENDU QFN56 package

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Figure 4-3 is the reference schematic for GR5515I0ND QFN56 package.

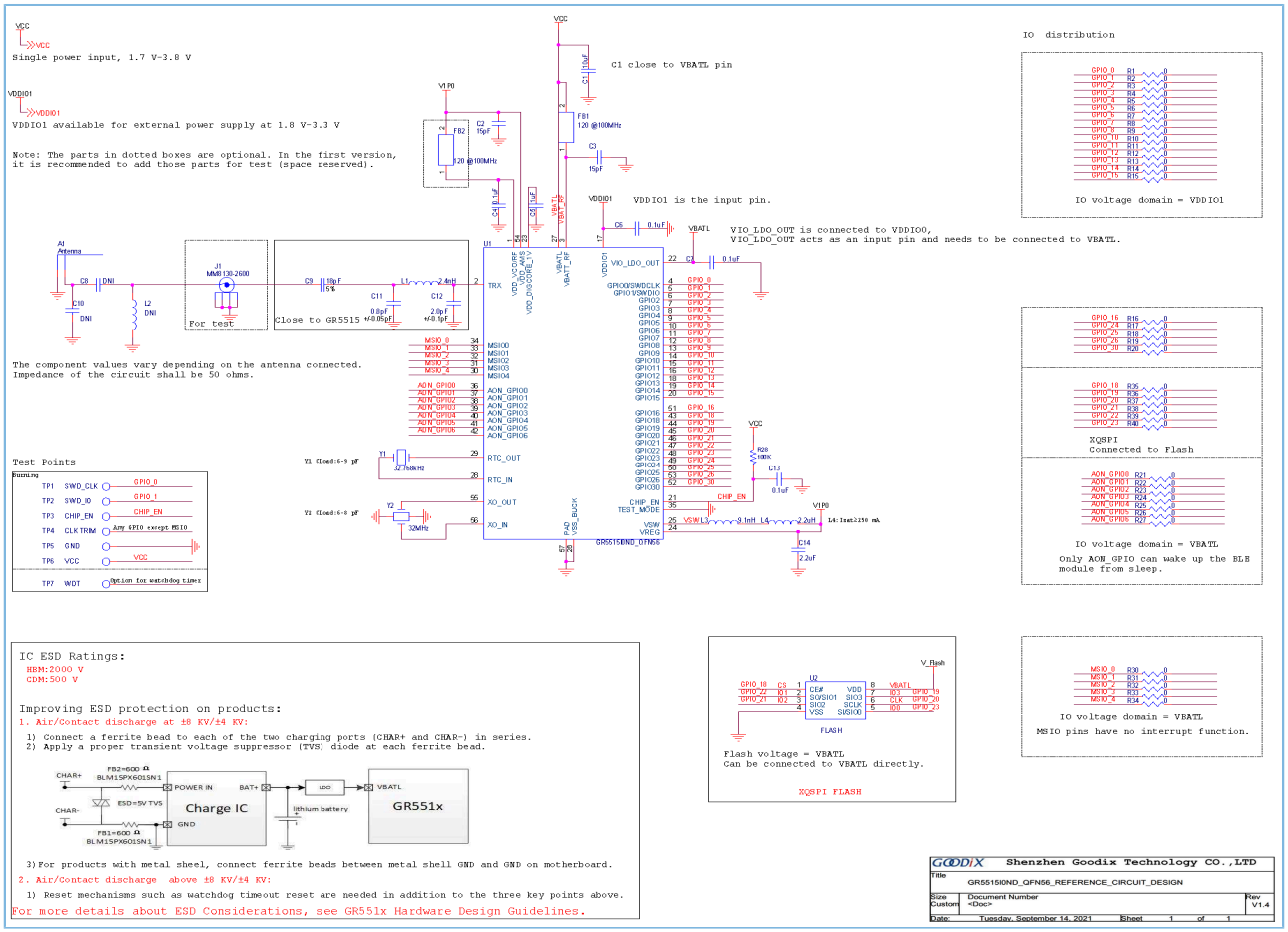


Figure 4-3 Reference schematic for GR5515I0ND QFN56 package

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Figure 4-4 is the reference schematic for GR5515I0NDA QFN56 package.

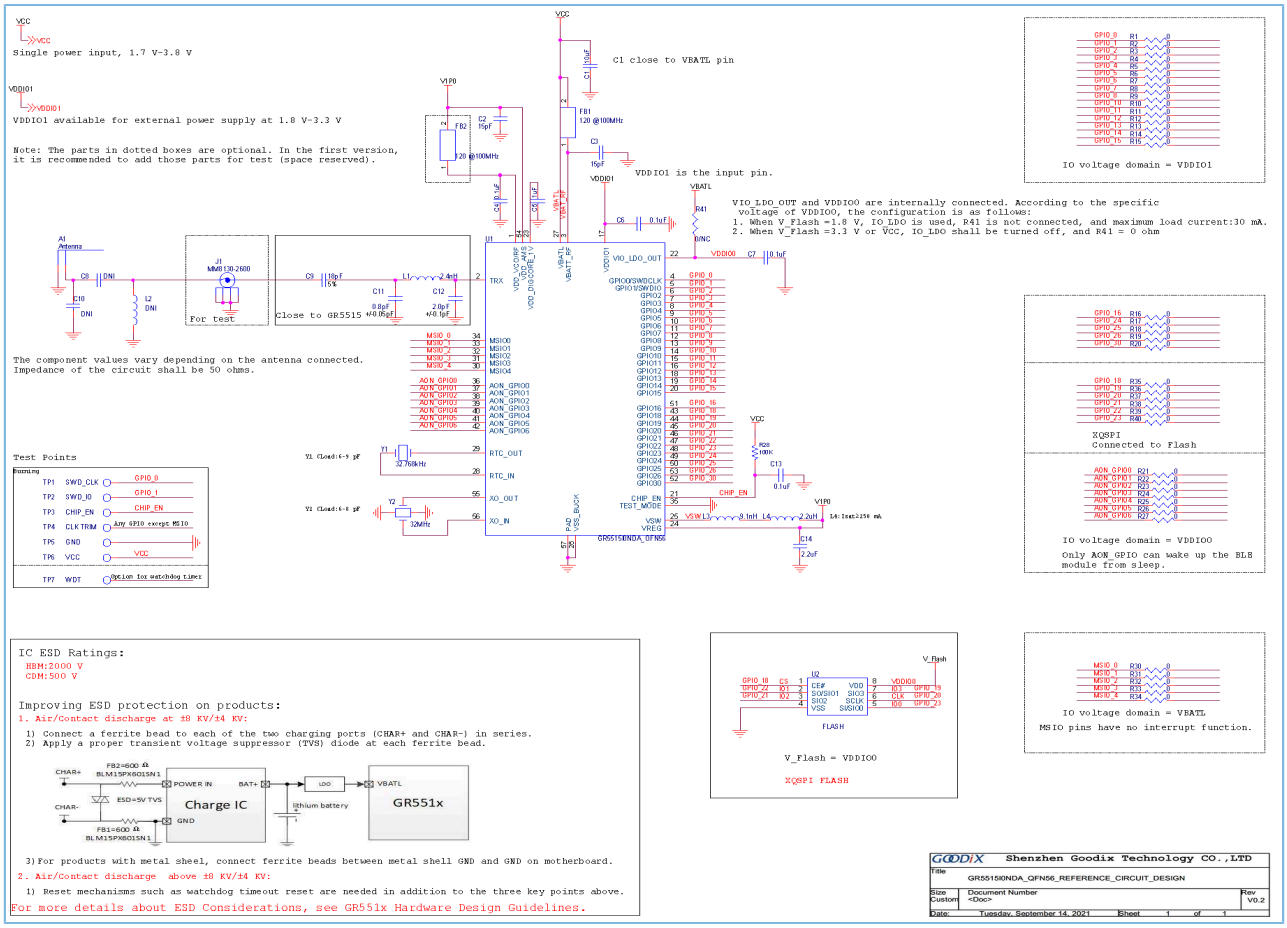


Figure 4-4 Reference schematic for GR5515I0NDA package

Figure 4-5 is the reference schematic for GR5515RGBD BGA68 package (NRND).

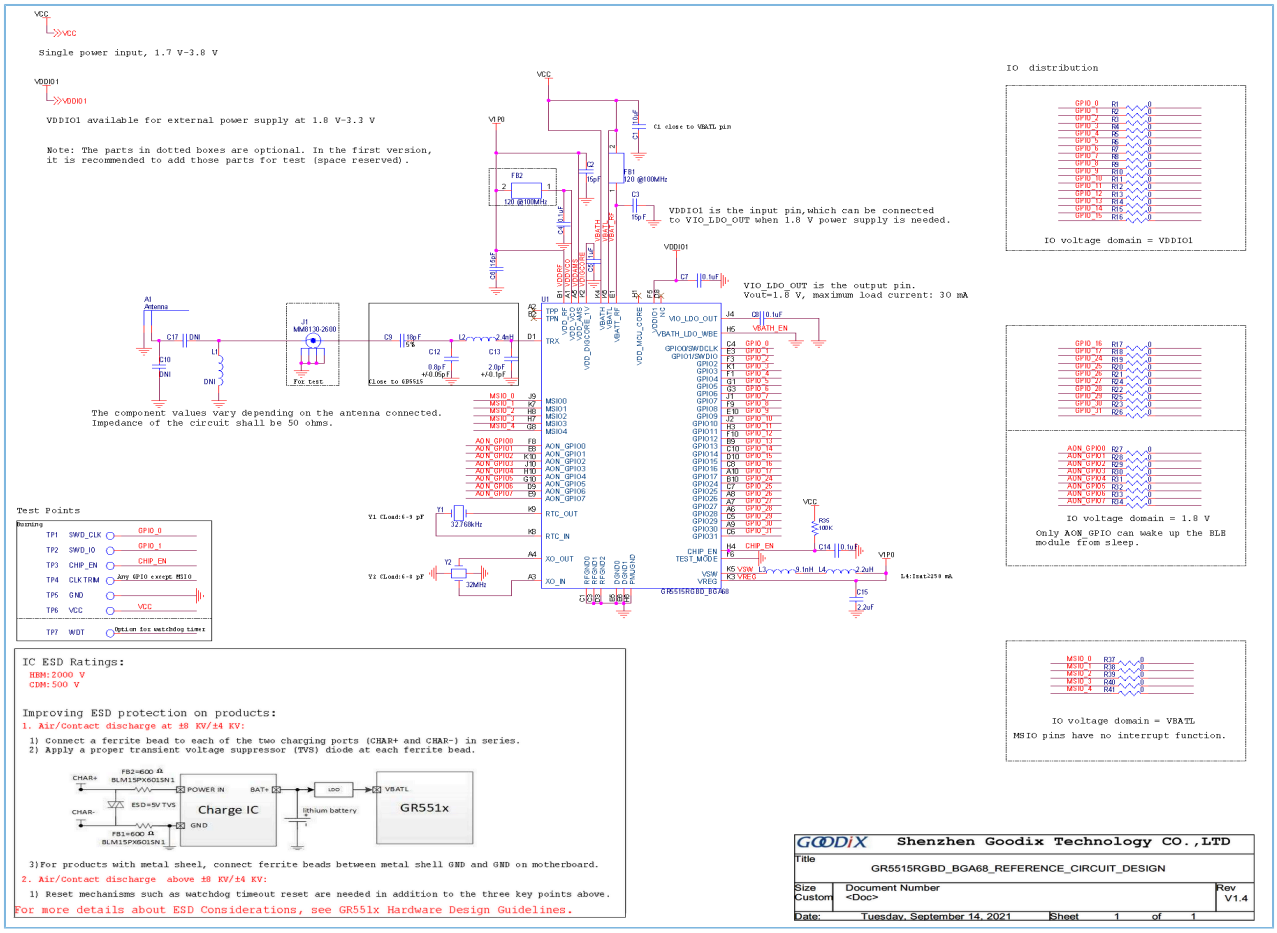


Figure 4-5 Reference schematic for GR5515RGBD BGA68 package (NRND)

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Figure 4-6 is the reference schematic for GR5515GGBD BGA55 package.

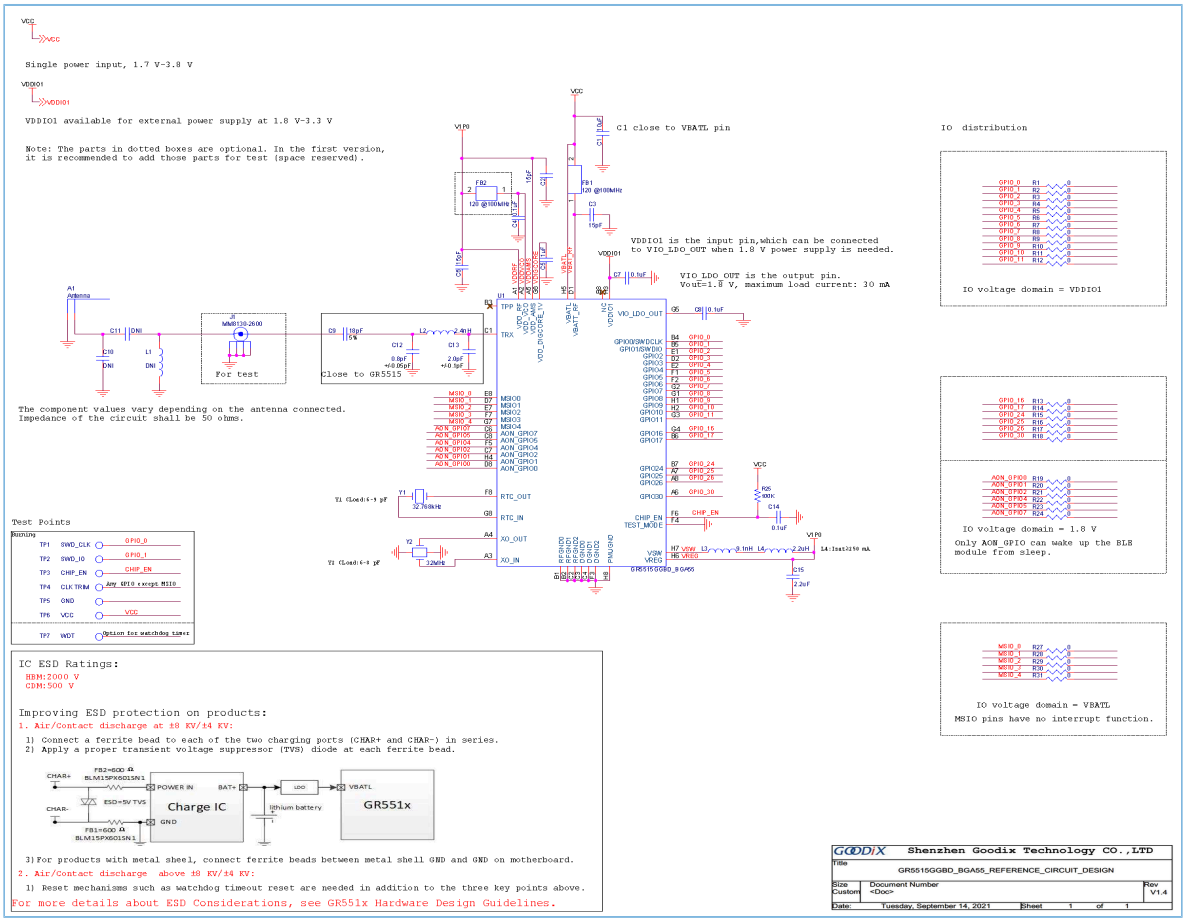


Figure 4-6 Reference schematic for GR5515GGBD BGA55 package

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Figure 4-7 is the reference schematic for GR5513BEND QFN40 package.

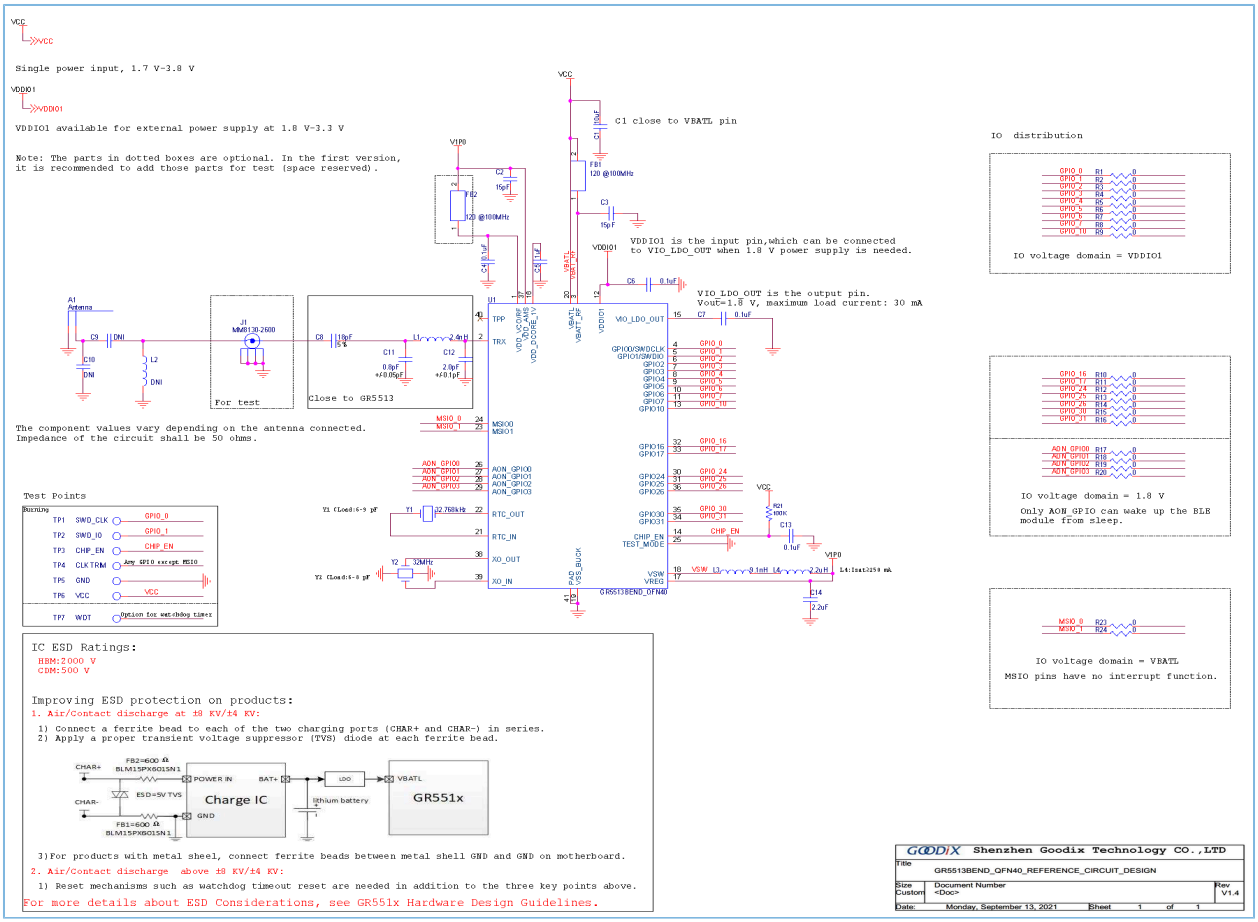


Figure 4-7 Reference schematic for GR5513BEND QFN40 package

Figure 4-8 is the reference schematic for GR5513BENDU QFN40 package.

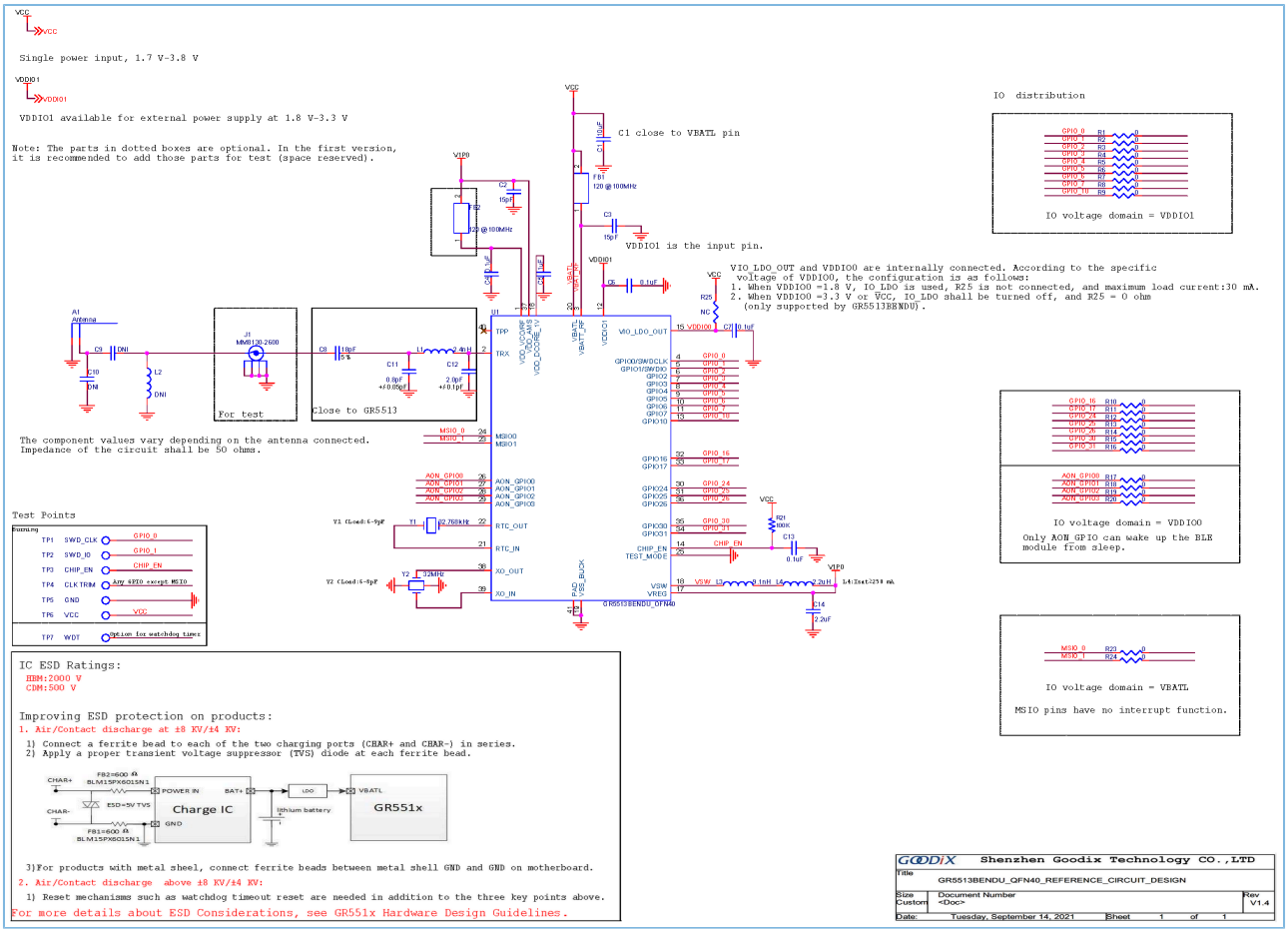


Figure 4-8 Reference schematic for GR5513BENDU QFN40 package

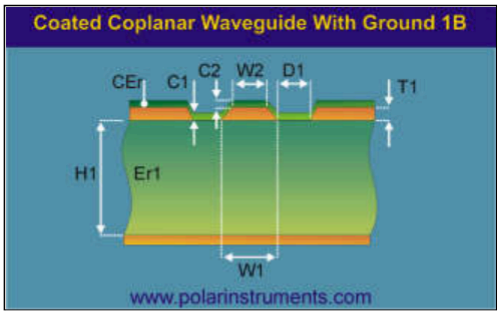
4.2 PCB Layout Reference Design

In accordance with rules specified in “Section 3.2 PCB Design and Layout Guideline”, this section provides two reference designs for PCB layout for the GR551x minimal system by taking SoCs mounting BGA68 and QFN56 packages as examples, to help users quickly get started with product development and design.

4.2.1 Four-layer PCBs in QFN56 Package

In this reference design, all GPIO signals are available as output. The 0.6 mm PCB is composed of four layers with plated through holes (PTHs). The RF route is 22 mil wide, which is the same with the component pad. To ensure the impedance of the RF route is not higher than 50 Ω, provide openings on the second layer, and use the third layer (PCB layer stackup: 0.6 mm, impedance: up to 50 Ω, as shown in Figure 4-9) as the reference plane.

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				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	14.6000	+/-	0.0000	14.6000	14.6000
Substrate 1 Dielectric	Er1	4.2000	+/-	0.0000	4.2000	4.2000
Lower Trace Width	W1	22.0000	+/-	0.0000	22.0000	22.0000
Upper Trace Width	W2	21.0000	+/-	0.0000	21.0000	21.0000
Ground Strip Separation	D1	11.0000	+/-	0.0000	11.0000	11.0000
Trace Thickness	T1	1.2000	+/-	0.0000	1.2000	1.2000
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000
Coating Dielectric	CEr	4.2000	+/-	0.0000	4.2000	4.2000
Impedance	Zo	50.33		------	50.33	50.33
Delay (ps/in)	D	148.357		------	148.357	148.357
Inductance (nH/in)	L	7.466		------	7.466	7.466
Capacitance (pF/in)	C	2.948		------	2.948	2.948

Figure 4-9 Impedance control details for the 4-layer PCB (QFN56)

Details for the PCB layout reference design are provided below.

1. Top layer

   This layer is used for component layout and routing of key signals such as RF.

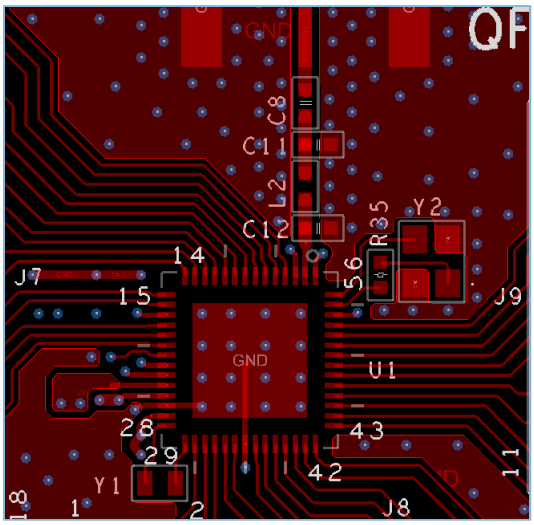


Figure 4-10 Top layer design for 4-layer PCB (QFN56)

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2. L2

This is the ground layer for returned signals. In the reference design, an opening is provided on L2 underneath the 50 Ω RF transmission line, and another two openings are provided underneath the signal output pads of the 32 MHz crystal to reduce parasitic capacitance. L3 acts as the reference ground where openings are provided on L2.

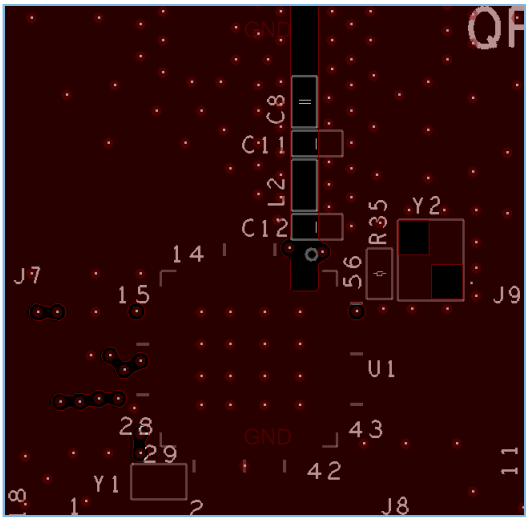


Figure 4-11 L2 design for 4-layer PCB (QFN56)

3. L3

This layer is used for the power and a small number of routes. In the reference design, L3 is used as the reference ground layer for the RF transmission line, and therefore the part underneath the RF transmission line shall be complete.

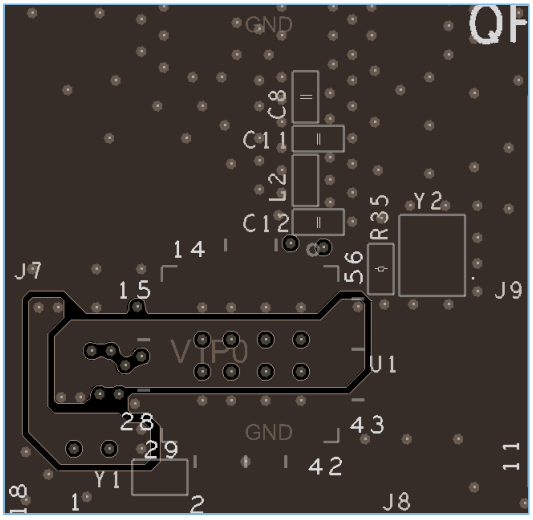


Figure 4-12 L3 design for 4-layer PCB (QFN56)

4. Bottom layer

This layer is used for filter components layout and signal routing. Filter components should be as close to the corresponding IC pins as possible.

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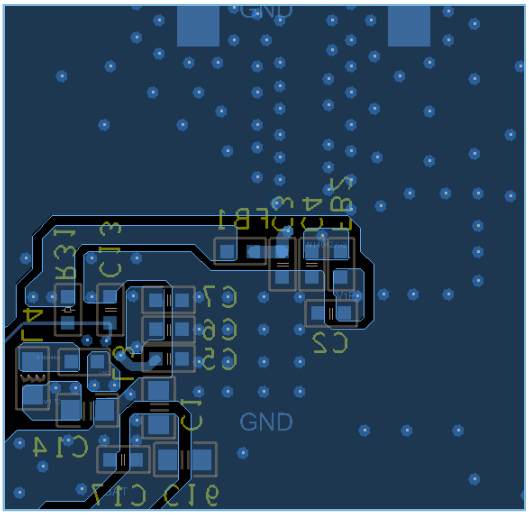


Figure 4-13 Bottom layer design for 4-layer PCB (QFN56)

4.2.2 Two-layer PCBs in QFN Packages

To reduce costs, users can design two-layer PCBs in QFN packages. In such case, due to the absence of a ground layer between the two layers, special attention should be paid to the two-layer PCB layout, especially for applications requiring high performance in ESD protection and radiation compliance. Strictly follow the PCB design rules in "Section 3.2 PCB Design and Layout Guideline". Most importantly, make sure power filter capacitors are placed close to power pins, and connection to the GND return path should be enhanced.

Details for the PCB layout reference design are provided below.

1. Try to place components and routing on the top layer only (as shown in Figure 4-14, the top layer is used for component layout and routing of key signals such as RF), so that the bottom layer can be as complete as possible.

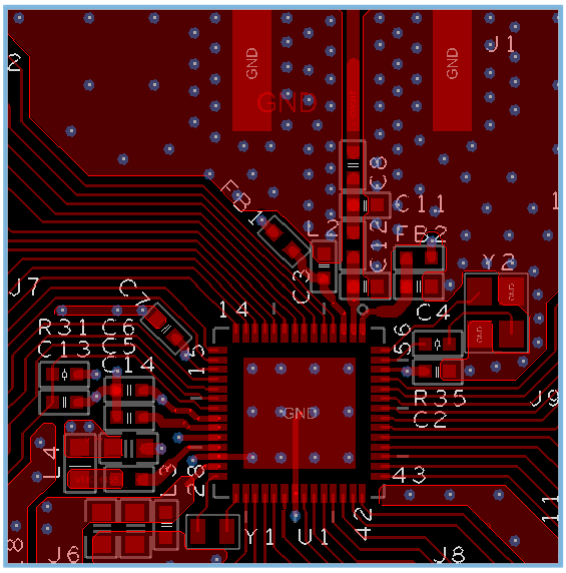


Figure 4-14 Top layer design for 2-layer PCB

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2. The figure below is a reference design for power and GND routing (taking PCB in QFN40 package as an example). The GND vias circled in yellow are used for return paths of power and RF signals, and shall be connected to the heat dissipation pad with short, wide traces through copper pour areas on the bottom layer (indicated by the green arrows in Figure 4-15).

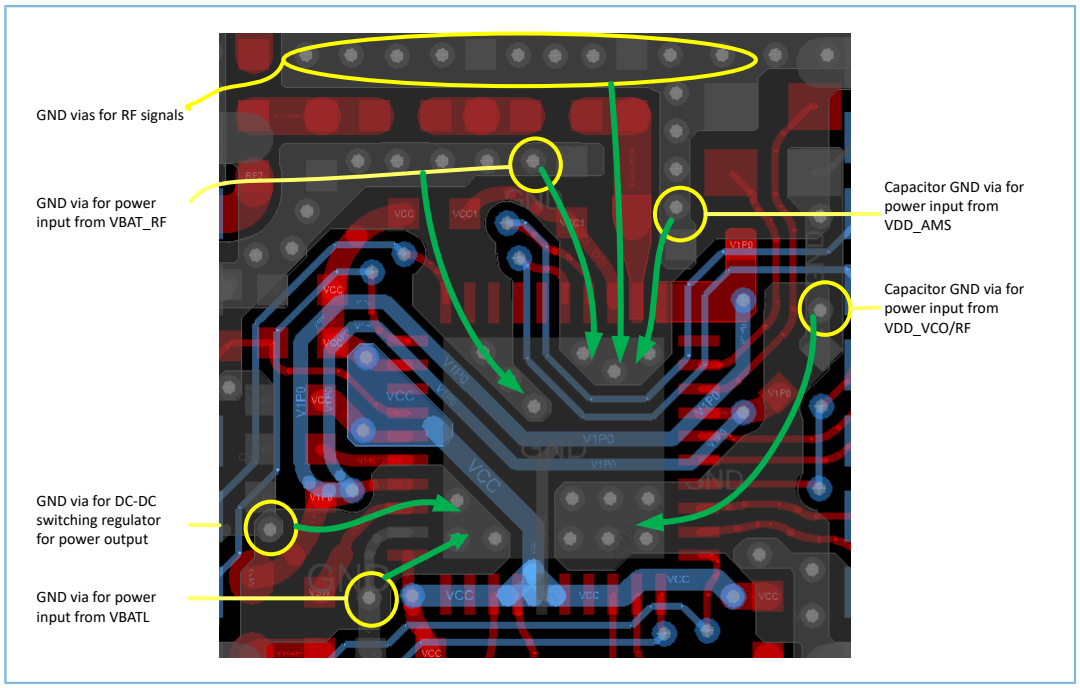


Figure 4-15 Power and GND routing reference design for 2-layer PCB (QFN40)

4.2.3 External Flash Connection for GR5515I0ND/GR5515I0NDA

GR5515I0ND/GR5515I0NDA uses external QSPI Flash with clock frequency up to 64 MHz. To avoid crosstalk from other signals, the Flash shall be as close to the IC as possible to minimize the QSPI route. QSPI route lengths should be matched, with the tolerance within 50 mil.

Figure 4-16 is a reference design for the PCB layout of GR5515I0ND/GR5515I0NDA.

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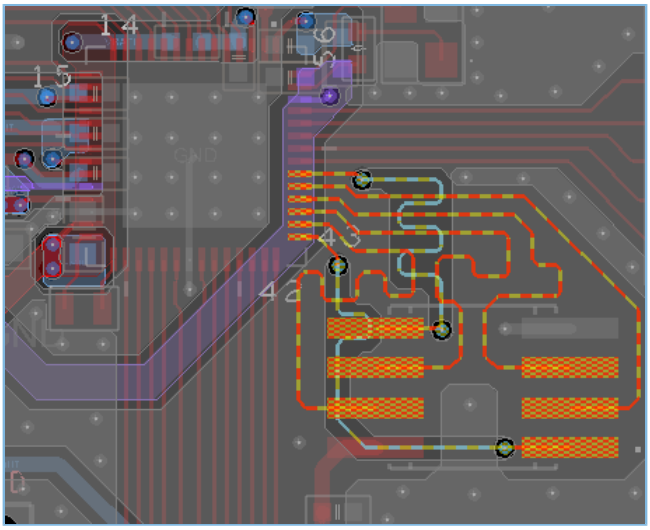


Figure 4-16 Reference design for GR5515I0ND/GR5515I0NDA PCB layout

4.2.4 Four-layer PCBs in BGA68 Package (NRND)

In this reference design, all GPIO signals are used as output. The 1.6 mm PCB is composed of four layers with PTHs. The RF route is 22 mil wide, which is the same with the component pad. As specified in "Section 3.2.1 PCB Layer Stackup", L2 is used as the reference plane for the 50 Ω RF transmission line.

Details for the PCB layout reference design are provided below.

1. Top layer

   This layer is used for component layout and routing for key signals such as RF.

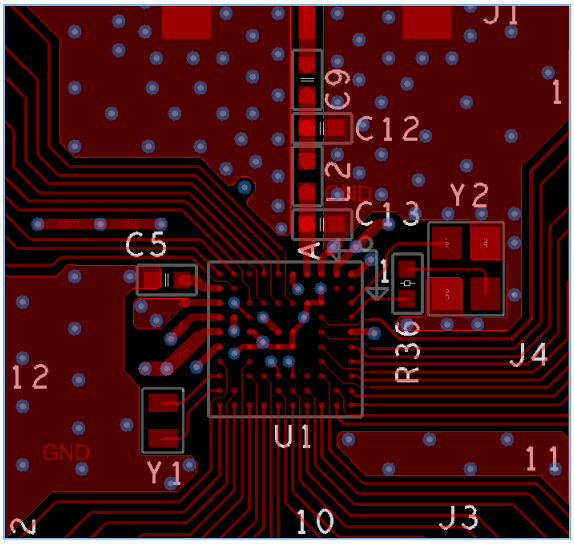


Figure 4-17 Top layer design for 4-layer PCB (BGA68)

2. L2

   This is the reference ground plane for the ground return path of the 50 Ω RF transmission line. Two openings are provided underneath the signal output pads of the 32 MHz crystal on L2, to reduce the parasitic load capacitance of the crystal.

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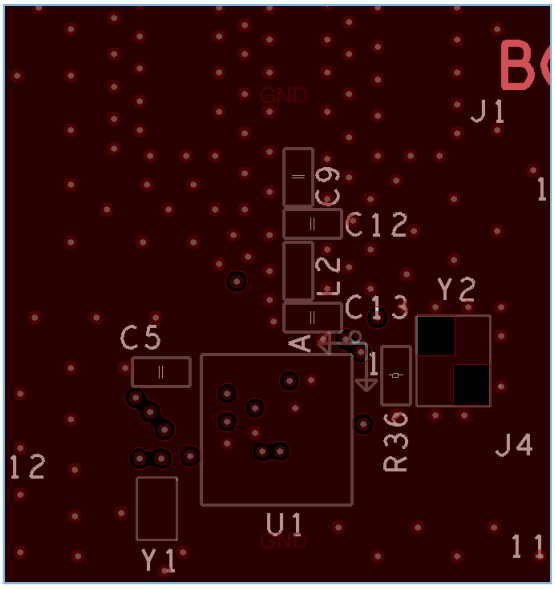


Figure 4-18 L2 design for 4-layer PCB (BGA68)

3. L3

This layer is used to split power domains and place a small number of signal lines.

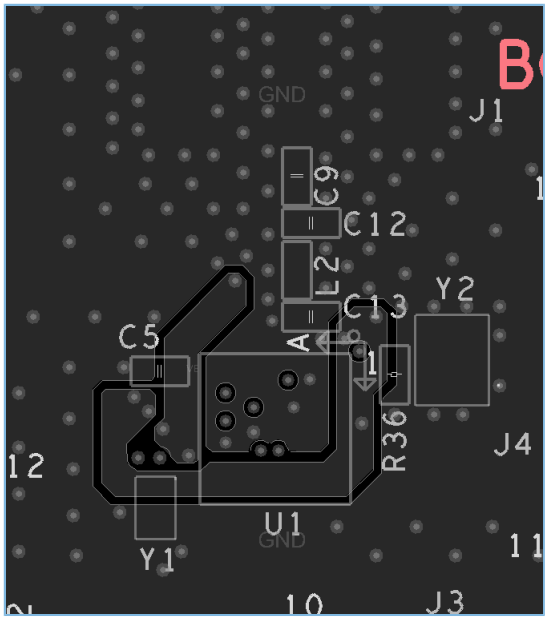


Figure 4-19 L3 design for 4-layer PCB (BGA68)

4. Bottom layer

This layer is used for filter components layout and signal routes. Filter components should be as close to the corresponding IC pins as possible.

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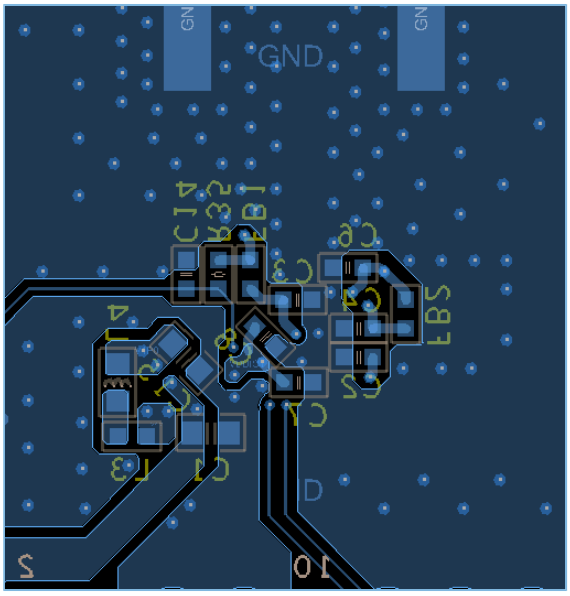


Figure 4-20 Bottom layer design for 4-layer PCB (BGA68)

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5 FAQ

5.1 Why Is the Power Consumption in GR551x Sleep Modes High?

- Description

  In power consumption tests, the power consumption of GR551x when in sleep mode varies depending on different I/O pin configurations. How to properly configure I/O pins before GR551x goes to sleep?

- Issue Analysis

  The power consumption of GR551x in sleep mode is high, and it may be because I/O pins are not properly configured.

  - I/O pins are at floating state.
  - I/O pins are configured in improper pull-up or pull-down state.

  Above incorrect configurations can cause system leakage, so you need to properly configure the state of I/Os before GR551x enters sleep mode.

- Solution

  Configure the state of I/O pins before GR551x enters sleep mode.

  - If an I/O pin is in pull-up/pull-down state or used as a driver output, it needs no pull-up/pull-down configuration.
  - If an I/O pin is not used or works in input mode without pull-up or pull-down, it needs to be configured to internal pull-down.

For sleep mode configurations, see *GR551x Sleep Mode and Power Consumption Measurement Application Note*.

5.2 Can the RF PI Circuits Be Simplified or Removed?

- Description

  In designing a PCB, can I modify the recommended RF PI circuit layout due to limited space?

- Issue Analysis

  GR551x recommends two PI circuits for RF: a PI circuit close to GR551x and a PI circuit close to the antenna. Whether these two PI circuits can be simplified or removed needs to be treated differently.

- Solution

  The PI circuit close to GR551x is used to match GR551x internal PA and cannot be removed. It cannot be simplified also as its inductance and capacitance values must be kept consistent with the recommended circuit. The impedance of the RF channel from the GR551x PI is 50 Ω and compatible with any 2.4 GHz antenna (2400 MHz to 2484 MHz) that supports Bluetooth products.

  The PI circuit close to the antenna end is used to match the antenna, and its circuit can be changed according to the antenna you use. For the matching of the antenna, you can complete simple matching adjustment by the S11 parameter or the Smith chart from the vector network analyzer. However, for matching of other indicators (such as antenna gain and directionality), you are recommended to seek help from professional antenna factories.

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6 Glossary

Table 6-1 Glossary

Name	Description
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AMS	Analog Mix Signal
BB	Baseband
BGA	Ball Grid Array Package
Bluetooth LE	Bluetooth Low Energy
BUCK	Type of DC-DC Converter
DC-DC	DC-to-DC Converter
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
Tg	Glass Transition Temperature
GPIO	General-Purpose Input/Output
LDO	Low-dropout
LNA	Low Noise Amplifier
NRND	Not Recommended for New Designs
PLL	Phase-Locked Loop
PMU	Power Management Unit
PCB	Printed Circuit Board
PTH	Plated Through Hole
QFN	Quad Flat No-Lead Package
QSPI	Queued Serial Peripheral Interface
RoHS	Restriction of Hazardous Substances Directive
SDK	Software Development Kit
SOC	System-on-Chip
SPI	Serial Peripheral Interface
SVHC	Substance of Very High Concern
SWD	Serial Wire Debug
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
XO	Crystal Oscillator

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7 Appendix: QFN and BGA Assembly Guideline

The QFN and BGA packages are qualified to MSL3 and are RoHS/green compliant. RoHS is the abbreviation of *Restriction of Hazardous Substances Directive*, which puts a limit on the amount of harmful substances in electronic devices, published by European Union in February 2003. MSL3 represents Moisture Sensitivity Level 3 which indicates that a moisture sensitive plastic device, once removed from a dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH before the solder reflow process.

GR551x storage conditions:

- Temperature: < 40°C
- Humidity: < 90% RH
- Period: 12 months

After opening the package: go through reflow for board assembly within 48 hours.

- Temperature: < 30°C
- Humidity: < 60% RH
- Stored at: < 10% RH

In BGA55 package outlines (as shown in "Section 7.1.3 BGA55"), both lead-free solder and Sn/Pb solder applications use the same rules for the general PCB design. Only the board surface finish and the board material have to be considered for lead-free application due to the higher reflow temperature and lead-free solder compatibility. A number of factors may have a significant effect on mounting QFN or BGA packages on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in exposed ground/thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow temperature profile.

Note:

It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort may be needed to optimize the process as per users' surface mount practices and requirements.

In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

Typically, the PCB pad pattern for an existing package is designed based on guidelines developed within a company or by following industry standards such as IPC-SM-782. For the purpose of this document, methodology of Association Connecting Electronics Industries (IPC) is used here for designing PCB pad pattern. However, because of exposed die paddle and the package lands on the bottom side of the package of GR551x, certain constraints are added to IPC's methodology. The pad pattern developed here includes considerations for lead and package tolerances.

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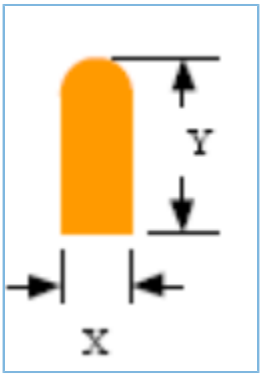


Figure 7-1 Land on the bottom side of the package

For the PCB pad design for GR551x QFN56 package (7 mm x 7 mm, 0.4 mm pitch), it is recommended to set X = 0.25 mm and Y = 0.75 mm. The pads may also be rounded on the inner edge. Maximum pad width is set to 0.25 mm to avoid solder bridging.

It is recommended to use non-solder-mask defined (NSMD) pads. For 0.4 mm pitch parts with PCB pad width of 0.25 mm, not enough space is available for solder mask web in between the pads in GR551x QFN56 package. In such cases, it is recommended to use “Trench” type solder mask opening where a big opening is designed around all pads on each side of the package with no solder mask in between the pads, as shown in Figure 7-2.

Note:

The inner edge of the solder mask should be rounded, especially for corner leads to allow for enough solder mask web in the corner area.

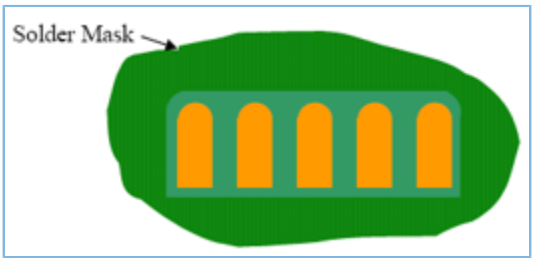


Figure 7-2 Solder mask definition for perimeter lands for 0.4 mm pitch parts

7.1 Package Information

GR551x offers QFN56, BGA68, BGA55, and QFN40 packages to support different environmental requirements.

7.1.1 QFN56

GR551x QFN56, including GR5515IGND QFN56, GR5515IENDU QFN56, GR5515I0ND QFN56, and GR5515I0NDA QFN56, is a 56-pin and 7 x 7 x 0.75 (mm) QFN package. It is qualified for MSL3.

Table 7-1 QFN56 package information

Parameter	Value	Unit	Tolerance
Package Size	7 x 7	mm	±0.1 mm

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Parameter	Value	Unit	Tolerance
QFN Pad Count	56		
Total Thickness	0.75	mm	±0.05 mm
QFN Pad Pitch	0.40		
Pad Width	0.20		
Exposed Pad Size	5.2 x 5.2		±0.1 mm

The Figure 7-3 shows the QFN56 package outlines.

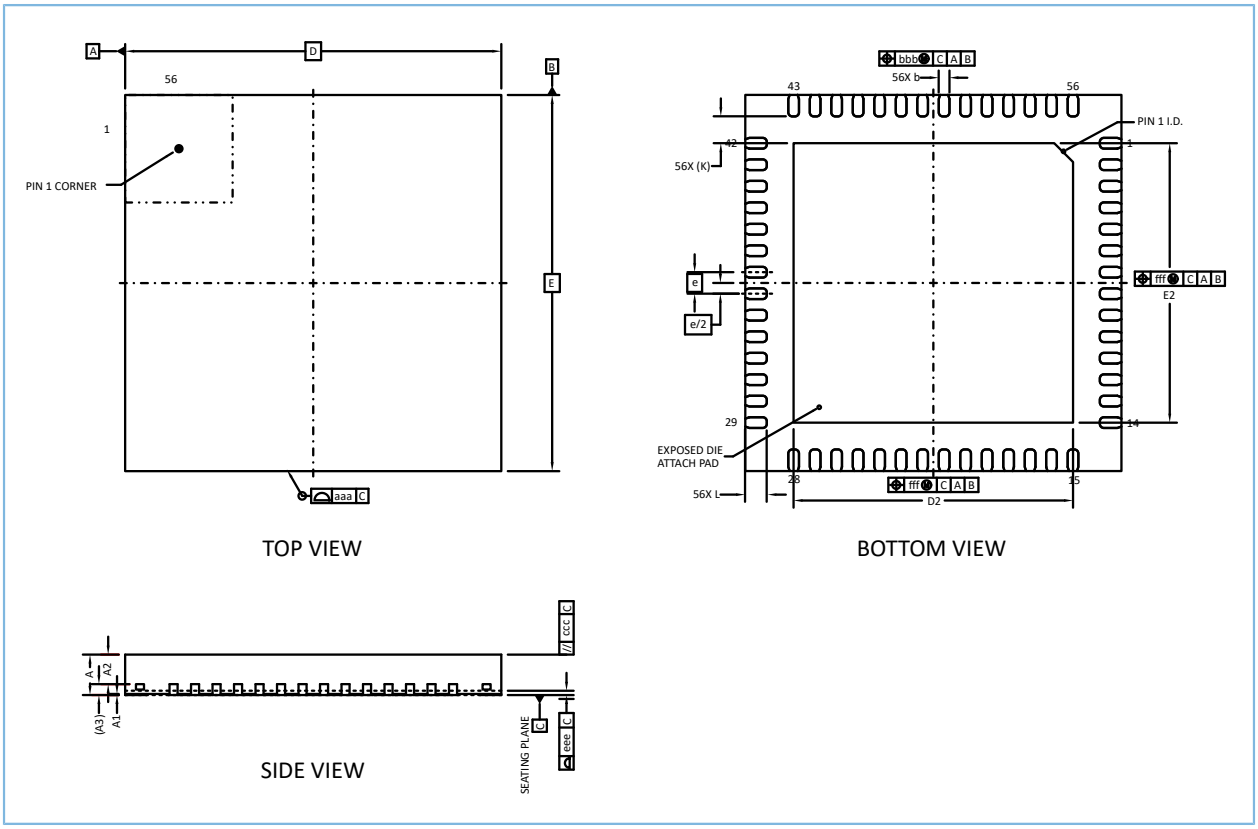


Figure 7-3 QFN56 package outlines

Note:

Drawing is not to scale.

Table 7-2 QFN56 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.550	-	-	0.022	-

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Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	7.000 BSC.			0.276 BSC.		
E	7.000 BSC.			0.276 BSC.		
e	0.400 BSC.			0.016 BSC.		
D2	5.100	5.200	5.300	0.201	0.205	0.209
E2	5.100	5.200	5.300	0.201	0.205	0.209
L	0.300	0.400	0.500	0.012	0.016	0.020
K	0.500 REF.			0.020 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

Refer to *JEDEC standard J-STD-020* for relevant soldering information.

7.1.2 BGA68 (NRND)

GR551x BGA68, including GR5515RGBD BGA68, is a 68-pin and 5.3 x 5.3 x 0.88 (mm) package. It is qualified for MSL3.

Table 7-3 BGA68 package information

Parameter	Value	Unit	Tolerance
Package Size	5.3 x 5.3	mm	±0.1 mm
BGA Ball Count	68		
Total Thickness	0.88	mm	±0.1 mm
BGA Ball Pitch	0.50		
Ball Diameter	0.25		
Ball Height	0.18		

Figure 7-4 below shows the BGA68 package outlines.

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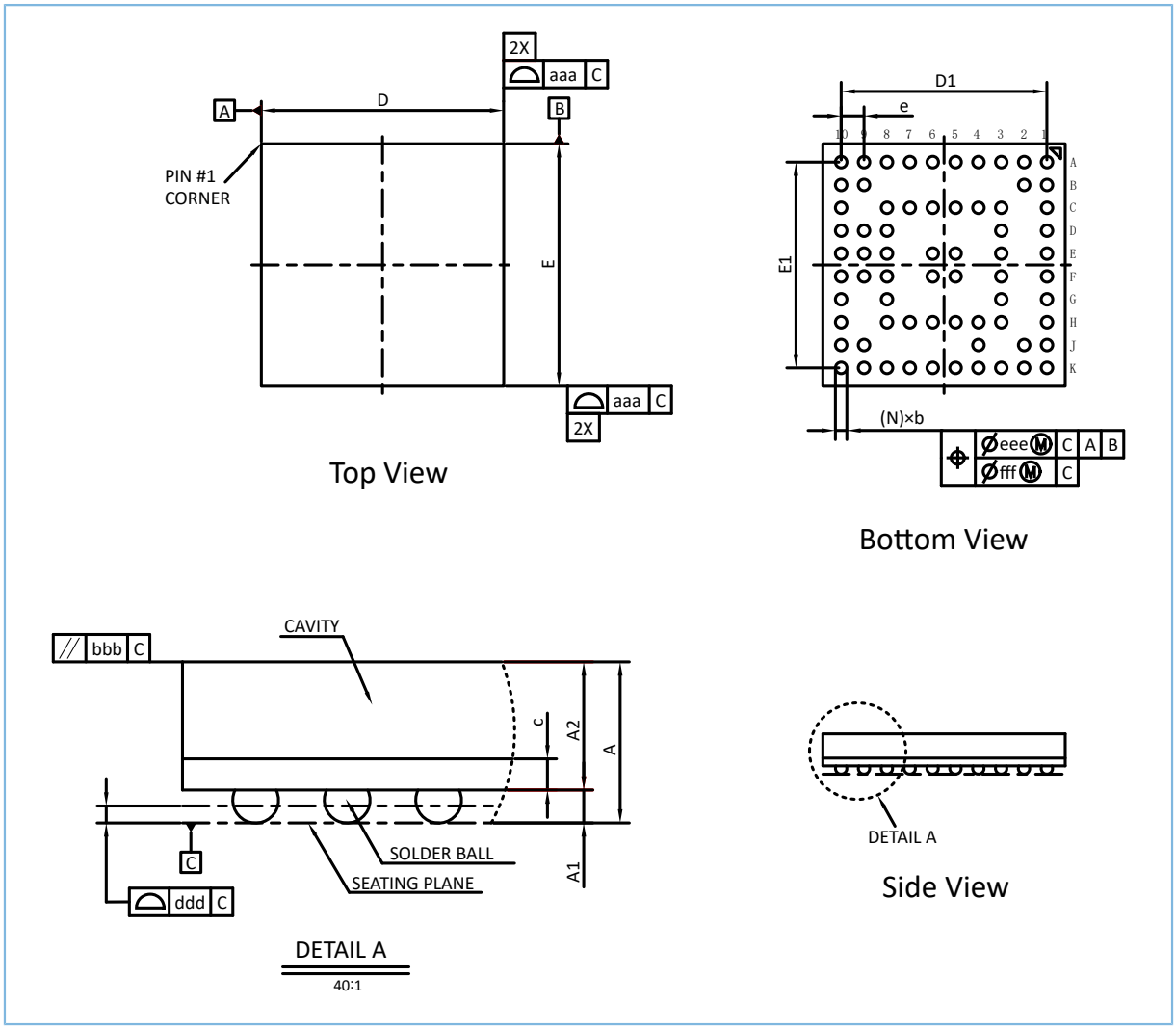


Figure 7-4 BGA68 package outlines

Note:

Drawing is not to scale.

Table 7-4 BGA68 package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.780	0.880	0.980	0.031	0.035	0.039
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.650	0.700	0.750	0.026	0.028	0.030
c	0.140	0.170	0.200	0.006	0.007	0.008
D	5.200	5.300	5.400	0.205	0.209	0.213
E	5.200	5.300	5.400	0.205	0.209	0.213

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Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
D1	--	4.500	--	--	0.177	--
E1	--	4.500	--	--	0.177	--
e	--	0.500	--	--	0.020	--
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		

Note:

Values in inches are converted from values in millimeters and rounded to 3 decimal digits.

7.1.3 BGA55

GR551x BGA55, including GR5515GGBD BGA55, is a 55-pin and 3.5 x 3.5 x 0.60 (mm) BGA package. It is qualified for MSL3.

Table 7-5 BGA55 package information

Parameter	Value	Unit	Tolerance
Package Size	3.5 x 3.5	mm	±0.1 mm
BGA Ball Count	55		
Total Thickness	0.60	mm	±0.05 mm
BGA Ball Pitch	0.40		
Ball Diameter	0.20		
Ball Height	0.12		±0.03 mm

The figure below shows the BGA55 package outlines.

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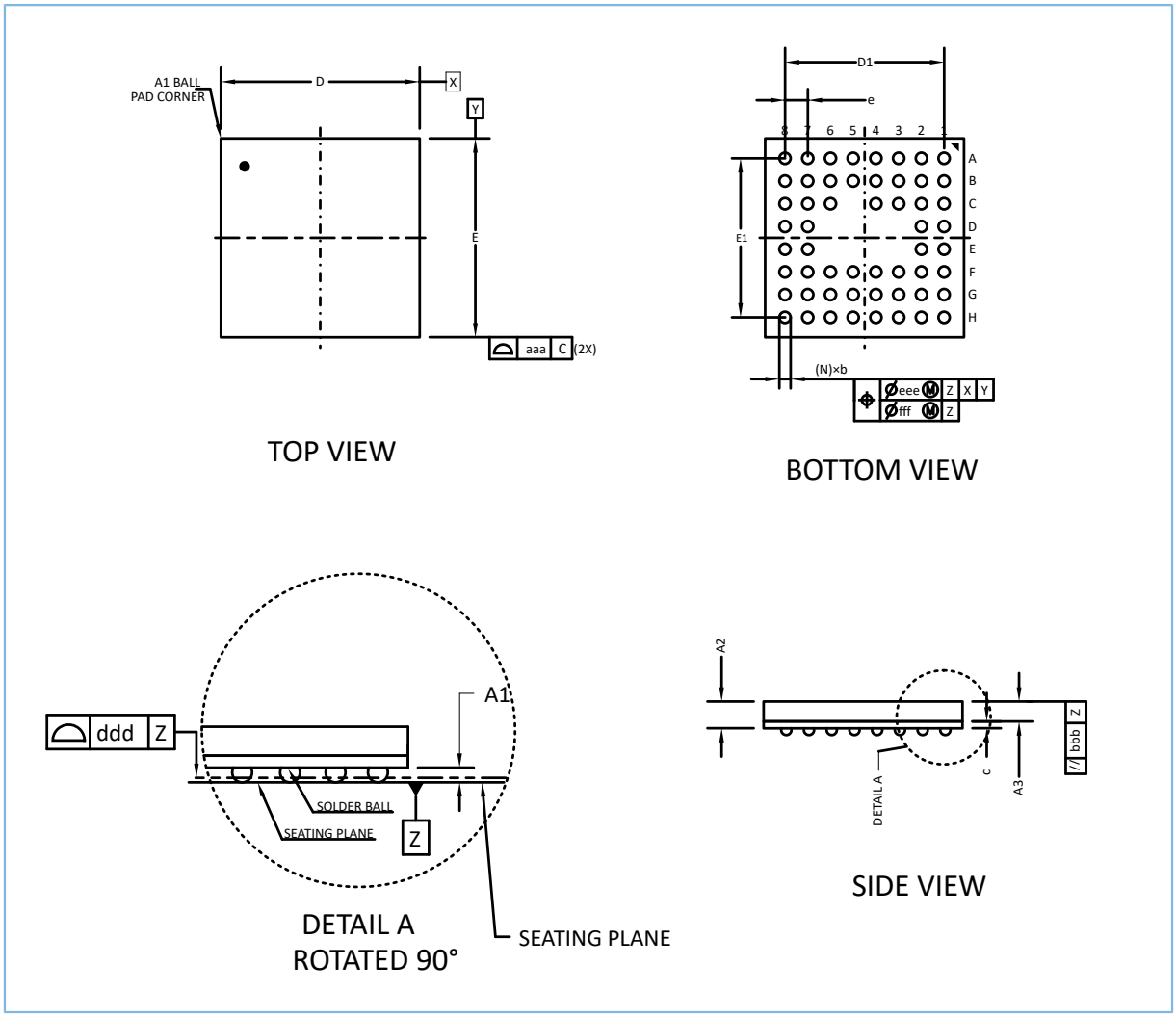


Figure 7-5 BGA55 package outlines

Note:

Drawing is not to scale.

Table 7-6 BGA55 package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.550	0.600	0.650	0.022	0.024	0.026
A1	0.090	0.120	0.150	0.004	0.005	0.006
A2	0.435	0.475	0.505	0.017	0.019	0.020
A3	0.350 REF.			0.014 REF.		
c	0.125 REF.			0.005 REF.		
D	-	3.500	-	-	0.138	-

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Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
E	-	3.500	-		0.138	
D1	-	2.800	-	-	0.110	-
E1	-	2.800	-	-	0.110	-
e	-	0.400	-	-	0.016	-
b	0.150	0.200	0.250	0.006	0.008	0.010
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		

Note:

Values in inches are converted from values in millimeters and rounded to 3 decimal digits.

7.1.4 QFN40

GR551x QFN40, including GR5513BEND QFN40 and GR5513BENDU QFN40, is a 40-pin and 5 x 5 x 0.75 (mm) package. It is qualified for MSL3.

Table 7-7 QFN40 package information

Parameter	Value	Unit	Tolerance
Package Size	5 x 5	mm	±0.1 mm
QFN Pad Count	40		
Total Thickness	0.75	mm	±0.05 mm
QFN Pad Pitch	0.40		
Pad Width	0.20		±0.05 mm
Exposed Pad Size	3.7 x 3.7		±0.1 mm

The figure below shows the QFN40 package outlines.

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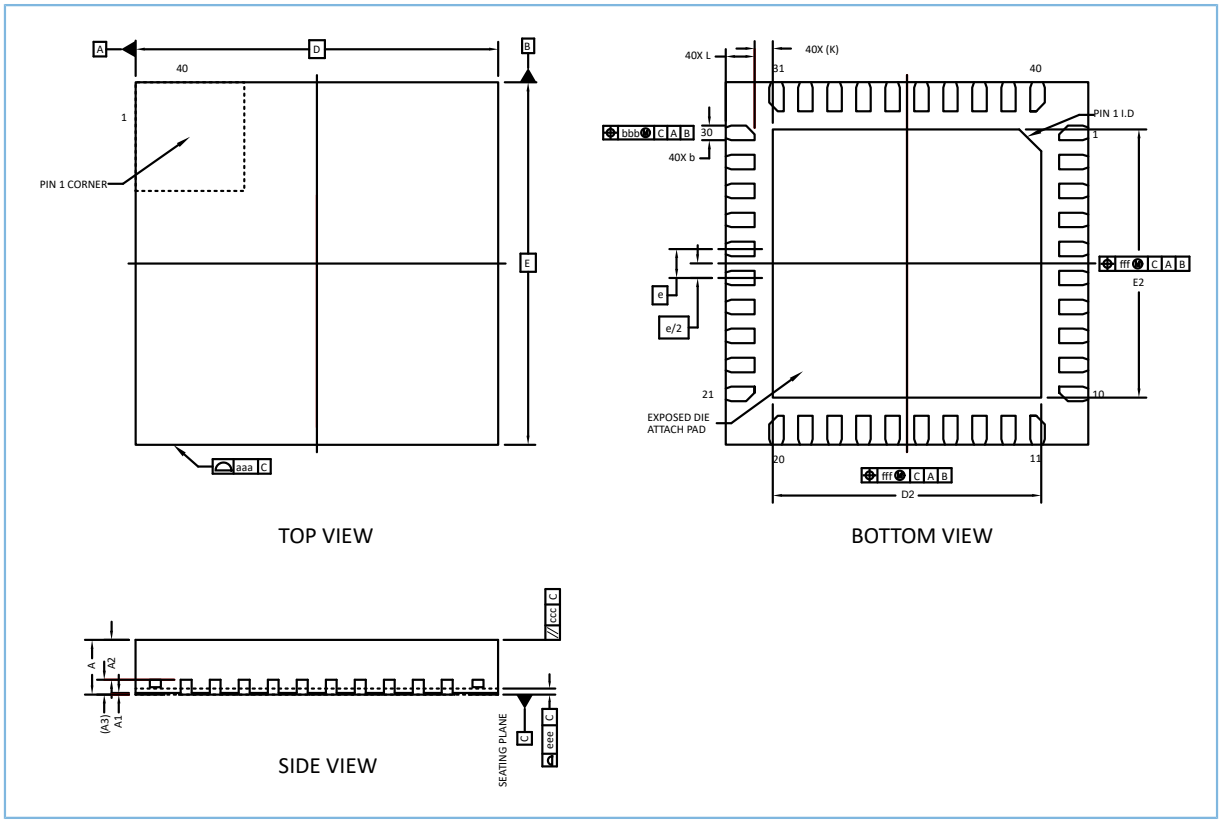


Figure 7-6 QFN40 package outlines

Note:

Drawing is not to scale.

Table 7-8 QFN40 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.550	-	-	0.022	-
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	5.000 BSC.			0.197 BSC.		
E	5.000 BSC.			0.197 BSC.		
e	0.400 BSC.			0.016 BSC.		
D2	3.600	3.700	3.800	0.142	0.146	0.150
E2	3.600	3.700	3.800	0.142	0.146	0.150
L	0.300	0.400	0.500	0.012	0.016	0.020

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Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
K	0.250 REF.			0.010 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.100			0.004		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

7.2 Board Mounting Guideline

Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for QFN and BGA packages. This is further complicated by the large grounding die pad underneath QFN packages and the proximity to the inner edges of the leads.

Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Because surface mount process varies from company to company, careful process development is recommended.

7.2.1 Stencil Design for Perimeter Pads

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 mils to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement.

The first step in achieving reliable solder joints is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

- Area ratio = area of aperture opening/aperture wall area
- Aspect ratio = aperture width/stencil thickness

For rectangular aperture openings, as required for GR551x packages, these ratios are given as:

- Area ratio = LW/2T (L + W)
- Aspect ratio = W/T

L and W are the aperture length and width, and T is stencil thickness. For optimum paste release, the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

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It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release.

It is also recommended that the stencil aperture tolerances should be tightly controlled, as these tolerances can effectively reduce the aperture size. It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the center exposed pad region. See Figure 7-7 for reference solder mask design in the center of the package.

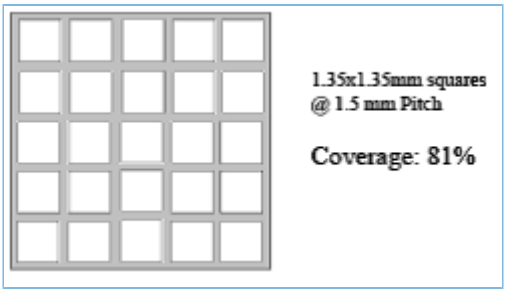


Figure 7-7 Exposed/Ground pad stencil design recommendation for QFN packages

7.2.2 Via Types and Solder Voiding

Voids within solder joints under the exposed grounding pad can have an adverse effect on high-speed and RF applications. Voids within this ground plane can increase the current path of the circuit.

The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any one via would not be rendered ineffectual based on any one void increasing the current path beyond the distance to the next available via.

7.2.2.1 Stencil Thickness and Solder Paste

The stencil thickness of 0.125 mm is recommended for 0.4 mm pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 paste (IPC standard J-STD-005) be used for mounting QFN packages. Nitrogen purge is also recommended during reflow.

The most common surface finishes that are compatible with lead-free surface mount technology (SMT) process are:

- Organic solderability preservatives (OSP)
- Electroless nickel/Immersion gold (ENIG)
- Immersion silver
- Immersion gold

Selection of a suitable finish will depend on end users’ requirements for board design, assembly process, handling/ storage, and cost.

7.2.2.2 PCB Materials

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Due to the higher reflow temperature requirement of the lead-free material set, the board material with higher glass transition temperature Tg (> 170°C) is recommended.

7.2.3 SMT Printing Process

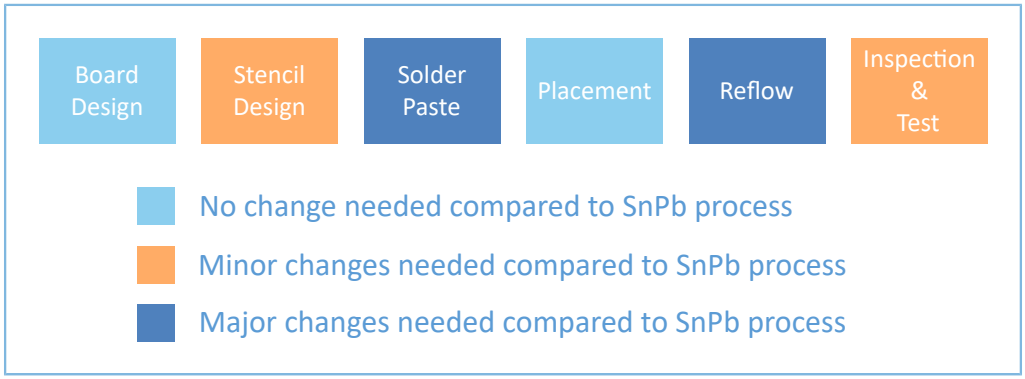


Figure 7-8 SMT printing process

- Solder Paste

  Sn-Ag-Cu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance.

- Stencil Design

  The recommended stencil is laser-cut, stainless-steel type with thickness of 5 to 7 mils and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 1 mil larger than the top can be utilized. Sn-Ag-Cu solder does not wet as well as Sn-Pb solder.

- Printing Process

  The printing process requires no significant changes, comparing with that applies Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste deposition.

- Placement

  With the self-aligning characteristic of the QFN packages during reflow, the placement accuracy is < 30% of the pad width or as long as the solder pads can touch solder paste.

7.3 SMT Reflow Process

The optimization of the reflow process is the most critical factor to be considered for the lead-free soldering. The development of an optimal profile should take into account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensure successful lead-free assembly, high yield and long-term solder joint reliability.

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1. Temperature Profiling

   Temperature profiling should be performed for all new board designs by attaching thermocouples at the solder joints of QFN and BGA packages, on the top surface of the larger components as well as at multiple locations of the boards. This is to ensure that all components are heated to temperature above the minimum reflow temperatures and the smaller components do not exceed maximum temperature limit.

   For larger or sophisticated boards with a large number of components, it is also important to minimize the temperature difference across the board to be less than 10 degree to minimize board warp. Maximum temperature at component body should not exceed the MSL3 qualification specification.

2. Reflow Profile Guideline

   The solder reflow profile should follow the recommendation from paste manufacturers and general standards such as JEDEC/IPC J-STD-20. Figure 7-9 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 7-9.

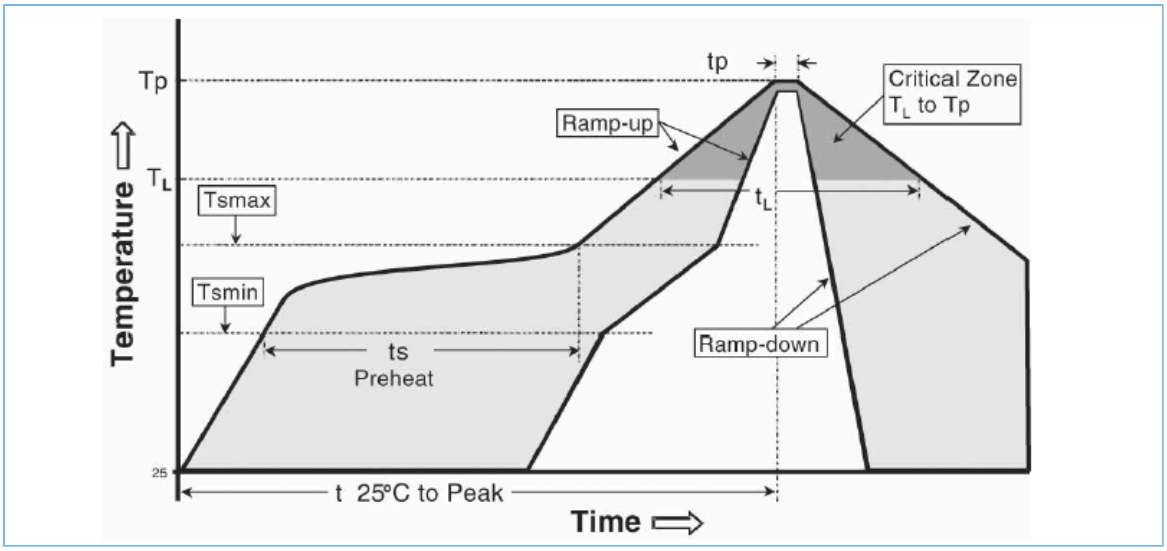


Figure 7-9 JEDEC recommended lead-free reflow profile

The GR551x fulfills the lead-free soldering requirements from IPC/JEDEC, i.e. reflow soldering with a peak temperature up to 260°C.

The QFN40 lead frame is made of CμAg and has Matte Sn plating. This is 100% Sn and thus Pb-free. Plating thickness is 300 – 600 μin. The Matte Sn CμAg LF can withstand 3x reflow at 260°C.

Table 7-9 Reflow Profile Parameters

Profile Parameters	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate (Tsmax to Tp)	3°C/second (max)
Preheat temperature (Tsmin to Tsmax)	150°C – 200°C
Preheat time (ts)	60 seconds – 180 seconds
Time above TBL, 217°C (TL)	60 seconds – 150 seconds
Time within 5°C of peak temperature (tp)	20 seconds – 40 seconds

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Profile Parameters	Lead-Free Assembly, Convection, IR/Convection
Ramp-down rate	6°C/second (max)
Time 25°C to peak temperature	8 minutes (max)

Note:

All specified temperatures in Table 7-9 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 7-9 to prevent thermal damage to the package. An example of reflow profile is shown in Figure 7-10.

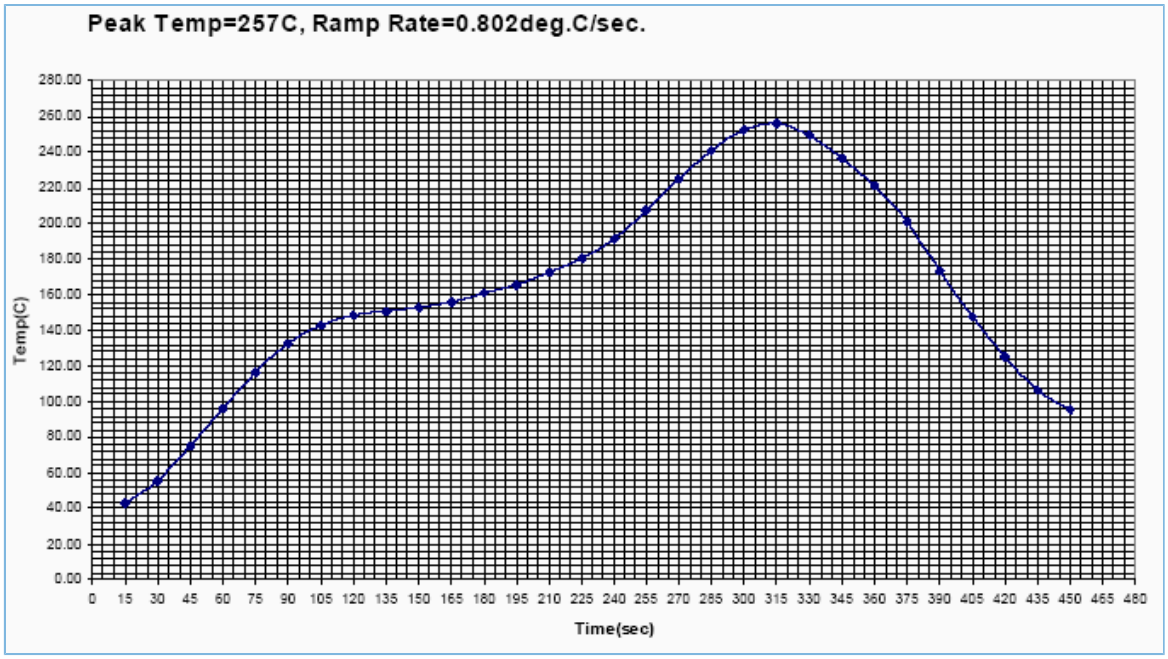


Figure 7-10 Reflow profile example with 257°C peak temperature

3. Reflow Oven

   It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. An oven with more heating zones offers higher flexibility to optimize the reflow profile for complex and/or larger boards. Nitrogen atmosphere can improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

7.4 Rework Guideline

Because solder joints are not fully exposed for QFN and BGA packages, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of QFN and BGA packages can be a challenge due to their small size.

In most applications, QFN and BGA packages will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Because reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent

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complexities, the following only provides a guideline and a starting point for the development of a successful rework process for QFN packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste printing
4. Component placement
5. Component attachment

Note:

Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

7.4.1 Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally, the reflow profile for part removal should be the same as the one used for part attachment. However, the time above the liquidus state can be reduced as long as the reflow is complete.

Note:

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and heated on the top side using hot gas or air.

Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided because this may cause chip scale package (CSP) to skew. Air velocity of 15 – 20 liters per minute is a good starting point. Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cool down.

Because of the small size of GR551x SoCs, the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad lift-off.

7.4.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and de-soldering braid. The width of the blade should match to the maximum width of the footprint and the blade temperature should be low enough to prevent any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer’s recommendations should be followed.

7.4.3 Solder Paste Printing

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Because of their small size and finer pitches, solder paste deposition for QFN packages requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100x magnification.

The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side. A 125 microns thick stencil with aperture size and shape same as the package land should be used.

In addition, no-clean flux should be used, because small standoff of QFN packages does not leave much room for cleaning.

7.4.4 Component Placement

QFN packages are expected to have superior self-centering ability due to their small mass. The placement of QFN packages should be similar to that of BGAs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The alignment should also be done at 50 to 100x magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

7.4.5 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Because all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

7.5 RoHS Compliant

GR551x is RoHS compliant, as per directive 2002/95/EC and its subsequent amendments.

7.6 SVHC Materials (REACH)

GR551x is compliant with Substance of Very High Concern (SVHC) list based on the publication by European Chemicals Agency (ECHA) on October 28, 2008 Regulation (EC) No 1907/2006 concerning *Registration, Evaluation, Authorisation and Restriction of Chemicals (REACH)*.

7.7 Halogen Free

GR551x is compliant with BS EN 14582: 2007 in regards to halogens: fluorine, chlorine, bromine, and iodine content.

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