# GR5525 Hardware Design Guidelines

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# Preface

## Purpose

This document is to present the necessary circuit required for proper operation of GR5525 Bluetooth System-on-Chips (SoCs). Recommended chip interfaces, peripherals, schematic diagram, and PCB layout guidelines of the GR5525 SoC family are provided.

This *Hardware Design Guidelines* intends to help system designers build minimal Bluetooth Low Energy (Bluetooth LE) hardware circuits and develop products.

## Audience

This document is intended for:

- Device user
- Bluetooth product engineer
- Bluetooth LE system designer
- Hardware engineer

## Release Notes

This document is the fourth release of *GR5525 Hardware Design Guidelines*, corresponding to GR5525 SoC series.

## Revision History

| Version | Date | Description |
|---|---|---|
| 1.0 | 2023-09-20 | Initial release |
| 1.1 | 2024-03-29 | Optimized some descriptions. |
| 1.2 | 2024-07-17 | Updated "Power-on Sequence" and "Reference Schematic Diagram". |
| 1.3 | 2024-09-12 | Deleted the GR5525IGNI SoC and updated "Reference Schematic Diagram". |

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# 1 Product Overview

The Goodix GR5525 series is a single-mode, low-power Bluetooth 5.3 System-on-Chip (SoC). It can be configured as a Broadcaster, an Observer, a Central, and a Peripheral and supports the combination of all the above roles, making it an ideal choice for Internet of Things (IoT) and smart wearable devices.

Based on Arm® Cortex®-M4F CPU core running at 96 MHz, the GR5525 integrates a 2.4 GHz RF transceiver, Bluetooth LE 5.3 protocol stack, on-chip programmable Flash memory, 256 KB system SRAM, and a rich set of peripherals, enhanced I2C/UART port number for sensor applications, as well as expanded I/O functionality. The GR5525 MCU enhances QSPI interface to support external RAM (PSRAM) to accommodate display while still leaving plenty of space for wearable schemes.

GR5525 series are offered in both QFN68 and QFN56 packages. The table below lists the detailed package configurations.

Table 1-1 GR5525 series

| Part Number | GR5525RGNI | GR5525IENI | GR5525I0NI |
|---|---|---|---|
| CPU | Cortex®-M4F | Cortex®-M4F | Cortex®-M4F |
| RAM | 256 KB | 256 KB | 256 KB |
| SiP Flash | 1 MB | 512 KB | N/A |
| I/O number | 50 | 39 | 39 |
| I/O voltage | 1.8 V–3.6 V | 1.8 V–3.6 V | In line with Flash voltage |
| Package (mm) | QFN68 (7.0 x 7.0 x 0.85) | QFN56 (7.0 x 7.0 x 0.75) | QFN56 (7.0 x 7.0 x 0.75) |

## 1.1 Features

- Bluetooth LE 5.3 transceiver
  - Supported data rates: 1 Mbps, 2 Mbps, and Long Range (500 kbps, 125 kbps)
  - TX power: –20 dBm to +7 dBm
  - RX sensitivity
    - –97 dBm sensitivity @ 1 Mbps mode
    - –93 dBm sensitivity @ 2 Mbps mode
    - –101 dBm sensitivity @ Long Range 500 kbps mode
    - –103 dBm sensitivity @ Long Range 125 kbps mode
  - Power consumption at 3.3 V VBAT input:
    - 6.3 mA TX current @ 0 dBm output power (64 MHz system clock)
    - 5.3 mA RX current @ 1 Mbps (64 MHz system clock)
- Arm® Cortex®-M4F 32-bit micro-processor with floating point support

  - Up to 96 MHz clock frequency
  - Built-in Memory Protection Unit (MPU) supporting eight programmable regions
  - Hardware Floating Point Unit (FPU)
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Non-maskable Interrupt (NMI) input
  - Serial Wire Debug (SWD) with 16 breakpoints, two watchpoints, and a debug timestamp counter
  - 56 µA/MHz CoreMark running from Flash @ 3.3 V, 64 MHz from HFXO
- On-chip memory
  - 256 KB RAM data memory with retention capabilities
  - 8 KB cache RAM instruction memory with retention capabilities
  - Stack ROM (including boot ROM and Bluetooth LE Stack)
  - 1 MB internal QSPI Flash (512 KB for GR5525IENI, and external Flash for GR5525I0NI)
- Digital peripherals
  - 2 x general-purpose DMA engines with six channels and up to 16 programmable request/trigger sources
- Analog peripherals
  - 1 x 13-bit Sense ADC with sampling rate of 1 Msps, supporting up to eight external I/O channels and three internal signal channels
  - Built-in die temperature and voltage sensors
  - Low-power comparator, supporting wakeup from sleep mode
- Flexible serial peripherals
  - 4 x UART modules up to 2 Mbps with flow control and IrDA features
  - 4 x I2C modules for peripheral communication, up to 3.4 MHz, operating as either Master or Slave
  - 2 x I2S interfaces (1 x I2S master interface and 1 x I2S slave interface)
  - PDM interface with hardware sampling rate converter
  - 1 x 8-bit/16-bit/32-bit SPI master interface and 1 x SPI slave interface for host communication
  - 1 x Dual-lane SPI (DSPI) interface for display, with MIPI DBI Type-C support
  - 3 x Quad SPI (QSPI) interfaces, up to 48 MHz; supporting direct access via memory mapping when connecting with external NOR Flash
- Security
  - Complete secure computing engine:
    - AES 128-bit/192-bit/256-bit symmetric encryption (ECB, CBC)

        - Hash-based Message Authentication Code (HMAC-SHA256)
        - Public key cryptography (PKC)
        - True random number generator (TRNG)
    - Comprehensive security operation mechanism:
        - Secure boot
        - Encrypted firmware running directly from Flash
        - eFuse for encrypted key storage
        - Differentiate application data key and firmware key, supporting one data key per device/product
- I/O peripherals
    - Up to 50 multiplexed I/O pins in total
        - Up to 34 general-purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors
        - Up to eight always-on I/O (AON I/O) pins, supporting wakeup from sleep mode
        - Up to eight mixed signal I/O (MSIO) pins, configurable to be digital/analog signal interfaces
- Timers
    - 2 x 32-bit general-purpose timers
    - 1 x dual timer with two programmable 32-bit or 16-bit down counters
    - 1 x sleep timer for waking the device up from sleep mode
    - 2 x 3-channel PWMs with edge-aligned and center-aligned modes
    - 2 x real-time counters (1 x Calendar, 1 x real-time counter)
- Power management
    - On-chip DC-DC to provide RF analog voltage and supply core LDO
    - On-chip I/O LDO to provide I/O voltage and supply external components
    - Programmable thresholds for brownout detector (BOD)
    - Supply voltage: 2.4 V–3.8 V
    - I/O voltage: 1.8 V–3.6 V
- Low-power consumption
    - Sleep mode: 7.3 µA (Typical) at 3.3 V VBAT input, wakeup sources from always-on domain, and LFXO_32K running
    - Ultra deep sleep mode: 5.0 µA (Typical), with no memory data in retention and wakeup sources from SLP Timer or AON I/Os

- OFF mode: 200 nA (Typical), with system in reset mode

- Operating temperature range: –40°C to +85°C
- Packages
  - QFN68: 7.0 x 7.0 x 0.85 mm, 0.35 mm pitch
  - QFN56: 7.0 x 7.0 x 0.75 mm, 0.4 mm pitch

## 1.2 Block Diagram

The block diagram of GR5525 is shown in the figure below.

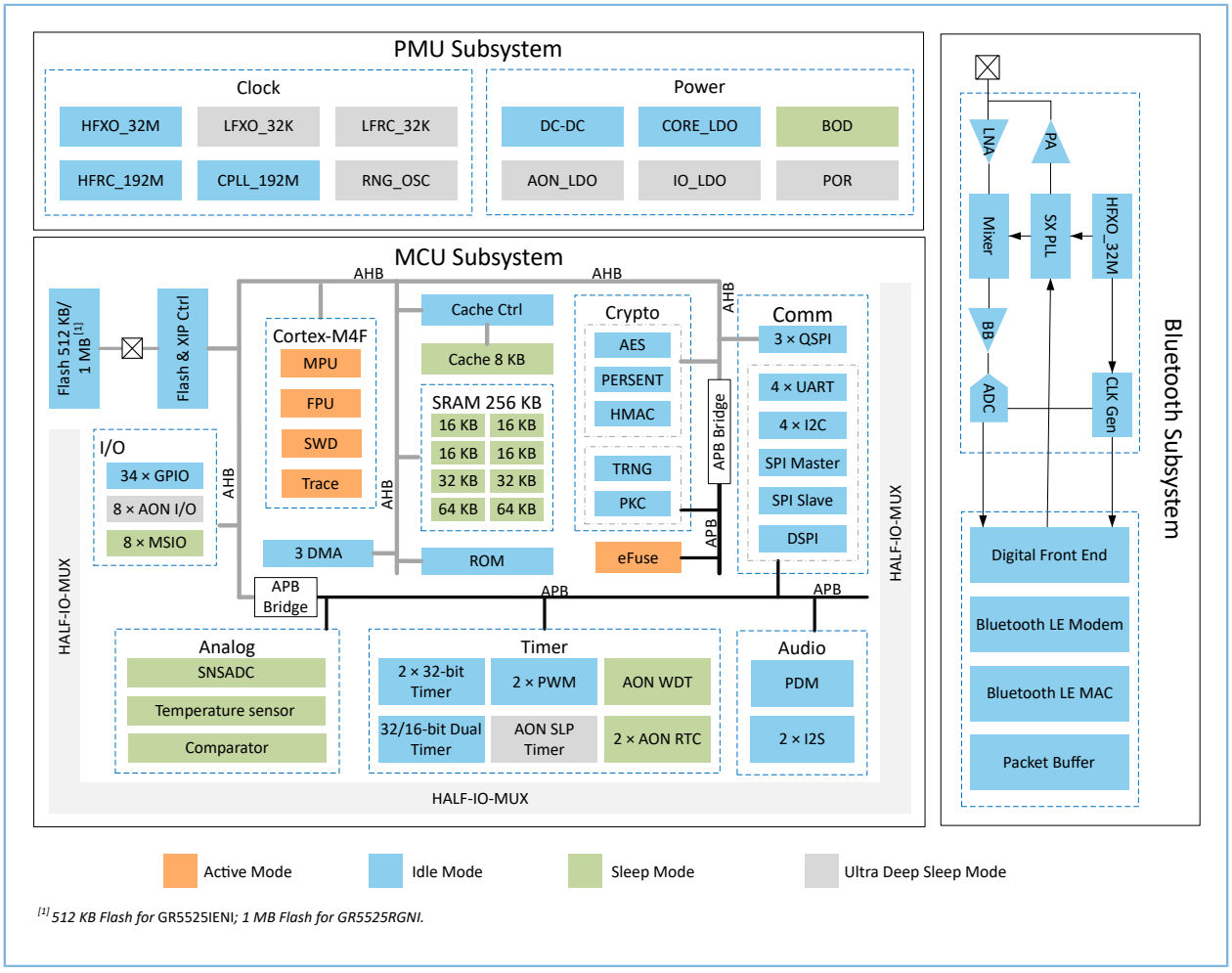


Figure 1-1 GR5525 block diagram

**Note**:

For more details of each module in this block diagram, see *GR5525 Datasheet*.

# 2 Pinout

This chapter describes the pin assignment of the device and provides detailed information for each individual pin.

## 2.1 QFN68

The figure below shows the pin assignment for devices in QFN68 package.

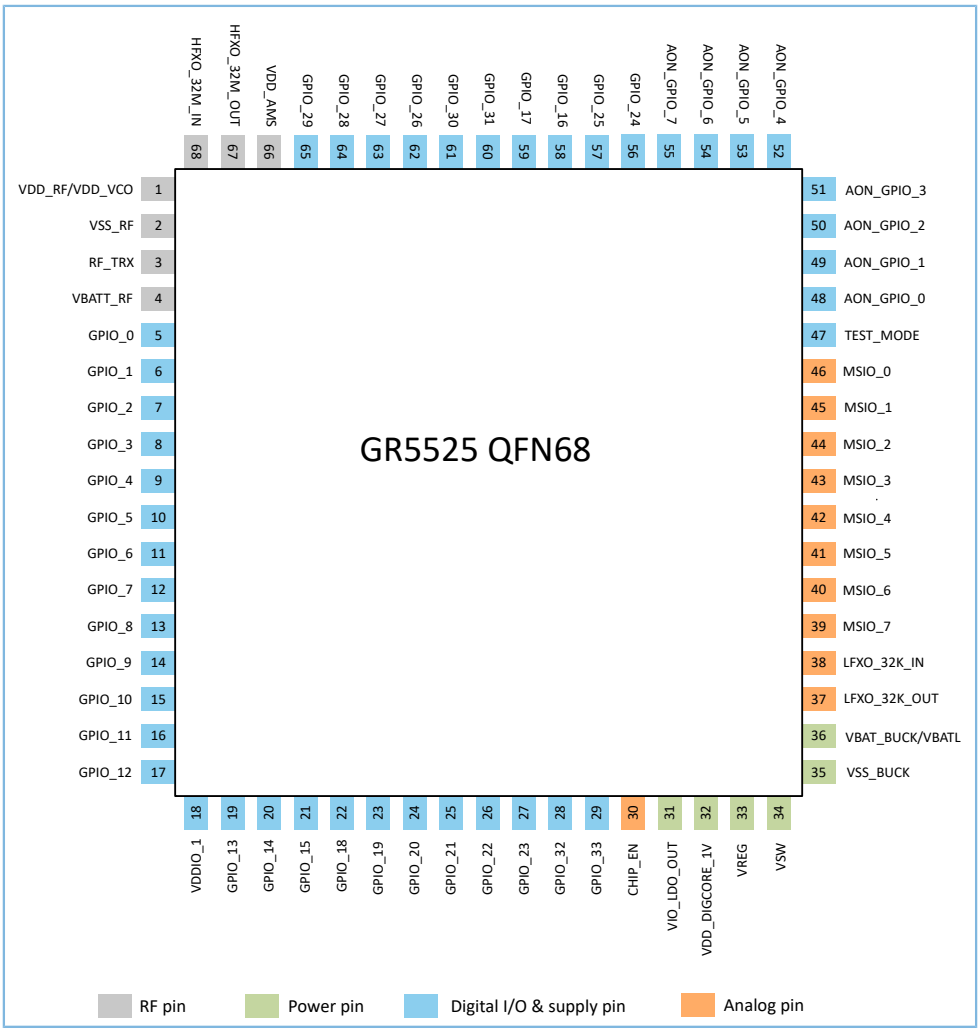


Figure 2-1 QFN68 pinout from top view

The following table provides the descriptions of pin functionality.

Table 2-1 Pin description

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 1 | VDD_RF/VDD_VCO | Analog/RF supply | Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG | |
| 2 | VSS_RF | Analog/RF | RF GND; connect to GND | |
| 3 | RF_TRX | Analog/RF | RF transceiver RX input and TX output | |
| 4 | VBATT_RF | Analog/RF Supply | RF SPA and Bandgap supply; connect to VBATL | |

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 5 | GPIO_0 | Digital I/O | General purpose I/O; default: SWD_CLK | VDDIO1 |
| 6 | GPIO_1 | Digital I/O | General purpose I/O; default: SWD_IO | |
| 7 | GPIO_2 | Digital I/O | General purpose I/O, configurable to be an SWO interface | |
| 8 | GPIO_3 | Digital I/O | General purpose I/O | |
| 9 | GPIO_4 | Digital I/O | | |
| 10 | GPIO_5 | Digital I/O | | |
| 11 | GPIO_6 | Digital I/O | | |
| 12 | GPIO_7 | Digital I/O | | |
| 13 | GPIO_8 | Digital I/O | | |
| 14 | GPIO_9 | Digital I/O | | |
| 15 | GPIO_10 | Digital I/O | | |
| 16 | GPIO_11 | Digital I/O | | |
| 17 | GPIO_12 | Digital I/O | | |
| 18 | VDDIO_1 | Digital I/O supply | Digital I/O supply input. Support external 1.8 V–3.3 V input voltage. | |
| 19 | GPIO_13 | Digital I/O | General purpose I/O | |
| 20 | GPIO_14 | Digital I/O | | |
| 21 | GPIO_15 | Digital I/O | | |
| 22 | GPIO_18 | Digital I/O | | |
| 23 | GPIO_19 | Digital I/O | | |
| 24 | GPIO_20 | Digital I/O | | |
| 25 | GPIO_21 | Digital I/O | | |
| 26 | GPIO_22 | Digital I/O | | |
| 27 | GPIO_23 | Digital I/O | | |
| 28 | GPIO_32 | Digital I/O | | |
| 29 | GPIO_33 | Digital I/O | | |
| 30 | CHIP_EN | Analog/PMU | Master Enable for chip reset pin.<br>The high level of CHIP_EN equals VBATL.<br>Minimum value of high level for CHIP_EN: 1 V | |
| 31 | VIO_LDO_OUT | PMU | Output of on-chip I/O supply regulator, connect internally to VDDIO0.<br>Typical output: 1.8 V | VDDIO0 |
| 32 | VDD_DIGCORE_1V | Analog/PMU | On-chip LDO output for digital core | |
| 33 | VREG | Analog/PMU | DC-DC feedback pin of switch regulator | |

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 34 | VSW | Analog/PMU | DC-DC converter switching node | |
| 35 | VSS_BUCK | Analog/PMU | DC-DC converter power GND | |
| 36 | VBAT_BUCK/VBATL | Analog/PMU | Power supply: 2.4 V to 3.8 V | |
| 37 | LFXO_32K_OUT | PMU | Output of inverting amplifier connected to 32.768 kHz crystal | |
| 38 | LFXO_32K_IN | PMU | Input of inverting amplifier connected to 32.768 kHz crystal | |
| 39 | MSIO_7 | Mixed Signal I/O | Configurable mixed-signal I/O with digital I/O and analog I/O | VBATL |
| 40 | MSIO_6 | Mixed Signal I/O | | |
| 41 | MSIO_5 | Mixed Signal I/O | | |
| 42 | MSIO_4 | Mixed Signal I/O | | |
| 43 | MSIO_3 | Mixed Signal I/O | | |
| 44 | MSIO_2 | Mixed Signal I/O | | |
| 45 | MSIO_1 | Mixed Signal I/O | | |
| 46 | MSIO0 | Mixed Signal I/O | | |
| 47 | TEST_MODE | Analog/RF | Input pin, used for factory test mode selection<br>• 1: factory test mode<br>• 0: normal operation mode<br>**Note:**<br>In practice, the value is set to 0 and the pin is connected to GND by default. | |
| 48 | AON_GPIO_0 | Digital I/O | Always-on GPIO; can wake up chip from sleep modes | VDDIO0 |
| 49 | AON_GPIO_1 | Digital I/O | | |
| 50 | AON_GPIO_2 | Digital I/O | | |
| 51 | AON_GPIO_3 | Digital I/O | | |
| 52 | AON_GPIO_4 | Digital I/O | | |
| 53 | AON_GPIO_5 | Digital I/O | | |
| 54 | AON_GPIO_6 | Digital I/O | | |
| 55 | AON_GPIO_7 | Digital I/O | | |
| 56 | GPIO_24 | Digital I/O | General purpose I/O | |
| 57 | GPIO_25 | Digital I/O | | |
| 58 | GPIO_16 | Digital I/O | | |
| 59 | GPIO_17 | Digital I/O | | |
| 60 | GPIO_31 | Digital I/O | | |
| 61 | GPIO_30 | Digital I/O | | |
| 62 | GPIO_26 | Digital I/O | | |

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 63 | GPIO_27 | Digital I/O | | |
| 64 | GPIO_28 | Digital I/O | | |
| 65 | GPIO_29 | Digital I/O | | |
| 66 | VDD_AMS | Analog/RF | AMS supply: 1.1 V. Connect to VREG. | |
| 67 | HFXO_32M_OUT | Analog/RF | Output of inverting amplifier connected to 32 MHz crystal | |
| 68 | HFXO_32M_IN | Analog/RF | Input of inverting amplifier connected to 32 MHz crystal | |

**Note**:

- The pad drive strength for GPIO and AON_GPIO pins can be configured to 4 mA under 3.3 V voltage.
- The pad drive strength for MSIO pins can be configured to 2 mA under 3.3 V voltage.

## 2.2 QFN56 (With Flash)

The figure below shows the pin assignment for devices in QFN56 package (with Flash).

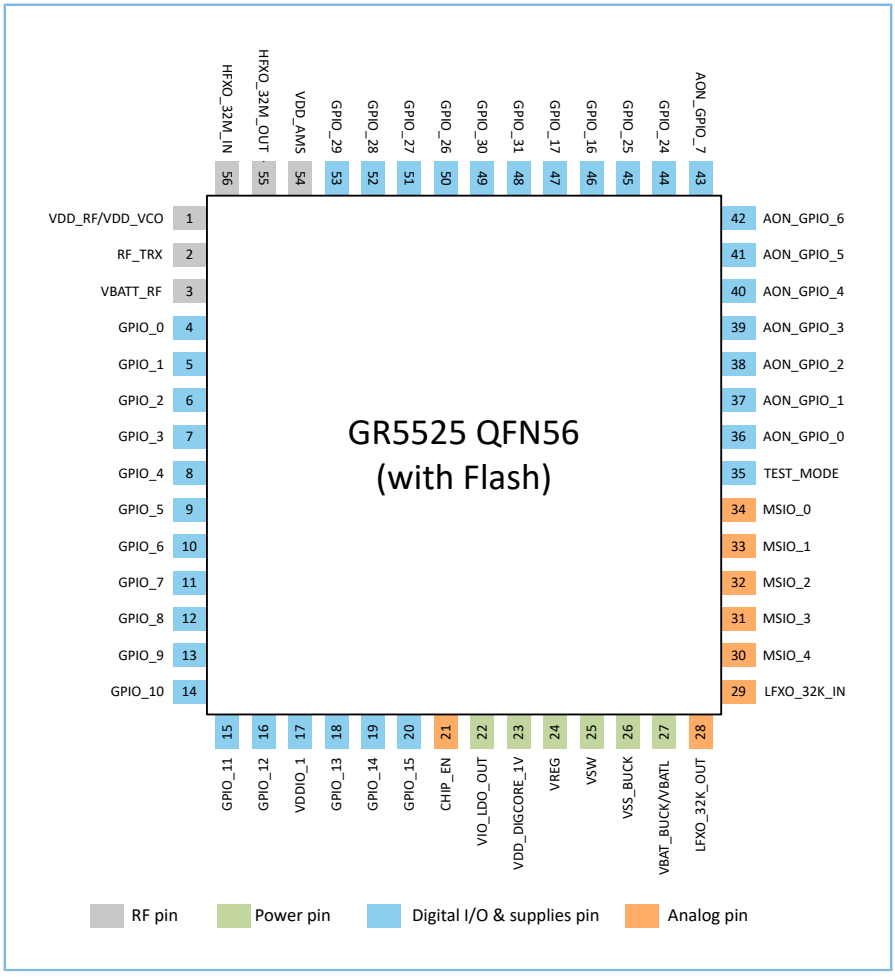


Figure 2-2 QFN56 (with Flash) pinout from top view

The following table provides the descriptions of pin functionality.

Table 2-2 Pin description

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 1 | VDD_RF/VDD_VCO | Analog/RF supply | Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG | |
| 2 | RF_TRX | Analog/RF | RF transceiver RX input and TX output | |
| 3 | VBATT_RF | Analog/RF Supply | RF SPA and Bandgap supply; connect to VBATL | |
| 4 | GPIO_0 | Digital I/O | General purpose I/O; default: SWD_CLK | VDDIO1 |
| 5 | GPIO_1 | Digital I/O | General purpose I/O; default: SWD_IO | |
| 6 | GPIO_2 | Digital I/O | General purpose I/O | |
| 7 | GPIO_3 | Digital I/O | | |
| 8 | GPIO_4 | Digital I/O | | |
| 9 | GPIO_5 | Digital I/O | | |
| 10 | GPIO_6 | Digital I/O | | |
| 11 | GPIO_7 | Digital I/O | | |
| 12 | GPIO_8 | Digital I/O | | |
| 13 | GPIO_9 | Digital I/O | | |
| 14 | GPIO_10 | Digital I/O | | |
| 15 | GPIO_11 | Digital I/O | | |
| 16 | GPIO_12 | Digital I/O | | |
| 17 | VDDIO_1 | Digital I/O supply | Digital I/O supply input. Support external 1.8 V–3.3 V input voltage. | |
| 18 | GPIO_13 | Digital I/O | General purpose I/O | |
| 19 | GPIO_14 | Digital I/O | | |
| 20 | GPIO_15 | Digital I/O | | |
| 21 | CHIP_EN | Analog/PMU | Master Enable for chip reset pin.<br>The high level of CHIP_EN equals VBATL.<br>Minimum value of high level for CHIP_EN: 1 V | |
| 22 | VIO_LDO_OUT | PMU | Output of on-chip I/O supply regulator, connect internally to VDDIO0.<br>Typical output: 1.8 V | VDDIO0 |
| 23 | VDD_DIGCORE_1V | Analog/PMU | On-chip LDO output for digital core | |
| 24 | VREG | Analog/PMU | DC-DC feedback pin of switch regulator | |
| 25 | VSW | Analog/PMU | DC/DC converter switching node | |
| 26 | VSS_BUCK | Analog/PMU | DC/DC converter supply and general battery GND | |
| 27 | VBAT_BUCK/VBATL | Analog/PMU | Power supply: 2.4 V to 3.8 V | |

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 28 | LFXO_32K_OUT | PMU | Output of inverting amplifier connected to 32.768 kHz crystal | |
| 29 | LFXO_32K_IN | PMU | Input of inverting amplifier connected to 32.768 kHz crystal | |
| 30 | MSIO_4 | Mixed Signal I/O | Configurable mixed-signal I/O with digital I/O and analog I/O | VBATL |
| 31 | MSIO_3 | Mixed Signal I/O | | |
| 32 | MSIO_2 | Mixed Signal I/O | | |
| 33 | MSIO_1 | Mixed Signal I/O | | |
| 34 | MSIO_0 | Mixed Signal I/O | | |
| 35 | TEST_MODE | Analog/RF | Input pin, used for factory test mode selection<br>• 1: factory test mode<br>• 0: normal operation mode<br>**Note:**<br>In practice, the value is set to 0 and the pin is connected to GND by default. | |
| 36 | AON_GPIO_0 | Digital I/O | Always-on GPIO; can wake up chip from sleep modes | VDDIO0 |
| 37 | AON_GPIO_1 | Digital I/O | | |
| 38 | AON_GPIO_2 | Digital I/O | | |
| 39 | AON_GPIO_3 | Digital I/O | | |
| 40 | AON_GPIO_4 | Digital I/O | | |
| 41 | AON_GPIO_5 | Digital I/O | | |
| 42 | AON_GPIO_6 | Digital I/O | | |
| 43 | AON_GPIO_7 | Digital I/O | | |
| 44 | GPIO_24 | Digital I/O | General purpose I/O | |
| 45 | GPIO_25 | Digital I/O | | |
| 46 | GPIO_16 | Digital I/O | | |
| 47 | GPIO_17 | Digital I/O | | |
| 48 | GPIO_31 | Digital I/O | | |
| 49 | GPIO_30 | Digital I/O | | |
| 50 | GPIO_26 | Digital I/O | | |
| 51 | GPIO_27 | Digital I/O | | |
| 52 | GPIO_28 | Digital I/O | | |
| 53 | GPIO_29 | Digital I/O | | |
| 54 | VDD_AMS | Analog/RF | AMS supply: 1.1 V. Connect to VREG. | |
| 55 | HFXO_32M_OUT | Analog/RF | Output of inverting amplifier connected to 32 MHz crystal | |

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 56 | HFXO_32M_IN | Analog/RF | Input of inverting amplifier connected to 32 MHz crystal | |

**Note**:

- The pad drive strength for GPIO and AON_GPIO pins can be configured to 4 mA under 3.3 V voltage.
- The pad drive strength for MSIO pins can be configured to 2 mA under 3.3 V voltage.

## 2.3 QFN56 (Without Flash)

The figure below shows the pin assignment for devices in QFN56 package (without Flash).

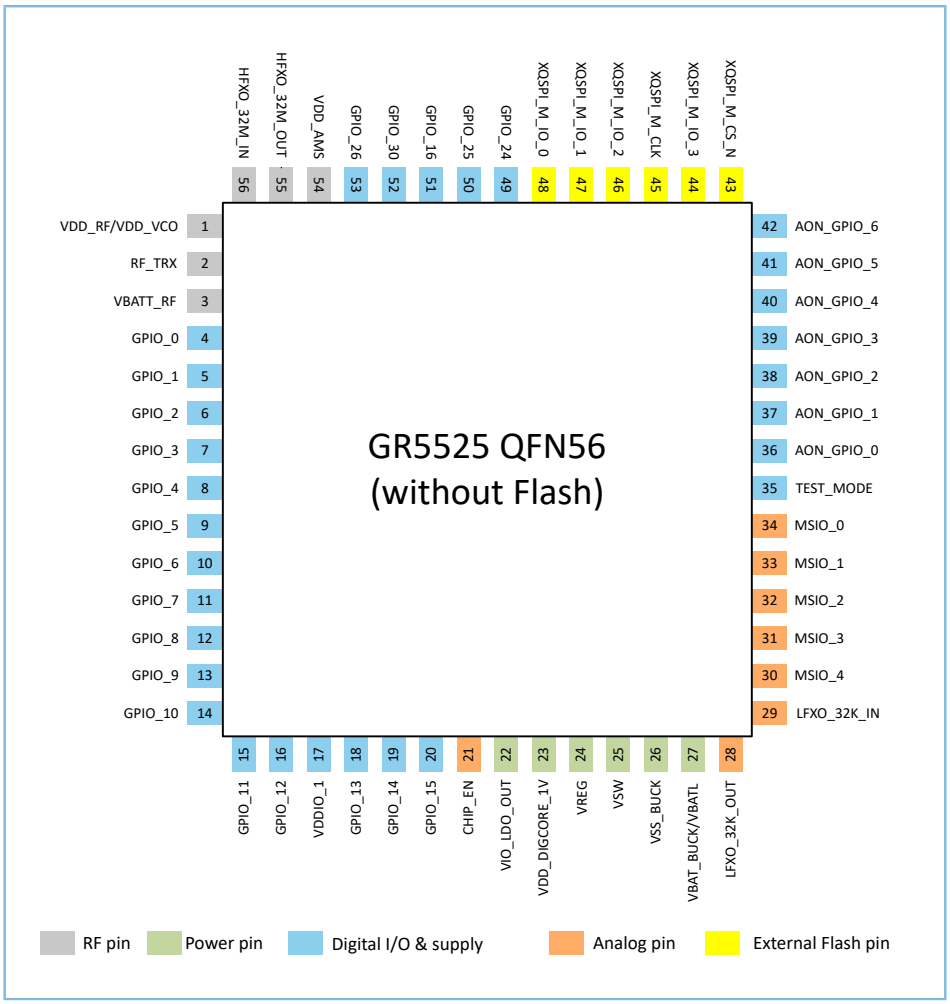


Figure 2-3 QFN56 (without Flash) pinout from top view

The following table provides the descriptions of pin functionality.

Table 2-3 Pin description

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 1 | VDD_RF/VDD_VCO | Analog/RF supply | Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG | |
| 2 | RF_TRX | Analog/RF | RF transceiver RX input and TX output | |
| 3 | VBATT_RF | Analog/RF Supply | RF SPA and bandgap supply; connect to VBATL | |
| 4 | GPIO_0 | Digital I/O | General purpose I/O; default: SWD_CLK | VDDIO1 |
| 5 | GPIO_1 | Digital I/O | General purpose I/O; default: SWD_IO | |
| 6 | GPIO_2 | Digital I/O | General purpose I/O | |
| 7 | GPIO_3 | Digital I/O | | |
| 8 | GPIO_4 | Digital I/O | | |
| 9 | GPIO_5 | Digital I/O | | |
| 10 | GPIO_6 | Digital I/O | | |
| 11 | GPIO_7 | Digital I/O | | |
| 12 | GPIO_8 | Digital I/O | | |
| 13 | GPIO_9 | Digital I/O | | |
| 14 | GPIO_10 | Digital I/O | | |
| 15 | GPIO_11 | Digital I/O | | |
| 16 | GPIO_12 | Digital I/O | | |
| 17 | VDDIO_1 | Digital I/O supply | Digital I/O supply input. Support external 1.8 V–3.3 V input voltage. | |
| 18 | GPIO_13 | Digital I/O | General purpose I/O | |
| 19 | GPIO_14 | Digital I/O | | |
| 20 | GPIO_15 | Digital I/O | | |
| 21 | CHIP_EN | Analog/PMU | Master Enable for chip reset pin.<br>The high level of CHIP_EN equals VBATL.<br>Minimum value of high level for CHIP_EN: 1 V | |
| 22 | VIO_LDO_OUT | PMU | Output of on-chip I/O supply regulator, connect internally to VDDIO0.<br>Typical output: 1.8 V | VDDIO0 |
| 23 | VDD_DIGCORE_1V | Analog/PMU | On-chip LDO output for digital core | |
| 24 | VREG | Analog/PMU | DC-DC feedback pin of switch regulator | |
| 25 | VSW | Analog/PMU | DC-DC converter switching node | |
| 26 | VSS_BUCK | Analog/PMU | DC-DC converter supply and general battery GND | |
| 27 | VBAT_BUCK/VBATL | Analog/PMU | Power supply: 2.4 V to 3.8 V | |
| 28 | LFXO_32K_OUT | PMU | Output of inverting amplifier connected to 32.768 kHz crystal | |

| Pin # | Pin Name | Pin Type | Description/Default Function | Voltage Domain |
|---|---|---|---|---|
| 29 | LFXO_32K_IN | PMU | Input of inverting amplifier connected to 32.768 kHz crystal | |
| 30 | MSIO_4 | Mixed Signal I/O | Configurable mixed-signal I/O with digital I/O and analog I/O | VBATL |
| 31 | MSIO_3 | Mixed Signal I/O | | |
| 32 | MSIO_2 | Mixed Signal I/O | | |
| 33 | MSIO_1 | Mixed Signal I/O | | |
| 34 | MSIO_0 | Mixed Signal I/O | | |
| 35 | TEST_MODE | Analog/RF | Input pin, used for factory test mode selection<br>• 1: factory test mode<br>• 0: normal operation mode<br>**Note:**<br>In practice, the value is set to 0 and the pin is connected to GND by default. | |
| 36 | AON_GPIO_0 | Digital I/O | Always-on GPIO; can wake up chip from sleep modes | VDDIO0 |
| 37 | AON_GPIO_1 | Digital I/O | | |
| 38 | AON_GPIO_2 | Digital I/O | | |
| 39 | AON_GPIO_3 | Digital I/O | | |
| 40 | AON_GPIO_4 | Digital I/O | | |
| 41 | AON_GPIO_5 | Digital I/O | | |
| 42 | AON_GPIO_6 | Digital I/O | | |
| 43 | XQSPI_M_CS_N | Digital I/O | Connected to an external Flash | |
| 44 | XQSPI_M_IO_3 | Digital I/O | | |
| 45 | XQSPI_M_CLK | Digital I/O | | |
| 46 | XQSPI_M_IO_2 | Digital I/O | | |
| 47 | XQSPI_M_IO_1 | Digital I/O | | |
| 48 | XQSPI_M_IO_0 | Digital I/O | | |
| 49 | GPIO_24 | Digital I/O | General purpose I/O | |
| 50 | GPIO_25 | Digital I/O | | |
| 51 | GPIO_16 | Digital I/O | | |
| 52 | GPIO_30 | Digital I/O | | |
| 53 | GPIO_26 | Digital I/O | | |
| 54 | VDD_AMS | Analog/RF | AMS supply: 1.1 V. Connect to VREG. | |
| 55 | HFXO_32M_OUT | Analog/RF | Output of inverting amplifier connected to 32 MHz crystal | |
| 56 | HFXO_32M_IN | Analog/RF | Input of inverting amplifier connected to 32 MHz crystal | |

**Note**:

- The pad drive strength for GPIO and AON_GPIO pins can be configured to 4 mA under 3.3 V voltage.
- The pad drive strength for MSIO pins can be configured to 2 mA under 3.3 V voltage.

# 3 Minimal Design for GR5525 SoC

The absolute necessary sections required for the GR5525 SoC minimal system operation include

- Power supply
- Clock
- RF
- I/O pins
- SWD interfaces
- External Flash

To ensure the proper operation of a GR5525 SoC, the design guidelines for the schematic diagram and the PCB layout are illustrated in the following sections.

## 3.1 Schematic Design Guideline

For the minimal schematic for a GR5525 SoC, see “Section 4.1 Reference Schematic Diagram”.

### 3.1.1 Power Supply

#### 3.1.1.1 Introduction

GR5525 SoCs are powered by external power sources through VBATL (voltage range: 2.4 V to 3.8 V).

To avoid the switch overshoot caused by battery welding, connect the battery to a resistor (0.39 Ω – 1 Ω) and VBATL in series when powering on a GR5525 SoC in operation. It is recommended to convert the battery voltage to 3.3 V with LDO or DC-DC before supplying VBATL.

Figure 3-1 shows the power management unit (PMU) in a GR5525 SoC.

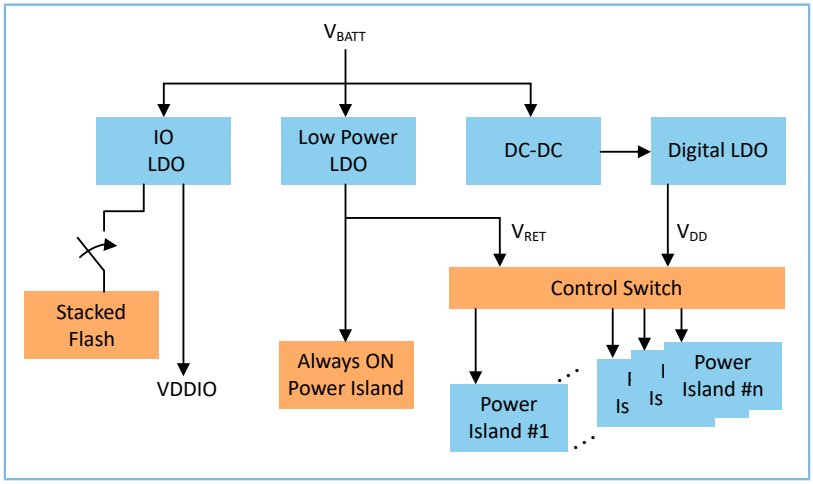


Figure 3-1 GR5525 PMU block diagram

PMU is responsible for generating all required voltages for different blocks in GR5525.

 

- I/O LDO supplies on-chip Flash (except for GR5525I0NI) and I/O pins. For more information, see "Section 3.1.1.3 I/O LDO".
- For active mode, a DC-DC converter generates the voltage for the transceiver and an LDO regulator generates the voltage for digital blocks.
- GR5525 uses an LDO regulator to supply its Always-ON (AON) modules that stay ON when both the MCU subsystem and the Bluetooth LE subsystem are OFF. The LDO regulator also generates a lower voltage for content retention to the memories where their content is needed after wake-up.
- Both the retention voltage and the digital voltage are connected to all power islands through a control switch matrix on the chip.

### 3.1.1.2 Power-on Sequence

The figure below shows the power-on sequence for GR5525.

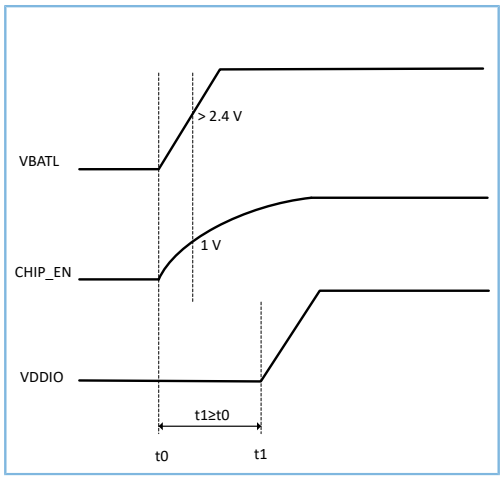


Figure 3-2 GR5525 power-on sequence

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**Note**:

- After power-on, when CHIP_EN reaches 1 V, VBATL shall be above 2.4 V.
- Do not power on VDDIO before VBATL.
- When GR5525 works as Slave, VBATL cannot be powered on after CHIP_EN is pulled low. Otherwise, the I/O state might be out of control and forced to output high level.

---

In GR5525 applications where devices are supplied by rechargeable batteries but the charger does not support power path management (PPM), when the battery is recharged after its voltage decreases to 0 V (battery depletion due to self-discharge in long-term shipping or storage), the system will fail to be started because it fails to follow the power-on sequence. To avoid this problem, it is recommended to follow the charger solutions below:

 

- Using a charger with PPM

  To use a charger that supports system power path management, follow the recommended circuit design in Figure 3-3.

  - The battery charging path and the system power supply path can be managed independently: When battery voltage drops to 0 V, connect the charger with an external power source from the USB port. After the input power going through Qbypass and Qrvs, the voltage $V_{SYS}$ supplies the system, and the Vbat controlled by Qswitch supplies the 0 V battery.
  - When charging starts, $V_{SYS}$ will instantly rise to the pre-set value, and GR5525 VBATL will also instantly reach the operating voltage or above. The system can keep working normally in this case, thanks to the delay circuit on CHIP_EN that helps ensure GR5525 power-on sequence.

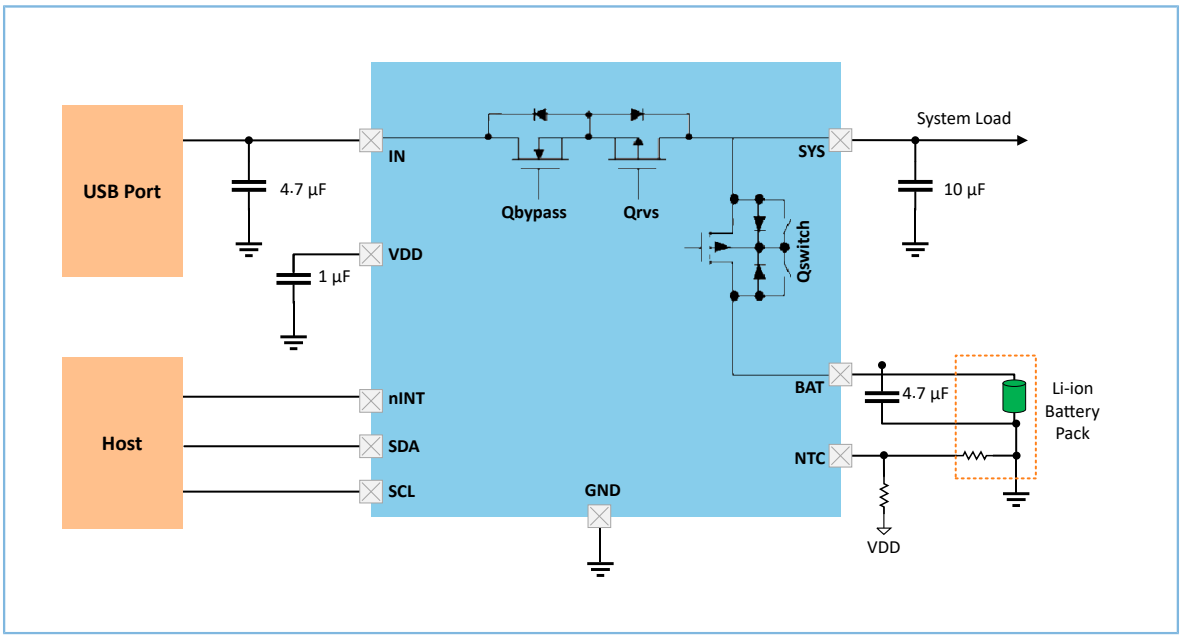


Figure 3-3 Reference design for charger with PPM

- Using a charger without PPM

  To use a charger that does not support PPM, you can add an external circuit for power path management, as shown below.

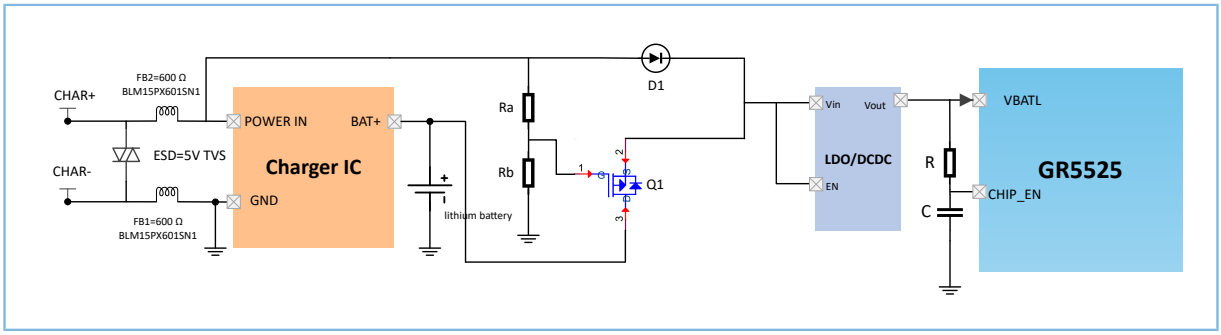


Figure 3-4 Reference design for charger not supporting PPM

- Power supply path in uncharged state

  In uncharged state, the battery conducts through the body diode of the PMOS transistor (Q1) to the LDO input (Vin pin), providing a high voltage to the source voltage (Vs) of Q1. By setting the gate voltage (Vg) of Q1 to 0 V with the pull-down of resistor Rb, Q1 is fully turned on, enabling the battery to power the subsequent system (such as the LDO). Additionally, a diode (D1) is used for reverse protection to prevent leakage current.

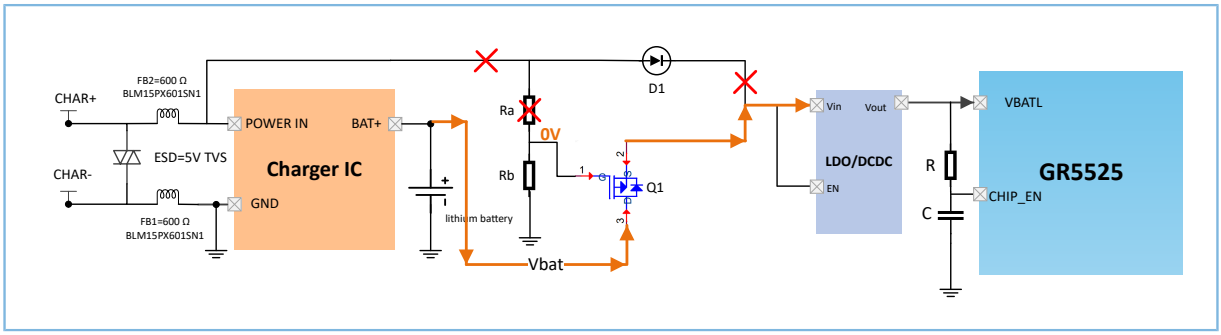


Figure 3-5 Power supply path in uncharged state

- Power supply path in charging state or fully charged state

  In charging state, the 5 V USB power source is stepped down through the diode D1 (assuming a voltage drop of 0.7 V) and outputs 4.3 V to power the system LDO. The gate voltage (Vg) of Q1 is divided by resistors Ra and Rb (typical values: Ra = 4.7 kΩ, Rb = 47 kΩ) to 4.54 V; the source voltage (Vs) of Q1 is 4.3 V. In this case, the voltage difference (Vgs) between the gate and source of Q1 is 0.24 V, Q1 is in off state, and the battery is in charging state and will not discharge.

  In fully charged state, the voltage difference (Vsd) between the source and drain of Q1 is 0.1 V, and the internal body diode cannot conduct, so Q1 remains in off state, preventing the battery from supplying the system. In this case, the system is supplied by the external USB power source.

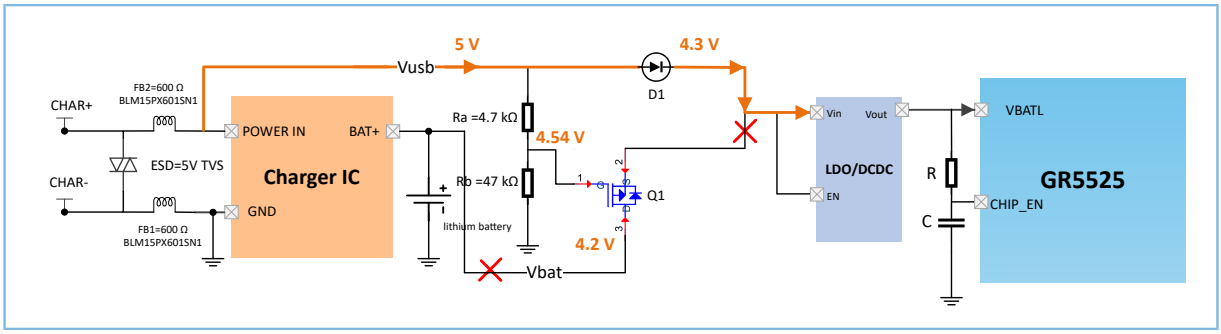


Figure 3-6 Power supply path in charging state or fully charged state

The reference formulas for voltage calculation are as follows:

Vg = Vusb * Rb / (Ra + Rb) = 4.54 V

Vs = Vusb – Vdiode = 4.3 V

Vd = Vbat = 4.2 V (Max.)

Vgs = Vg – Vs = 0.24 V

Vsd (Min.) = Vs – Vd (Max.) = 0.1 V

Recommended PMOS transistors and diodes are detailed as follows:

Table 3-1 Recommended PMOS transistor (Q1)

| Part Number | Vgs(th) | Id | Rds(on) @Vgs = –2.5 V | Footprint Reference | Manufacturer |
|---|---|---|---|---|---|
| CJBB3139K | > –0.35 V (typical) | –0.66 µA | 780 mΩ | DFN1006-3L-A | JSET |
| NTK3139P | > –0.45 V (typical) | –1 µA | 520 mΩ | SOT-723 | ON Semiconductor |

Table 3-2 Recommended diode (D1)

| Part Number | Vf | Ir | Footprint Reference | Manufacturer |
|---|---|---|---|---|
| 1N4148WT | 0.715 V (typical) | 1 µA @Vr =75 v | SOD-523 | DIODES |
| BAS716 | 0.77 V (typical) | 5 nA @Vr =75 v | SOT-523 | NXP |

**Tip**:

- Choose a diode with an appropriate voltage drop according to the requirements on system power supply.
- Resistances of Ra and Rb can be set according to the parameters of Q1.
- The current carrying capacity of the USB charging adapter should be greater than the sum of the system current and the charging current.

#### 3.1.1.3 I/O LDO

The GR5525 has an on-chip linear LDO regulator that supplies on-chip Flash at a nominal value of 1.8 V by default (and also supplies the external Flash through VIO_LDO_OUT), as well as the chip's I/O (the VDDIO0 pins). Additionally, this regulator can supply external components (sensors) which interfaces to the GR5525. The LDO is capable of supplying up to 30 mA load current.

The output of this regulator is the VIO_LDO_OUT pin. A 1 µF decoupling capacitor should be placed close to this pin.

Three I/O voltage domains are provided for GR5525: two digital voltage domains (VDDIO_0 and VDDIO_1), as well as one mixed signal I/O domain MSIO, corresponding to reference voltage levels at VDDIO_0, VDDIO_1, and VBATL respectively. Figure 3-7 is a circuit diagram showing the connection between VIO_LDO_OUT and the I/O domains.

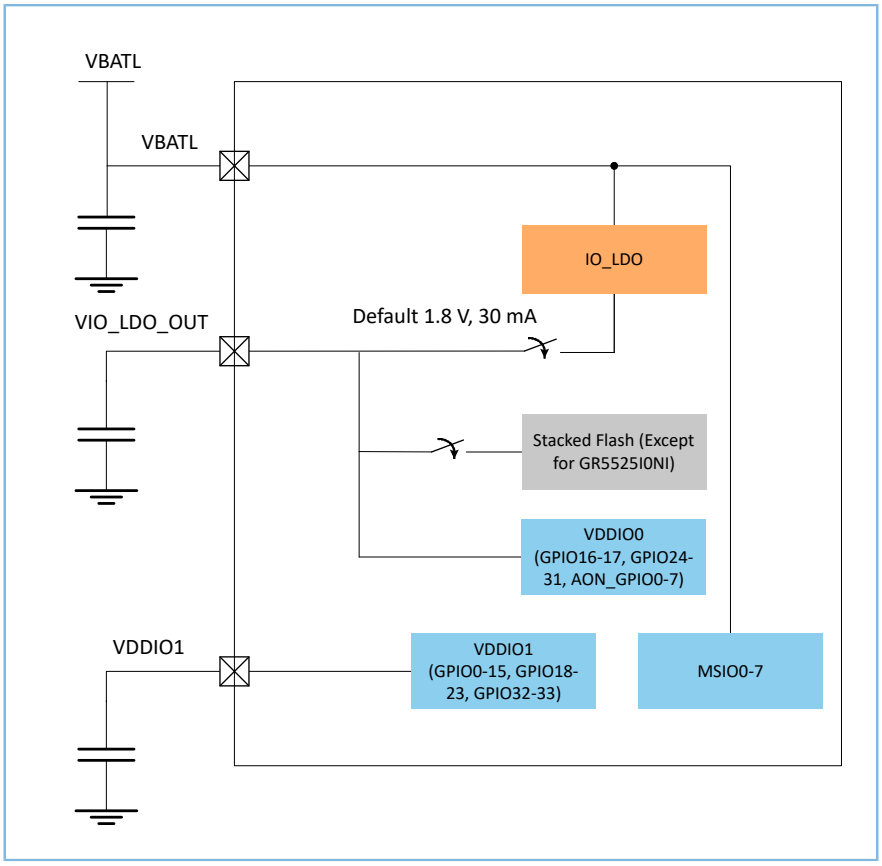


Figure 3-7 Connection between VIO_LDO_OUT and I/O domains

**Note**:

- Voltage supply from I/O LDO is adjustable within the range of 1.8 V to 3.0 V (default: 1.8 V) by software configuration.
- VDDIO_0 is connected to VIO_LDO_OUT internally, and is not bonded to any package pins.
- The power source of VDDIO_1 can be either VIO_LDO_OUT or an external power supply (typical voltage range: 1.8 V–3.3 V). When VDDIO_1 is powered by VIO_LDO_OUT, VDDIO_1 needs to be connected to VIO_LDO_OUT outside the chip.
- When VDDIO_1 is powered by an external source, the GPIO levels of VDDIO_1 vary, depending on the source voltage level.
- The leakage current of I/O LDO is approximately 0.7 µA.
- The input voltage of VDDIO_0 (VIO_LDO_OUT) and VDDIO_1 cannot exceed VBATL.
- The voltage domain VDDIO_1 supplies GPIO_0 – GPIO_15, GPIO_18–GPIO_23 and GPIO_32–GPIO_33; VDDIO_0 supplies GPIO_16 – GPIO_17, GPIO_24 – GPIO_31 and AON_GPIO_0 – AON_GPIO_7.

#### 3.1.1.4 Power Supply Scheme

GR5525 SoCs are equipped with a complete set of power management modules, which guarantee the smooth and secure functioning of the GR5525 SoCs. This section introduces the GR5525 reference circuit design by taking a GR5525 SoC in QFN68 package as an example (see Figure 3-8).

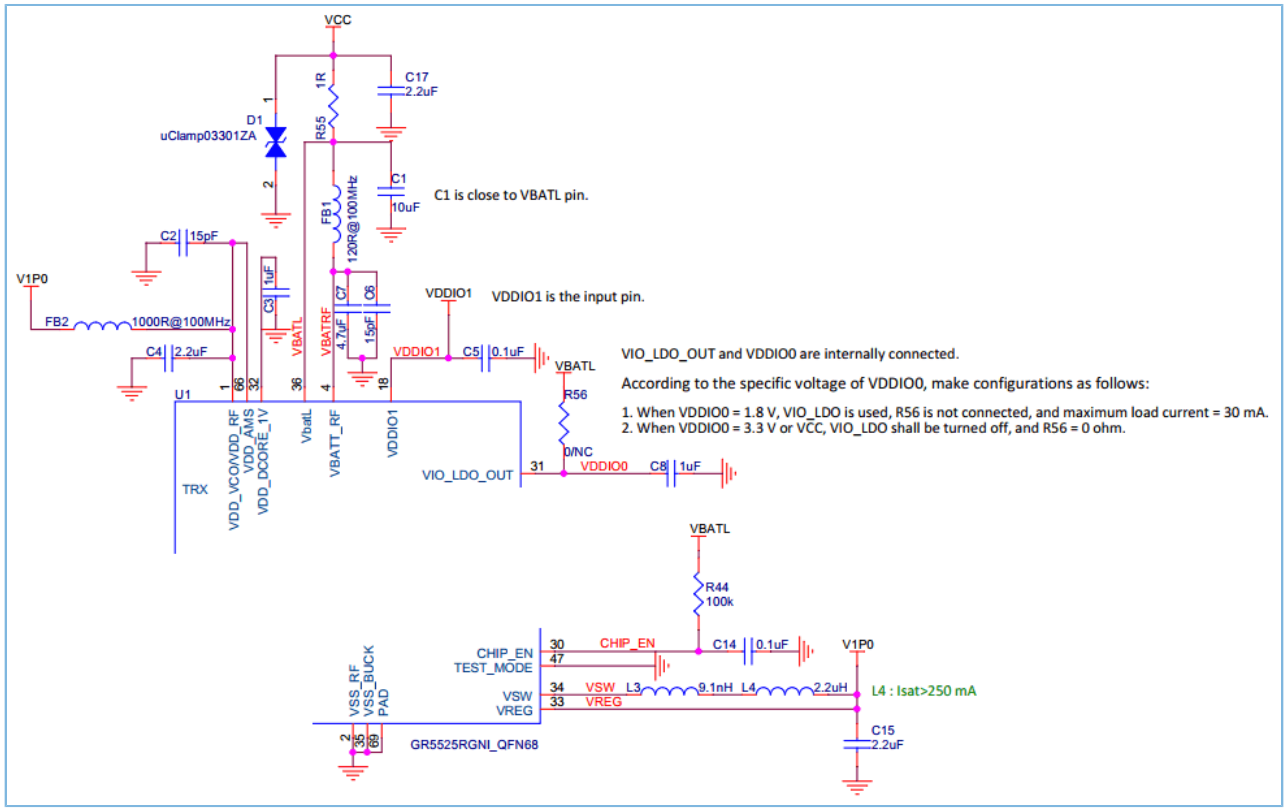


Figure 3-8 Power section of GR5525

The detailed pin descriptions and connection guidance are as follows:

- **VDD_VCO/VDD_RF:** internal RF block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 2.2 µF filter capacitor
- **VDD_AMS:** internal analog block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 15 pF filter capacitor
- **VDD_DIGCORE_1V:** output of digital LDO, which supplies the digital core logic. Place a 1 µF filter capacitor on this pin.
- **VBATL:** input supply for chip – ranging from 2.4 V to 3.8 V; typical value: 3.3 V; connected to a 10 µF filter capacitor
- **VBATT_RF:** connected to VBATL; connected to a 4.7 µF/15 pF filter capacitor
- **VIO_LDO_OUT:** output of the on-chip VDDIO LDO regulator (connected to VDDIO0 internally by default), which is used to supply the on-chip Flash. Typical output voltage: 1.8 V. It can also supply the VDDIO pins and external sensors with up to 30 mA load current. Connected to a 1 µF decoupling capacitor
- **VSW:** DC-DC switching regulator output, connected to two inductors in series: a 9.1 nH inductor for reducing RF interference caused by switching noise and a 2.2 µH power inductor, as well as a 2.2 µF capacitor, to supply the SoC from V1P0 as a complete DC-DC circuit. The pin is also connected to VDD_VCO/VDD_RF and VDD_AMS through external circuits.
- **VREG:** feedback pin from the DC-DC switching regulator output, connected to V1P0

- **VDDIO1:** supply pin for I/O1 voltage domain, supplied from VIO_LDO_OUT or external regulator, connected to a 0.1 µF filter capacitor

Recommended capacitors, ferrite beads, and inductors are listed in following tables.

Table 3-3 Recommended decoupling capacitors and ferrite beads for the power section

| Reference | Description | Value | Package | Mfg Part # |
|---|---|---|---|---|
| C15 | CAP, CER, X5R, 2.2 µF (±10%), 6.3 V | 2.2 µF | 0603 | Murata GRM188R61C225KE15D |
| C5, C14 | CAP, CER, X7R, 0.1 µF (±10%), 10 V | 0.1 µF | 0402 | Murata GRM155R71A104KA01D |
| C3, C8 | CAP, CER, X5R, 1 µF (±10%), 6.3 V | 1 µF | 0402 | Samsung CL05A105KO5NNNC |
| C4 | CAP, CER, 2.2 µF (±10%), X5R, 10 V | 2.2 µF | 0402 | Murata GRM155R61A225KE95D |
| C1 | CAP, CER, X5R, 10 µF (±20%), 10 V | 10 µF | 0603 | Murata GRM188R61A106ME69 |
| C2, C6 | CAP, CER, NPO, 15 pF (±5%), 50 V | 15 pF | 0402 | Murata GRM1555C1H150JA01D |
| C7 | CAP, CER, 4.7 µF (±10%), X5R, 10 V | 4.7 µF | 0402 | Murata GRM155R61A475KEAAD |
| FB1, FB2 | Ferrite bead, 120 Ω @ 100 MHz, 400 mA, 500 mΩ, 0603 | 120 Ω @ 100 MHz | 0603 | Murata BLM18AG121SN1 |

Table 3-4 DC-DC inductors (9.1 nH) recommended for use

| Reference | Value | DC Resistance (Max) | Saturation Current | Size L x W x H (mm) | Mfg Part # |
|---|---|---|---|---|---|
| L3 | 9.1 nH | 0.32 Ω | 300 mA | 1.0 x 0.5 x 0.5 | Murata LQG15HS9N1J02D |

Table 3-5 DC-DC inductors (2.2 µH) recommended for use

| Reference | Value | DC Resistance (Typ) | Saturation Current | Size L x W x H (mm) | Mfg Part # |
|---|---|---|---|---|---|
| L4 | 2.2 µH ± 20% | 0.3 Ω | 250 mA | 1.6 x 0.8 x 0.8 | Sunlord MPH160809S2R2 |
| | | 0.2 Ω | 250 mA | 1.6 x 0.8 x 0.8 | Murata LQM18PN2R2MGH |
| | | 0.38 Ω | 300 mA | 1.6 x 0.8 x 0.8 | Murata LQM18PN2R2MFH |

The 2.2 µH DC-DC inductors are adopted in DC-DC buck converter circuits in Pulse Skip Mode (PSM) and play a crucial role in these circuits. The saturation current of the circuit shall be higher than 250 mA. To ensure secure operation and to improve the performance of GR5525, inductors with higher saturation current and lower direct current resistance are preferred, because a higher direct current resistance means higher power consumption.

## 3.1.2 Clock

### 3.1.2.1 Introduction

GR5525's clock source is generated by an external 32 MHz crystal oscillator, and the real-time clock by an external 32.768 kHz crystal oscillator.

### 3.1.2.2 32 MHz Clock (XO)

The system clock, or CPU clock, is provided by an external 32 MHz crystal oscillator. Table 3-6 shows the specification for the crystals that can be used for these applications, and Table 3-7 shows some recommended component examples.

Table 3-6 GR5525 crystal specifications

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Crystal Freq | Crystal oscillator frequency | - | - | 32 | - | MHz |
| ESR | Equivalent series resistance | - | - | - | 100 | ohm |
| $C_{load}$ | Load capacitance | - | 6 | - | 8 | pF |
| f-Xtal | Crystal frequency initial tolerance | - | - | - | ±50 | ppm |
| f-Xtal | Crystal frequency tolerance – over temperature | - | - | - | ±30 | ppm |
| f-Xtal | Crystal frequency tolerance – aging over life of product | - | - | - | ±10 | ppm |
| $P_{DRV}$ | Max drive power | - | - | - | 100 | µW |

Table 3-7 Recommended 32 MHz crystal examples

| **Part Number** | Abracon<br>ABM10W-32.0000MHZ-6-D1X-T3 | TAITIEN G0068-X-006-3 | Murata<br>XRCGB32M000F5N10R0 | TXC 8Z32000004 |
|---|---|---|---|---|
| **Frequency** | 32 MHz | 32 MHz | 32 MHz | 32 MHz |
| **Initial tolerance** | ±10 ppm | ±40 ppm | ±50 ppm | ±10 ppm |
| **Tolerance over Temp.** | ±20 ppm | ±30 ppm | ±30 ppm | ±20 ppm |
| **Load capacitance** | 6 pF | 6 pF | 6 pF | 8 pF |
| **ESR** | 70 ohm | 30 ohm | ≤ 100 Ω | ≤ 60 Ω |
| **Temperature range** | –40°C to +85°C | –40°C to +105°C | –40°C to +85°C | –40°C to +85°C |
| **Size (L x W x H, mm)** | 2.5 x 2.0 x 0.60 | 2.5 x 2.0 x 0.60 | 2.0 x 1.6 x 0.60 | 2.5 x 2.0 x 0.60 |

**Note**:

- To ensure system stability and low power consumption, load capacitance of the 32 MHz crystal oscillator should be within the range from 6 pF to 8 pF. The 32 MHz crystal oscillator does not need to be connected with load capacitors, but it needs to use the production tool for frequency offset calibration.
- When designing an application circuit, reserve the interface or test points (SWDCLK, SWDIO, CLK_TRIM (any GPIOs except MSIOs), GND, VBAT) required by the mass production tool.

### 3.1.2.3 32.768 kHz Clock

The GR5525 uses a low-power, low-frequency clock in sleep modes, which also extends battery lifespan. The utilization of the external 32.768 kHz crystal oscillator provides tighter timing and better accuracy, resulting in lower overall power consumption.

The GR5525 integrates an adjustable load capacitor, and typically no external load capacitors are required.

The external crystal must meet the recommended operating conditions as indicated in Table 3-8, and Table 3-9 shows examples of crystals that meet the specifications.

Table 3-8 32.768 kHz crystal oscillator recommended operating conditions

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Crystal Freq | Crystal oscillator frequency | - | - | 32.768 | - | kHz |
| ESR | Equivalent series resistance | - | - | - | 100,000 | ohm |
| $C_{load}$ | Load capacitance | - | 6 | - | 9 | pF |
| f-Xtal | Crystal frequency initial tolerance | - | - | - | ±50 | ppm |
| f-Xtal | Crystal frequency tolerance – over temperature and aging | - | - | - | ±250 | ppm |
| PDRV | Max drive power | - | - | - | 0.5 | µW |

Table 3-9 32.768 kHz crystal oscillator example specifications

| | |
|---|---|
| **Part Number** | Abracon ABS05-32.768KHZ-9-T |
| **Frequency** | 32.768 kHz |
| **Initial tolerance** | ±20 ppm |
| **Tolerance over Temp.** | ±250 ppm |
| **Load capacitance** | 9 pF |
| **ESR** | 90,000 ohm |
| **Temperature range** | –40°C to +85°C |
| **Size (L x W x H, mm)** | 1.6 x 1.0 x 0.50 |

**Note**:

To ensure system stability and low power consumption, load capacitance of the 32.768 kHz crystal oscillator shall be within the range from 6 pF to 9 pF.

## 3.1.3 RF

### 3.1.3.1 Introduction

Figure 3-9 shows the functional block diagram of a GR5525 transceiver.

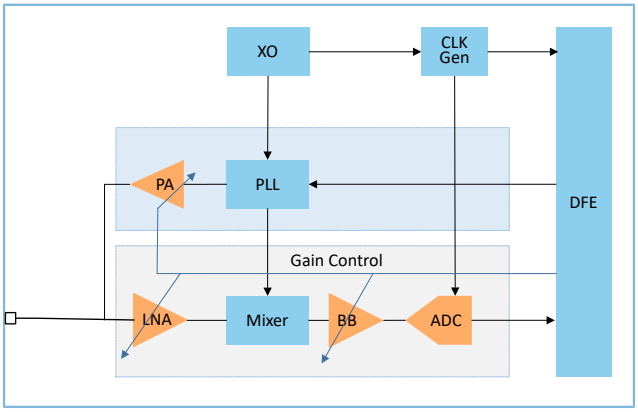


Figure 3-9 GR5525 transceiver architecture

Operating mechanisms:

- On the receiver side:
  1. After the antenna receives an RF signal, the receiver digitizes the signal in a path: Low noise amplifier (LNA) > Mixer > Baseband (BB) amplifier > an analog-to-digital converter (ADC).
  2. The digitized signals are sent to the digital frontend (DFE) for demodulation.
  3. The digital frontend provides Automatic Gain Control (AGC) feedback signals to adjust the gain of the LNA and BB amplifier to maximize the signal-to-noise ratio (SNR) at the demodulation.
- On the transmitter side:
  1. The digital signal from the DFE is transmitted to a phase-locked loop (PLL) for modulation.
  2. The modulated carrier wave is delivered to a power amplifier (PA) with amplification factor configurable by the digital gain settings.
  3. The modulated carrier is transmitted to the antenna through a low-power or high-power PA path. The antenna radiates the amplified carrier wave through electromagnetic waves.

**Note**:

RF and digital clocks are generated from the HFXO_32M.

### 3.1.3.2 RF Scheme

The following figure is the recommended RF matching circuit in the GR5525 SoC minimal system, by taking a GR5525 SoC in QFN56 package as an example.

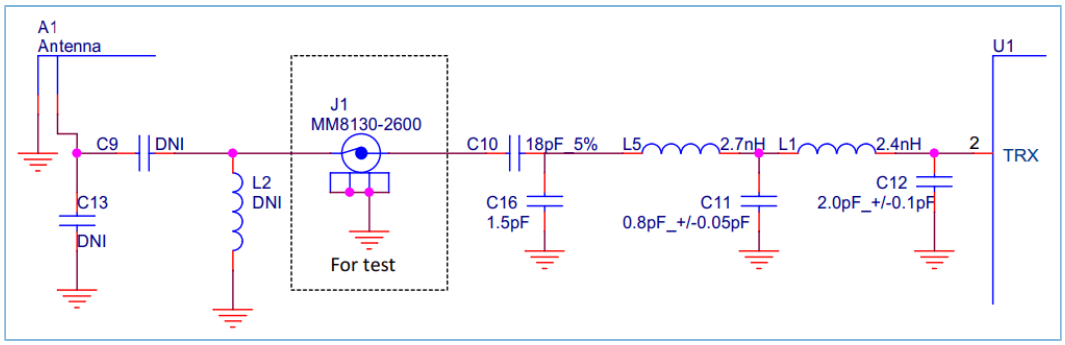


Figure 3-10 RF scheme (QFN56 package)

Two matching networks are recommended for the RF TRX path from the TRX pin to the antenna, to achieve matching of PA output impedance to antenna impedance.

- Antenna matching network

  In the circuit, the left PI matching network (composed of the inductor L2 plus capacitors C9 and C13) matches the antenna. Values of the matching component are adjusted according to the actual antenna used. It is recommended to use mature antenna schemes and recommended values from antenna manufacturers.

- SoC matching network

  The right PI type matching network (composed of the inductors L1 and L5 plus capacitors C11, C12 and C16) matches the internal PA of GR5525. The network connects to the TRX pin of the chip.

The two matching networks are connected by the DC blocking capacitor C10.

Recommended configurations of the capacitors and inductors are displayed in Table 3-10.

Table 3-10 Recommended components for the RF section

| Reference | Description | Value | Package Size | Mfg Part # |
|---|---|---|---|---|
| C10 | CAP, CER, NPO, 18 pF (±5%), 50 V | 18 pF | 0402 | Murata GRM1555C1H180JA01D |
| C11 | CAP, CER, NPO, 0.8 pF (±0.05 pF), 50 V | 0.8 pF | 0402 | Murata GRM1555C1HR80WA01D |
| C12 | CAP, CER, NPO, 2.0 pF (±0.1 pF), 50 V | 2.0 pF | 0402 | Murata GRM1555C1H2R0BA01D |
| C16 | CAP, CER, C0G, 1.5 pF (±0.1 pF), 50 V | 1.5 pF | 0201 | Murata GRM0335C1H1R5BA01D |
| L1 | Inductor, Wirewound, 2.4 nH (±0.2 nH), 50 mohm, Q = 20 @ 250 MHz | 2.4 nH | 0402 | Murata LQW15AN2N4B00 |
| L5 | Inductor, 2.7 nH (±0.1 nH), 120 mΩ, Q = 14@500 MHz | 2.7 nH | 0402 | Murata LQG15HS2N7B02D |

## 3.1.4 I/O Pins

The GR5525 has software-configurable I/O pin assignment where different peripherals can be multiplexed out on different chip pins. When configured to GPIOs, they can be set as input, output, with configurable pull-up or pull-down resistors. I/O pins retain their last state when system enters the sleep or deep sleep mode. Only AON_GPIOs can be used to wake up the system from sleep/deep sleep mode.

**Note**:

- For more details of pin mux, refer to *GR5525 Datasheet*.
- Note that MSIO pins do not support hardware interrupt when allocating I/O functions during designing PCB applications.
- Two PWM modules (PWM0 and PWM1) are provided, with each containing three separate output channels: PWMA, PWMB, and PWMC. Frequencies of the three PWM channels in one group are the same, and individual frequency control is not supported. Phase and duty cycle of each channel can be configured via registers.
- Make sure the input voltages of VDDIO_1 and VIO_LDO_OUT (VDDIO_0) do not exceed the VBATL voltage.
- Make sure the sink voltages of all I/Os (GPIOs, MSIOs, and AON IOs) do not exceed the VBATL voltage.

### 3.1.5 SWD Interfaces

GR5525 connects to J-Link for modulation by using Serial Wire Debug (SWD) interfaces.

Table 3-11 shows the pins to which the SWD interfaces connect in QFN68 and QFN56 packages.

Table 3-11 Pin matching for SWDCLK and SWDIO in QFN68 and QFN56 packages

| SWD | Pin # (QFN68) | Pin # (QFN56) |
|---|---|---|
| SWD_CLK | Pin 5 | Pin 4 |
| SWD_IO | Pin 6 | Pin 5 |

The pins can be multiplexed as GPIOs when the SWD interfaces are not in use.

### 3.1.6 Flash

Most GR5525 members provides embedded Flash, with only one exception (GR5525I0NI) which uses external Flash. Details about the Flash of the GR5525 series are provided below.

Table 3-12 GR5525 Flash details

| Part Number | GR5525RGNI | GR5525IENI | GR5525I0NI |
|---|---|---|---|
| Flash Type | Internal | Internal | External |
| Voltage Features | Wide voltage<br>Range: 1.65 V–3.6 V | Wide voltage<br>Range: 1.65 V–3.6 V | Low & high voltage<br>• Low (Typ.): 1.8 V<br>• High (Typ.): 3.3 V |

- **Power source:**

- I/O LDO: Both embedded Flash and external Flash can be supplied by the on-chip LDO regulator (I/O LDO), with the typical LDO output voltage at 1.8 V.

  On-chip Flash is connected to I/O LDO internally. To supply the external Flash, connect VIO_LDO_OUT to the power input of the external Flash.

- External power supply: as specified in the option 1 below

- **High voltage scenario application**:

  For GR5525 members embedded with wide-voltage Flash and for GR5525I0NI, to use the SoCs in high-voltage scenarios, make sure to:

  1. Set I/O LDO to off mode in eFuse, and use an external power supply. Use VIO_LDO_OUT as input for the VDDIO_0 domain, and connect VIO_LDO_OUT to the external power supply.
  2. Alternatively, set I/O LDO to bypass mode and connect VBATL to the output of I/O LDO.

- **External Flash: model selection**

  GR5525I0NI uses an external Flash with various model options provided and supports both low-voltage (typical: 1.8 V) and high-voltage (typical: 3.3 V) Flash. Typically, GR5525 supports all generic Flash models that meet the electrical characteristics as specified in *GR5515I0NDA Flash Selection Guide*. A number of Flash models are tested, with the recommended ones listed below.

Table 3-13 Recommended GR5525I0NI series Flash candidates (high voltage)

| Flash Model | Manufacturer | Flash Size | Voltage Range (V) |
|---|---|---|---|
| P25Q128H | Puya Semiconductor | 128 Mb | 2.30–3.60 |
| W25Q64JV | Winbond | 64 Mb | 2.70–3.60 |
| XM25QH64A | XMC | 64 Mb | 2.30–3.60 |
| XT25F64B | XTX | 64 Mb | 2.70–3.60 |

Table 3-14 Recommended GR5525I0NI series Flash candidates (low voltage)

| Flash Model | Manufacturer | Flash Size | Voltage Range (V) |
|---|---|---|---|
| P25Q128L | Puya Semiconductor | 128 Mb | 1.65–2.00 |
| XT25Q64D | XTX | 64 Mb | 1.65–2.10 |

**Note**:

- Not all external Flash supports data read at 64 MHz. In such case, lower the Quad SPI data rate based on the actual Flash data transfer rate.
- In practice, the operating frequency of GR5525I0NI Flash varies depending on component package, layout, and routing of the whole system. Therefore, it is recommended that you choose a proper Flash memory that meets the electrical characteristics and functional requirements based on actual project demands.

## 3.2 PCB Design and Layout Guideline

### 3.2.1 PCB Layer Stackup

A 4-layer PCB layout is recommended to be used for all GR5525 package options. Figure 3-11 shows the recommended layer stackup (thickness: 1.6 mm) of GR5525.

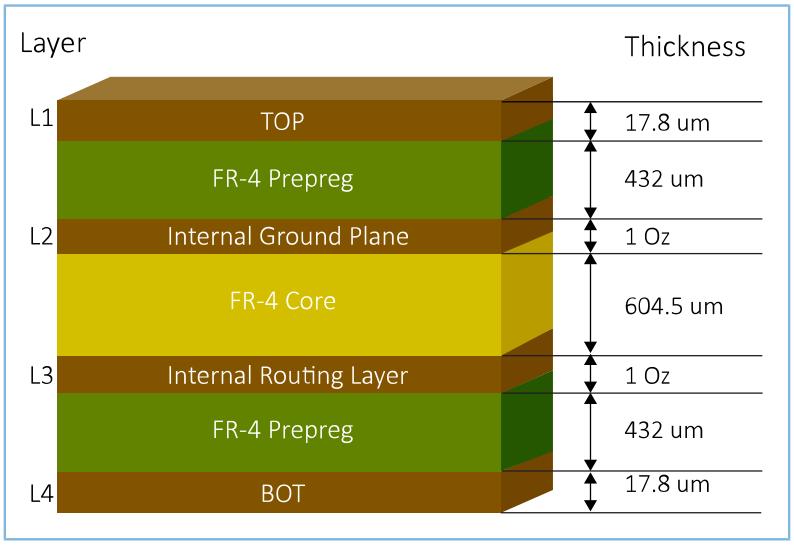


Figure 3-11 GR5525 PCB layer stackup

L1: top layer where components, RF transmission lines, and key signal lines are placed

L2: internal ground plane, used for both the ground return path and the reference plane for the 50 ohm RF transmission line

L3: internal routing layer, used to split power domains and place a small number of signal lines

L4: bottom layer where components and signal lines are placed

---

**Note**:

The customer's product design can be adjusted according to the actual situation. A typical example for designing 4-layer PCB layouts is provided in "Section 4.2.1 Four-layer PCBs", to help users quickly get started with development and PCB layout design.

For users who need to reduce costs, choose 2-layer PCBs, with special attention to the layout of power filter components, power input, the ground return path for DC-DC buck converters, and completeness of the reference plane for RF route. For details on the layout and routing, see "Section 4.2.2 Two-layer PCBs".

---

## 3.2.2 Components Layout

All components operating at high frequency should have their layout made as compact as possible. This will prevent the cross-coupling between lines and also minimize the parasitic effects which will have a negative impact on the operating parameters.

When designing the layout, make sure the main chip is as close to the antenna interface as possible, and no other components are under the RF routing if possible (the layout and routing of RF components are of higher priority).

## 3.2.3 Power Supply

Power supply is essential to ensure proper operation of an SoC, and therefore special attention should be paid on the layout and routing of the key power systems, which are DC-DC switching regulator and RF input power supply. To avoid system-level issues (such as poor performance in ESD protection and radiation off limits) caused by improper power design, abide by the design guides described in the two following sections.

### 3.2.3.1 DC-DC Switching Regulator

Take GR5525RGNI for example. The chip includes a DC-DC switching regulator. To design the PCB layout involving a DC-DC switching regulator,

1. Components (L3: 9.1 nH inductor, L4: 2.2 µH inductor, and C15: 2.2 µF capacitor) connected to DC-DC switching regulator should be placed as close to VSW and VREG of the chip as possible. A distance within 3 mm is recommended.
2. The net of VSW radiates stronger interference before VSW signals passing through the inductors, and thus should be placed at a minimum distance of 0.2 mm from other power nets and signals, especially V1P0 and VDD_DIGCORE_1V.
3. Placing L4 perpendicular to L3 is recommended, to avoid inductive coupling. C15 should be placed behind L4, and VREG network is connected to the power supply after capacitor filtering.
4. GND pin of C15 should be placed as close to VSS_BUCK of the chip as possible. Vias of C15 GND pin should be placed as close to the GND pin as possible. It is recommended to connect the C15 GND pin to VSS_BUCK by using GND Polygon Plane, so that the return path of the power can be kept minimal.

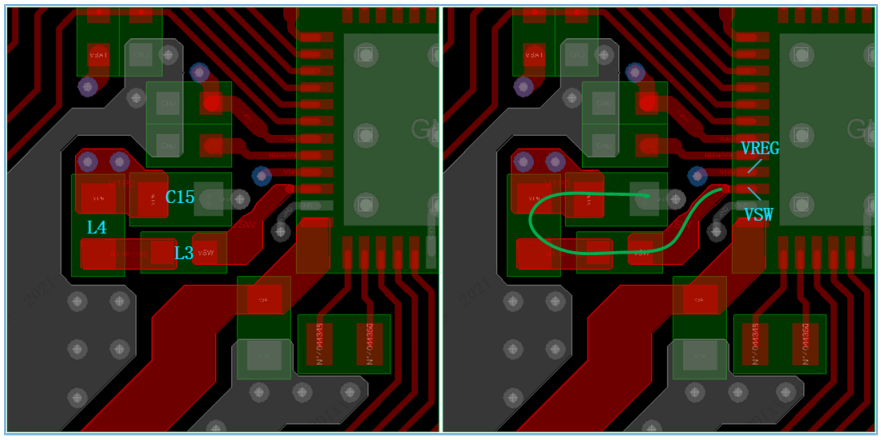


Figure 3-12 Reference layout and routing for DC-DC switching regulator

**Note**:

The green line in the right figure of Figure 3-12 indicates the power output path.

### 3.2.3.2 RF Input Power Supply

Make sure the following instructions are met when designing RF input power supply in PCB layout, to ensure optimal performance and to avoid excessively high radiation.

1. Decoupling capacitors connected to VDD_VCO/VDD_RF and VBATT_RF should be as close to the corresponding pins as possible (around 1 mm is recommended, and shall not exceed 3 mm, as shown in Figure 3-13). C4 and C5 are placed close to VDD_VCO and VDD_RF respectively, and C3 is placed close to VBATT_RF. Place the capacitors on the same layer with the pins if possible, and make sure the wiring path goes through the capacitors first and then connected to the chip power pins. In case the capacitors are not placed on the same layer with the pins, the vias should be located close to the decoupling capacitors.
2. The power trace should be as short as possible, and at least 0.2 mm wide. A minimum distance at 0.2 mm from other signals should be guaranteed.

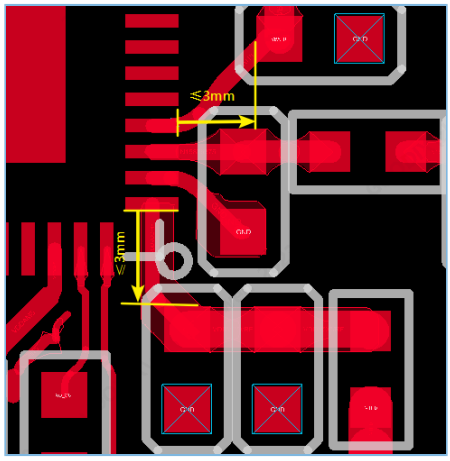


Figure 3-13 Reference layout and routing for RF input power supply

### 3.2.3.3 Digital and Analog Power Supply

Decoupling capacitors connected to digital/analog power supply pins should also be placed as close to the corresponding pins as possible, as specified below.

Table 3-15 Correlations between capacitors and digital/analog power pins

| Reference | Value | Corresponding Pin |
|---|---|---|
| C1 | 10 µF | VBATL |
| C2 | 15 pF | VDD_AMS |
| C3 | 1 µF | VDD_DIGCORE_1V |
| C5 | 0.1 µF | VDDIO_1 |
| C8 | 1 µF | VIO_LDO_OUT |

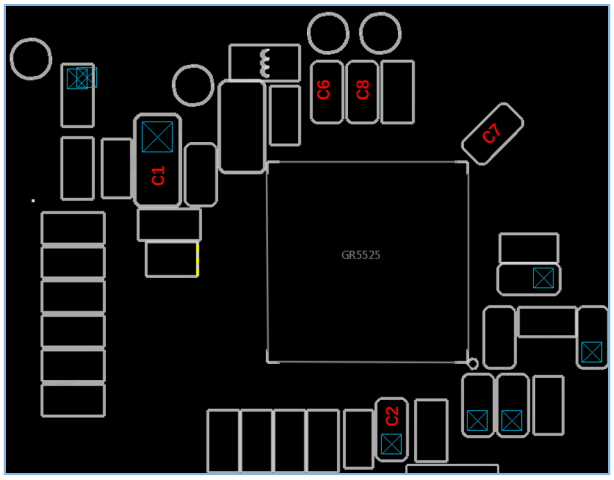


Figure 3-14 Layout reference of decoupling capacitors for digital/analog power supply pins

### 3.2.4 Clock

Place the crystal as close as possible to the IC (recommended distance: ≤4 mm). This will minimize any additional capacitive load on the input pins and reduce the chance of crosstalk and interference with other signals on the board. Make sure there is no other trace routed next to/under the crystal or the crystal routing traces.

It is recommended to shield the routing traces of the 32 MHz crystal with GND traces. If the ground below the crystal is clean and no crosstalk or interference is involved, provide openings underneath the crystal pads (as shown in Figure 3-16) to reduce parasitic capacitance.

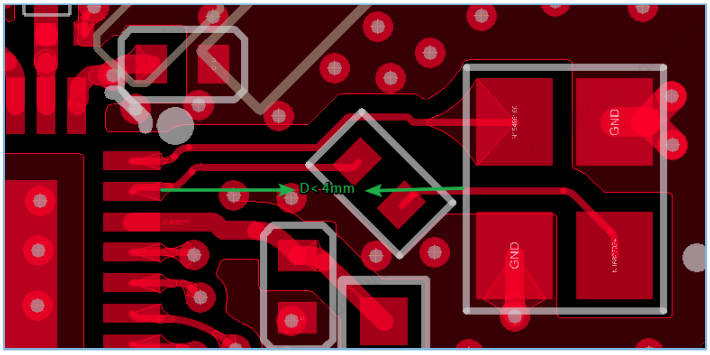


Figure 3-15 Reference clock layout

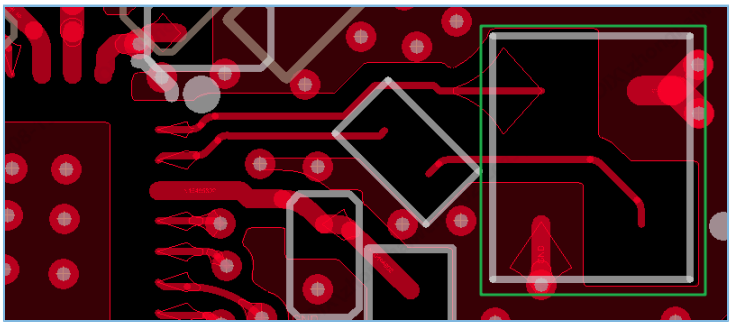

Figure 3-16 Openings under XO pads

### 3.2.5 RF Port

The GR5525 provides a single-ended RF port. A copper RF trace with a characteristic impedance of 50 Ω is required to interconnect the RF port and the antenna. Because the impedance of RF port is not 50 Ω, a matching network is required to match the port impedance between the RF port and the 50 Ω transmission line.

Components in this network must be placed as close as possible to the RF pin. Try to place the first component no further than 1 mm from the RF pin. Figure 3-17 shows the PCB layout of the RF port.

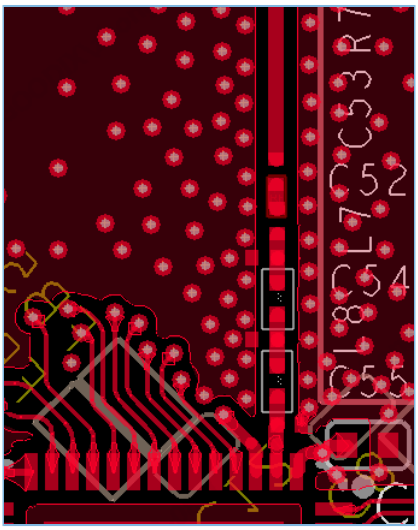

Figure 3-17 RF port PCB layout

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**Note**:

- The RF route should be straight and as short as possible. If a curving route is necessary for a specific structure, an inverted arc is required for a turning, and angles at or less than 90° are not allowed.
- RF routing at the PCB surface (the top layer or the bottom layer) helps avoid using vias or switching layers, and is therefore preferred. Avoid stub routes, and make sure the reference ground plane underneath the RF route is complete. The RF route should be of the same width as the component pad, to avoid discontinuities in the 50 Ω transmission line due to mismatch between the component pad size and trace size.

---

Taking the 4-layer PCB layout design as an example, the transmission line is routed as a coplanar waveguide using layer-2 ground as the reference plane. The dimensions are:

- Trace width: 559 µm
- Spacing from trace to top layer: 178 µm
- Spacing from top layer to layer 2: 432 µm

The design uses FR-4 dielectric and 0.5 ounce copper on the outer layer. In actual design, PCB manufacturers are required to provide single-ended RF traces with an impedance of 50 Ω (±10%).

Ground vias should be placed along the transmission line every 1.25 mm and right next to the ground pads of the matching components.

A PI-network should be placed close to the antenna feedpoint for antenna matching purposes. The matching network value of antenna is adjusted according to the actual antenna used. It is recommended to use mature antenna schemes and recommended values of antenna factories.

### 3.2.6 Grounding

Always provide a solid grounding for the radio IC of GR5525. Use as many vias as possible to create a solid GND under the IC itself and connect it to inner and bottom GND layers.

For the center ground paddle (at the package bottom), use a matrix of 3 x 3, 4 x 4, or other vias to the ground-plane.

The GND of the 10 µF filter capacitor connecting to VBATL shall be close to the main GND pin, and apply copper pouring if possible (see "Section 3.2.3 Power Supply"). The ground return path of the GND pin (VSS_BUCK) of DC-DC power shall be in good condition, which guarantees stable and secure operation of ICs.

---

**Note**:

- Make sure the ground-pad shape follows the shape of the paddle on chip, including the exposed paddle parts.
- Make sure a ground via is placed right next to the TRX pin.

---

## 3.3 ESD Protection Design

### 3.3.1 System-level ESD Design

System efficient electrostatic discharge (ESD) design is crucial for any circuits, and requires users to follow the design guidelines (including schematic diagrams, PCB layout, and product structural designs) provided in the sections below.

#### 3.3.1.1 ESD Schematic Design

1. GR5525 series is powered by an independent external LDO regulator (see "Section 3.1.1 Power Supply" for details).
2. A transient voltage suppressor (TVS) diode is connected to the VBATL pin, to improve the ESD capability of the system; recommended TVS diode model: µClamp03301ZA, with its electrical characteristics excerpted below.

Table 3-16 Electrical characteristics of µClamp03301ZA (T = 25°C unless otherwise specified)

| Parameters | Descriptions | Conditions | | Min. | Typ. | Max. |
|---|---|---|---|---|---|---|
| $V_{RWM}$ (V) | Reverse stand-off voltage | Pin 1 to 2 | | | | 3.3 |
| $V_{BR}$ (V) | Reverse breakdown voltage | $I_t$ = 1 mA, Pin 1 to 2 | | 5 | 6.5 | 8 |
| $I_R$ (nA) | Reverse leakage current | $V_{RWM}$ = 3.3 V, Pin 1 to 2 | | | <1 | 50 |
| $V_C$ (V) | Clamping voltage | tp = 1.2/50 µs (Voltage), 8/20 µs (Current) combination Waveform, $R_S$ = 2 Ω | $I_{PP}$ = 15 A, Pin1 to 2 | | 3.8 | 5.5 |
| $V_C$ (V) | ESD clamping voltage | tp = 0.2/100 ns (TLP), Pin 1 to 2 | $I_{PP}$ = 4 A | | 3.6 | |

| Parameters | Descriptions | Conditions | | Min. | Typ. | Max. |
|---|---|---|---|---|---|---|
| | | | $I_{PP}$ = 16 A | | 4.7 | |
| $R_{DYN}$ (Ohms) | Dynamic resistance | tp = 0.2/100 ns (TLP), Pin 1 to 2 | | | 0.08 | |
| $C_J$ (pF) | Junction capacitance | $V_R$ = 0 V, f = 1 MHz | | | 38 | 50 |

3. To suppress static voltages, connect a ferrite bead to each of the two charging ports (CHAR+ and CHAR-) in series, and connect a proper TVS diode between the two ferrite beads to enhance ESD protection, as shown in the figure below.

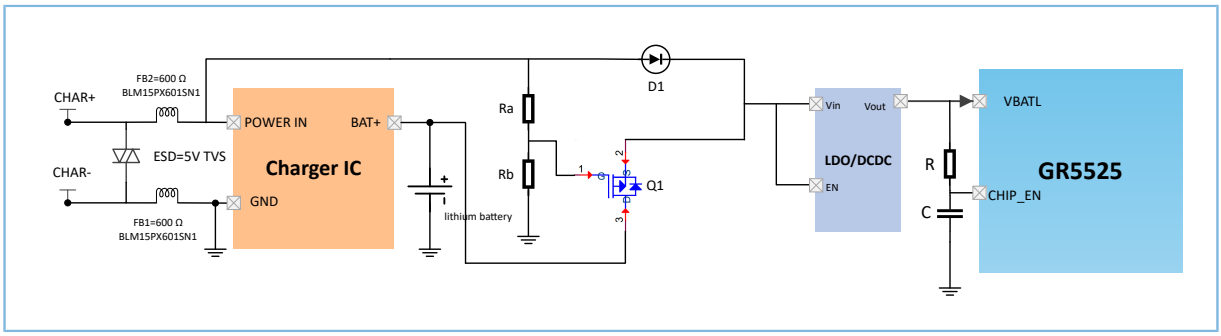



Figure 3-18 ESD protection scheme at charging pads

Recommended models of TVS diodes and ferrite beads, as well as model selection requirements, are listed in the tables below.

Table 3-17 Model selection for TVS diodes

| Parameters | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| $V_{RwM}$ (V) | Reverse stand-off voltage | - | 5 V | - |
| $V_{BR}$ (V) | Breakdown voltage | - | 7 V | - |
| $V_{clamp}$ (V) | Clamp voltage | - | 6 V | - |
| $V_{ESD}$ (kV) | ESD prevention performance | • Contact discharge: ±10 kV<br>• Air discharge: ±12 kV | - | - |

Table 3-18 Model selection for ferrite beads

| Parameters | Description | Min. | Typ. | Max. |
|---|---|---|---|---|
| Impedance@100 MHz (Ω) | Impedance @ 100 MHz | - | 600 Ω | - |
| $I_R$ (mA) | Rated operating current | - | 900 mA | - |
| $R_{DC}$ Max. (mΩ) | Maximum DC resistance | - | 230 mΩ | - |

Table 3-19 Recommended TVS diodes

| Part Number | $V_{RWM}$ (V) | $V_{BR}$ (V) | $V_{clamp}$ (V) | Operating Temperature | $V_{ESD}$ (kV) | Package | Manufacturer |
|---|---|---|---|---|---|---|---|
| AZ5C25-01B | 5 | 9 | 6 | –55°C to 85°C | • Contact discharge: ±13 kV<br>• Air discharge: ±16 kV | 0201 | Amazing Micro. |
| OVE38E32S1M | 6.5 | 7 | 10 | –55°C to 85°C | • Contact discharge: ±25 kV<br>• Air discharge: ±25 kV | 0402 | OVREG |

Table 3-20 Recommended ferrite beads

| Part Number | Impedance @100 MHz | Rated Current | Max. DC Resistance | Operating Temperature | Package | Manufacturer |
|---|---|---|---|---|---|---|
| BLM15PX601SN1 | 600 Ω | 900 mA | 230 mΩ | –55°C to 125°C | 0402 | Murata |
| WLBD1005HCU601TL | 600 Ω | 900 mA | 230 mΩ | –55°C to 125°C | 0402 | Walsin |

4. To protect products with metal shell against ESD, connect ferrite beads between metal shell GND and the GND on motherboard.
5. To protect products such as smartwatch/wristband against ESD, additional reset mechanisms (such as watchdog timeout reset) are required to enhance ESD protection.

If an external WDT needs to be included, do not start the WDT before firmware is programmed to the SoC, to avoid inadvertent system reset.

Choose WDT that meets the requirements in Table 3-21. A recommended model series is also provided.

Table 3-21 WDT requirements and recommended models

| ESD Susceptibility | WDT Reset Time $t_{WD}$ | WDT Output Reset Time $t_{RST}$ | Voltage Input Range | Operating Voltage | Operating Temperature | Recommended Model | Manufacturer |
|---|---|---|---|---|---|---|---|
| HBM > 2000 V<br>CDM > 500 V | Configurable<br>< 10s | > 100 ms | 1.6 V – 5 V | Supporting device sleep mode. No higher than 5 μA is recommended. | –40°C to 85°C | SGM820A/B-X | SGMICRO |

To reset the system by using SGM820 as the external WDT, the WDT timeout period can be set with an external capacitor.

Set WDT countdown value with SGM820A-X (standard):

$$t_{WD\_standard}(\mathrm{ms}) = 3.33 \times C_{CWD}(\mathrm{nF}) + 0.28(\mathrm{ms})$$

Set WDT countdown value with SGM820B-X (extended):

$$t_{WD\_extended}(\mathrm{ms}) = 78.3 \times C_{CWD}(\mathrm{nF}) + 51(\mathrm{ms})$$

During the reset period $t_{WD}$, after a feeding-dog pulse signal output (> 50 ns) occurs, the WDT is cleared and the system will not be reset; when an ESD event occurs and leads to software failure, the WDT cannot be cleared during $t_{WD}$. In this case, the WDT generates a reset signal (200 ms) to reset the system.

A reference schematic design of the WDT is shown in Figure 3-19. Connect nRESET to GR5525 CHIP_EN, so that the WDT can send reset signals to reboot the system in the case of software failure; connect WDI_820 to any GPIO to feed the dog.

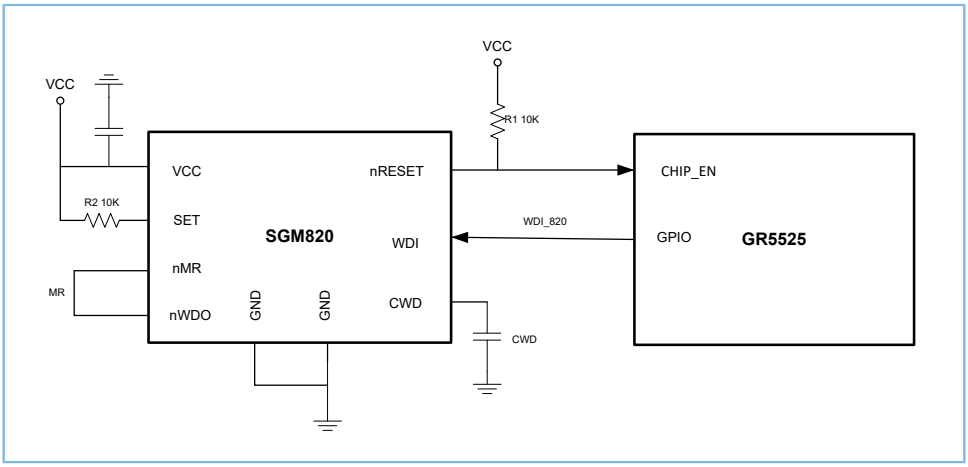



Figure 3-19 Hardware WDT schematic design (reference)

### 3.3.1.2 PCB Layout Design

1. Live by the following rules for GR5525 PCB grounding:
   - It is recommended to use PCB with four layers or above, and place a GR5525 SoC on the layer adjacent to the GND layer. Make sure the GND layer is solid and complete, to effectively prevent static from setting in.
   - Connect GR5525 GND pin to the GND pin on the top layer, and then connect the GR5525 SoC GND pin to the GND pins on the other layers through vias.
   - Make sure the GND pin of the input capacitor (10 µF) is placed as close to the VSS_BUCK pin as possible, and is connected to EPAD on other layers through at least two vias near VSS_BUCK. The trace from VSS_BUCK to the GND pin should be 0.25 mm wide or above, so as to reduce power/GND loop impedance.
2. To design the layout for charging pads,
   - It is not recommended to place charging pads (CHAR+ and CHAR-) and GR5525 SoC on the same layer. However, if the charging pads and GR5525 SoC are on the same layer, a minimum distance between the two at 4 mm should be guaranteed.

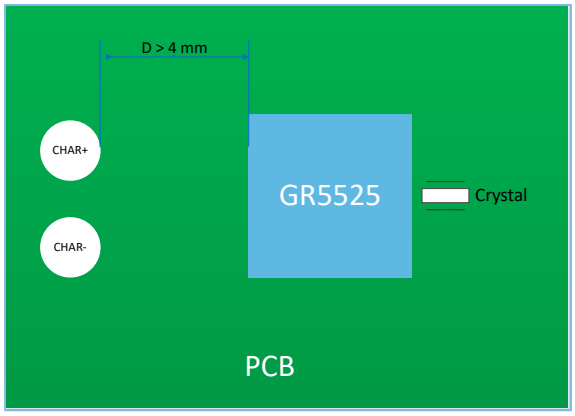



Figure 3-20 Charging pads layout

- Do not place charging pads close to ESD sensitive signals (including clock, reset, and communication signals). Those signals shall also be shielded with ground traces.

3. Place filter capacitors as close to the power pins of GR5525 as possible, to keep the power return path minimal, so as to enhance filtering performance.

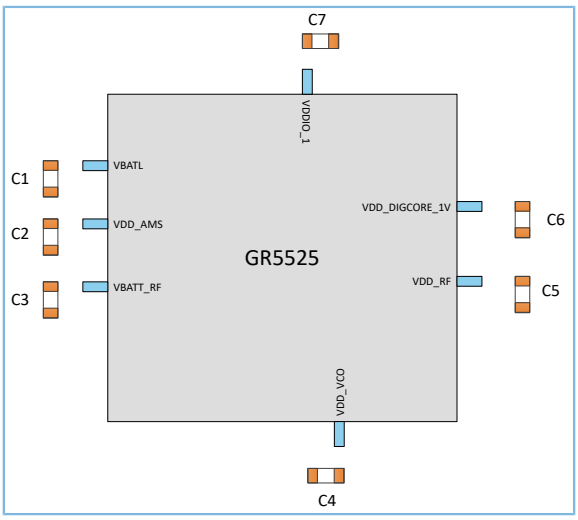



Figure 3-21 Filter capacitor layout for power supply

4. It is recommended to place communication signals neither on the top layer nor the bottom layer in the PCB stack-up, due to the ESD susceptibility of I/O pins. Avoid routing signals susceptible to ESD events (such as clocks and reset pins) at the edge of the board. It is recommended to shield the I/O pins and ESD susceptible signals with GND traces.

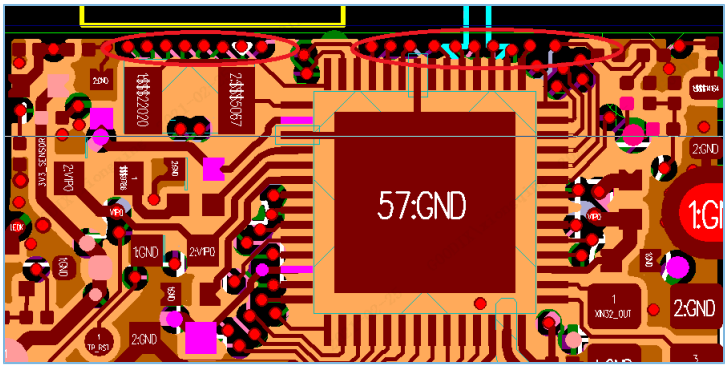



Figure 3-22 Improper I/O routing at board edge (not shielded by GND traces)

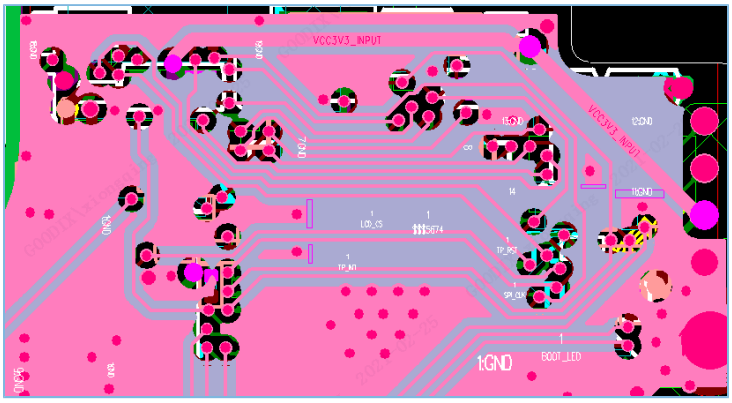



Figure 3-23 Proper routing of I/O pins

5. The capacitors or ESD protection devices should be routed through the pad. Avoid using long wires to connect the capacitors/ESD protection devices to pad, which undermines filtering/protection performance.

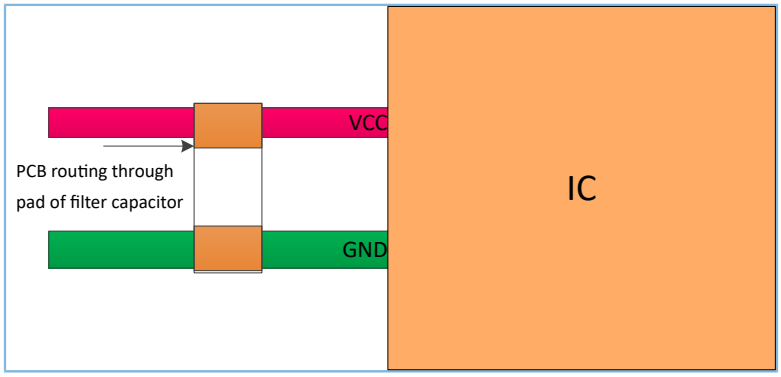



Figure 3-24 Proper routing for a capacitor (as an example)

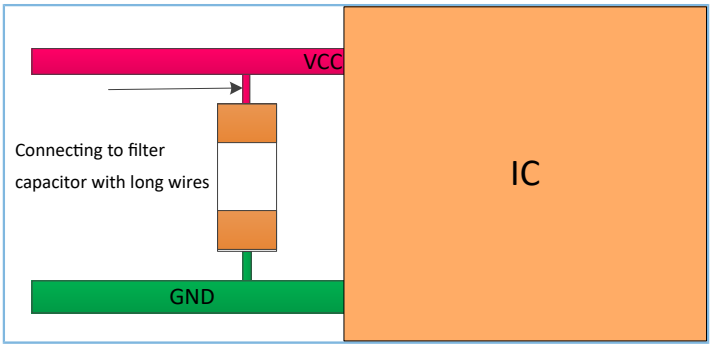



Figure 3-25 Improper routing for a capacitor (as an example)

#### 3.3.1.3 Product Structural Design

- Make sure the shell gaps are sealed to prevent static electricity from setting in.
- Connect ferrite beads in series to the GND pins on the metal shell, and connect the GND pins to the GND circuit on the motherboard, to protect the motherboard from static electricity transmitted through the metal shell.
- Suspended metal structure is not allowed. The steel stiffener of sensors (such as touch/display sensors) should be grounded.
- Try to avoid close contact with the overlapped area between the FPC on the motherboard and the FPC on touch/display sensor module. It is recommended to apply heat resistant adhesives on the exposed area of motherboard connectors, to prevent short circuit or static electricity from setting in.

### 3.3.2 ESD Considerations in Production, Transport, and Debugging

To steer away from ESD events, stringent ESD control is also required during production, transport, debugging, and other relevant phases.

- Wear antistatic wrist strap in these processes. Touching the SoC with bare hands or using metal tweezers is forbidden.
- Use an antistatic bag/tray to hold the SoC.
- Countermeasures against ESD are essential for soldering irons, welding tables, and test instruments.
- Strictly comply with ESD preventive requirements for the production line during production and transport.

# 4 Reference Design

## 4.1 Reference Schematic Diagram

Figure 4-1 is the reference schematic for GR5525RGNI QFN68 package.

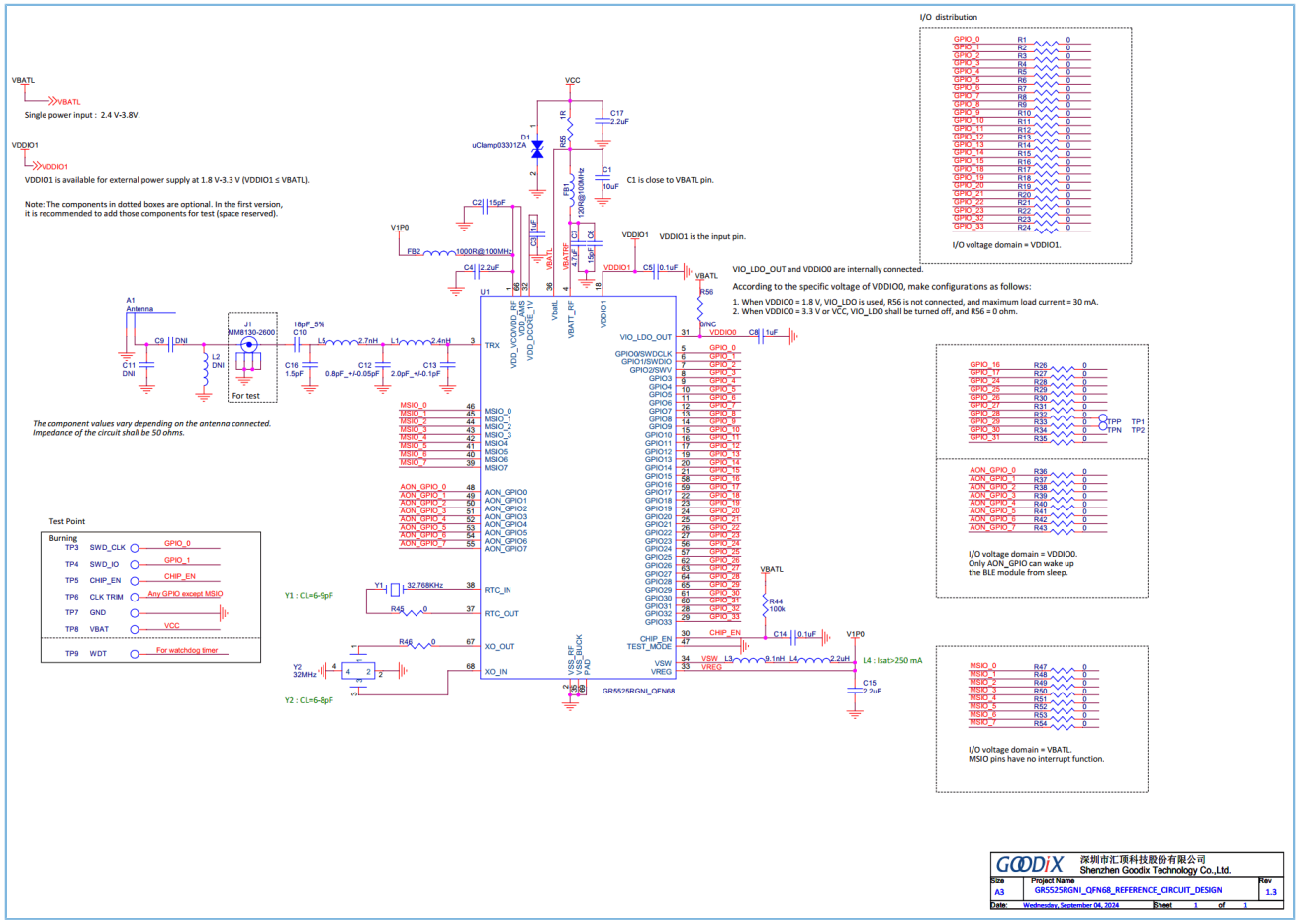



Figure 4-1 Reference schematic for GR5525RGNI QFN68 package

Figure 4-2 is the reference schematic for GR5525IENI QFN56 package.

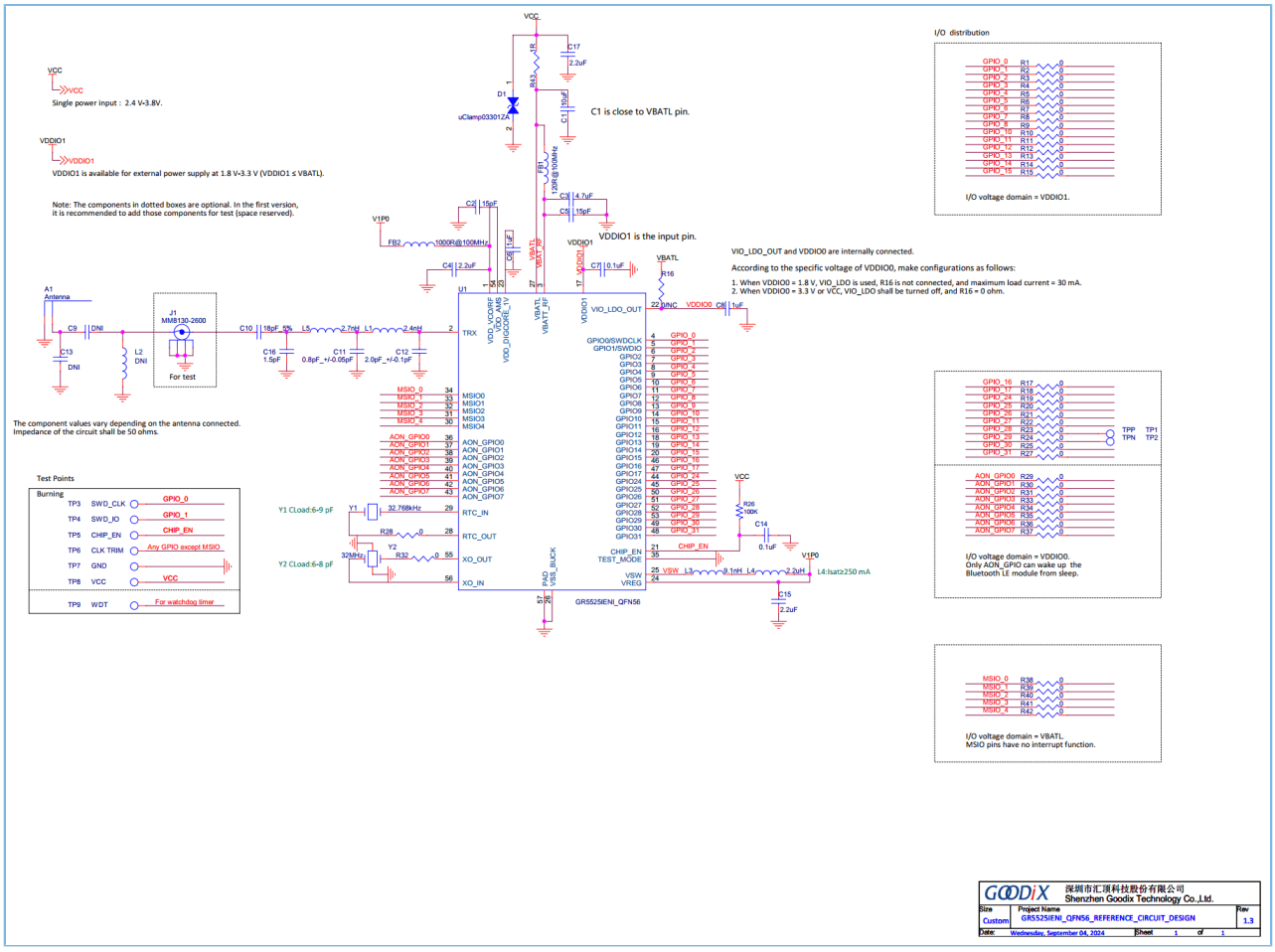



Figure 4-2 Reference schematic for GR5525IENI QFN56 package

Figure 4-3 is the reference schematic for GR5525I0NI QFN56 package.

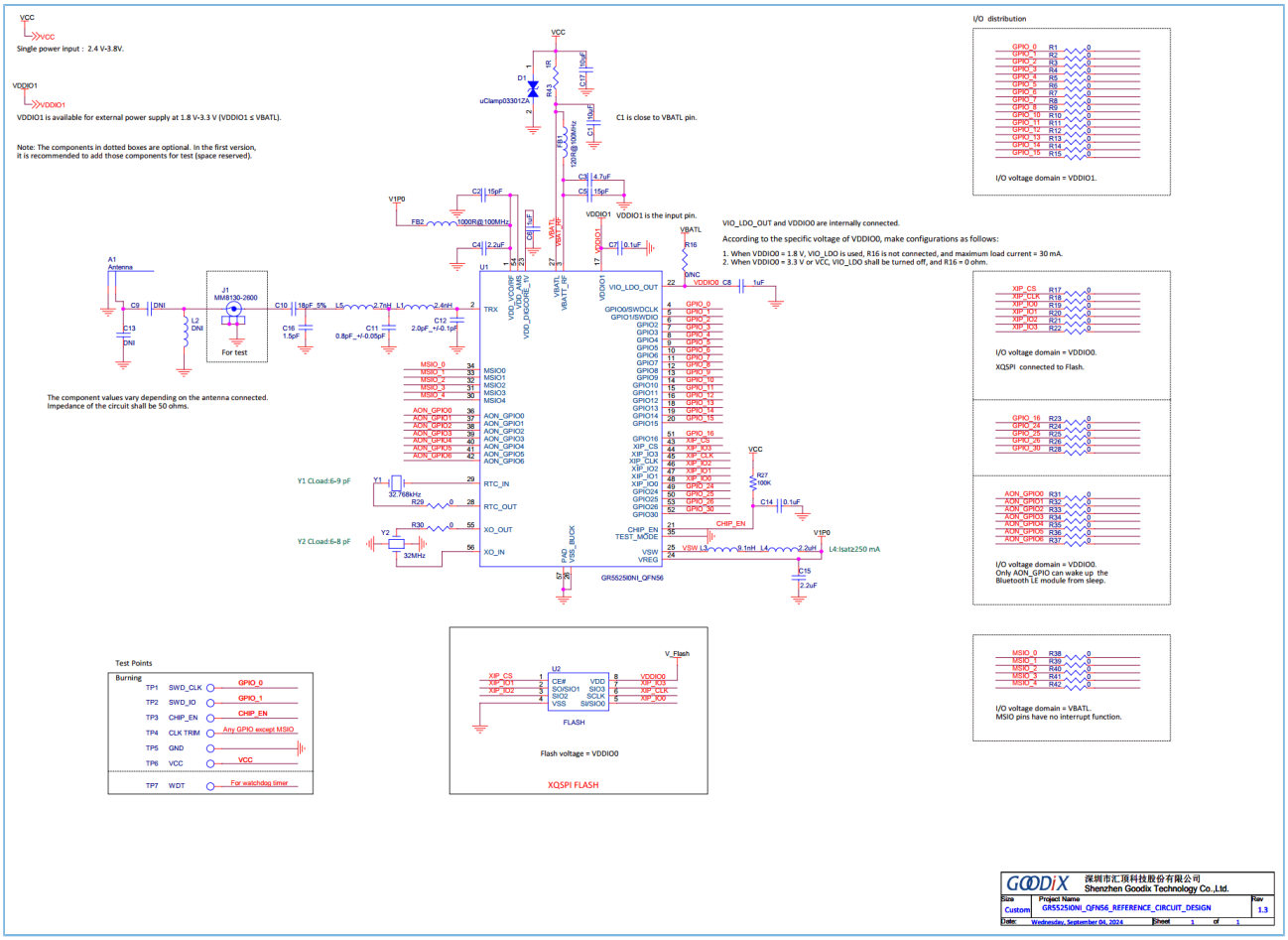


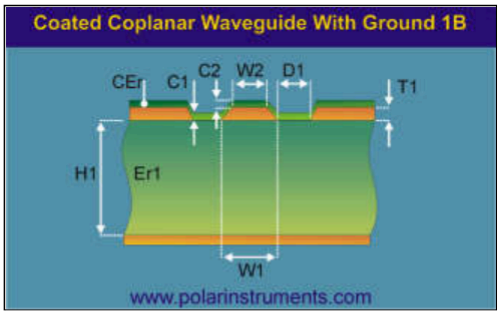

Figure 4-3 Reference schematic for GR5525I0NI QFN56 package

## 4.2 PCB Layout Reference Design

In accordance with rules specified in “Section 3.2 PCB Design and Layout Guideline”, this section provides two reference designs for PCB layout for the GR5525 minimal system by taking SoCs mounting QFN56 package as examples, to help users quickly get started with product development and design.

### 4.2.1 Four-layer PCBs

In this reference design, all GPIO signals are available as output. The 0.6 mm PCB is composed of four layers with plated through holes (PTHs). The RF route is 22 mil wide, which is the same with the component pad. To ensure the impedance of the RF route is not higher than 50 Ω, provide openings on the second layer, and use the third layer (PCB layer stackup: 0.6 mm, impedance: up to 50 Ω, as shown in Figure 4-4) as the reference plane.




| | | | | Tolerance | Minimum | Maximum |
|---|---|---|---|---|---|---|
| Substrate 1 Height | H1 | 14.6000 | +/- | 0.0000 | 14.6000 | 14.6000 |
| Substrate 1 Dielectric | Er1 | 4.2000 | +/- | 0.0000 | 4.2000 | 4.2000 |
| Lower Trace Width | W1 | 22.0000 | +/- | 0.0000 | 22.0000 | 22.0000 |
| Upper Trace Width | W2 | 21.0000 | +/- | 0.0000 | 21.0000 | 21.0000 |
| Ground Strip Separation | D1 | 11.0000 | +/- | 0.0000 | 11.0000 | 11.0000 |
| Trace Thickness | T1 | 1.2000 | +/- | 0.0000 | 1.2000 | 1.2000 |
| Coating Above Substrate | C1 | 1.0000 | +/- | 0.0000 | 1.0000 | 1.0000 |
| Coating Above Trace | C2 | 1.0000 | +/- | 0.0000 | 1.0000 | 1.0000 |
| Coating Dielectric | CEr | 4.2000 | +/- | 0.0000 | 4.2000 | 4.2000 |
| Impedance | Zo | 50.33 | | ------ | 50.33 | 50.33 |
| Delay (ps/in) | D | 148.357 | | ------ | 148.357 | 148.357 |
| Inductance (nH/in) | L | 7.466 | | ------ | 7.466 | 7.466 |
| Capacitance (pF/in) | C | 2.948 | | ------ | 2.948 | 2.948 |

Figure 4-4 Impedance control details for the 4-layer PCB (QFN56)

Details for the PCB layout reference design are provided below.

1. Top layer

   This layer is used for component layout and routing of key signals such as RF.

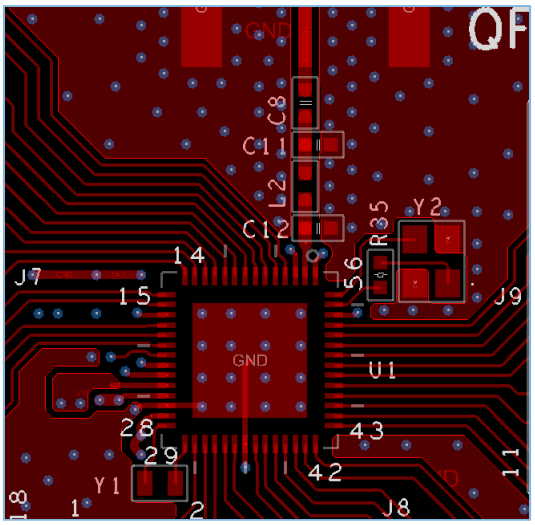



Figure 4-5 Top layer design for 4-layer PCB (QFN56)

2. Layer 2

This is the ground layer for returned signals. In the reference design, an opening is provided on Layer 2 underneath the 50 Ω RF transmission line, and another two openings are provided underneath the signal output pads of the 32 MHz crystal to reduce parasitic capacitance. Layer 3 acts as the reference ground where openings are provided on Layer 2.

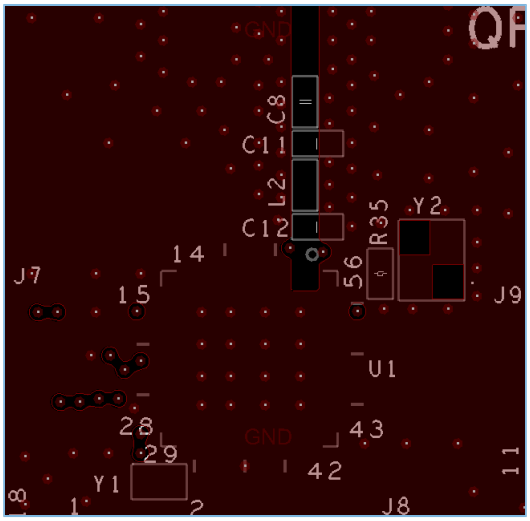



Figure 4-6 Layer 2 design for 4-layer PCB (QFN56)

3. Layer 3

This layer is used for the power and a small number of routes. In the reference design, Layer 3 is used as the reference ground layer for the RF transmission line, and therefore the part underneath the RF transmission line shall be complete.

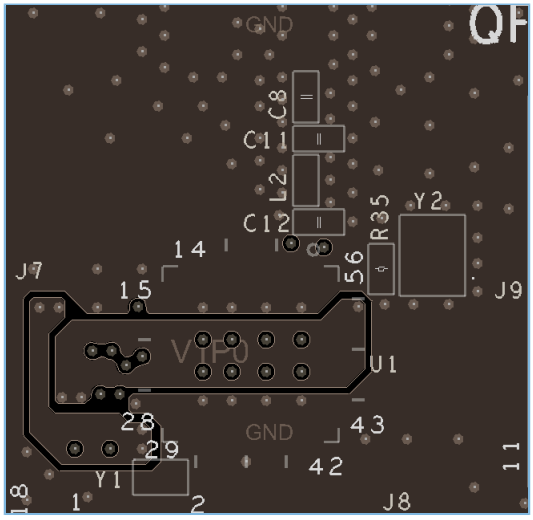



Figure 4-7 Layer 3 design for 4-layer PCB (QFN56)

4. Bottom layer

This layer is used for filter components layout and signal routing. Filter components should be as close to the corresponding IC pins as possible.

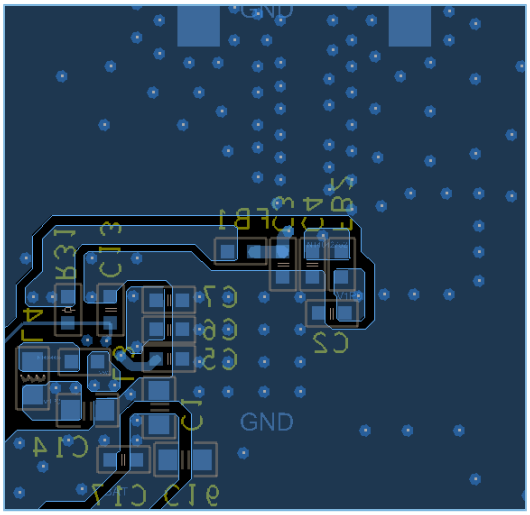



Figure 4-8 Bottom layer design for 4-layer PCB (QFN56)

### 4.2.2 Two-layer PCBs

To reduce costs, users can design two-layer PCBs. In such case, due to the absence of a ground layer between the two layers, special attention should be paid to the two-layer PCB layout, especially for applications requiring high performance in ESD protection and radiation compliance. Strictly follow the PCB design rules in "Section 3.2 PCB Design and Layout Guideline". Most importantly, make sure power filter capacitors are placed close to power pins, and connection to the GND return path should be enhanced.

Details for the PCB layout reference design are provided below.

1. Try to place components and routing on the top layer only (as shown in Figure 4-9, the top layer is used for component layout and routing of key signals such as RF), so that the bottom layer can be as complete as possible.

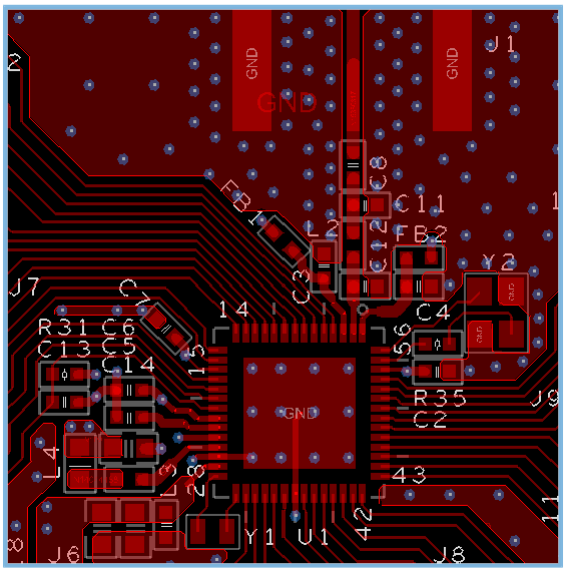



Figure 4-9 Top layer design for 2-layer PCB

2. The figure below is a reference design for power and GND routing. The GND vias circled in yellow are used for return paths of power and RF signals, and shall be connected to the heat dissipation pad with short, wide traces through copper pour areas on the bottom layer (indicated by the green arrows in Figure 4-10).

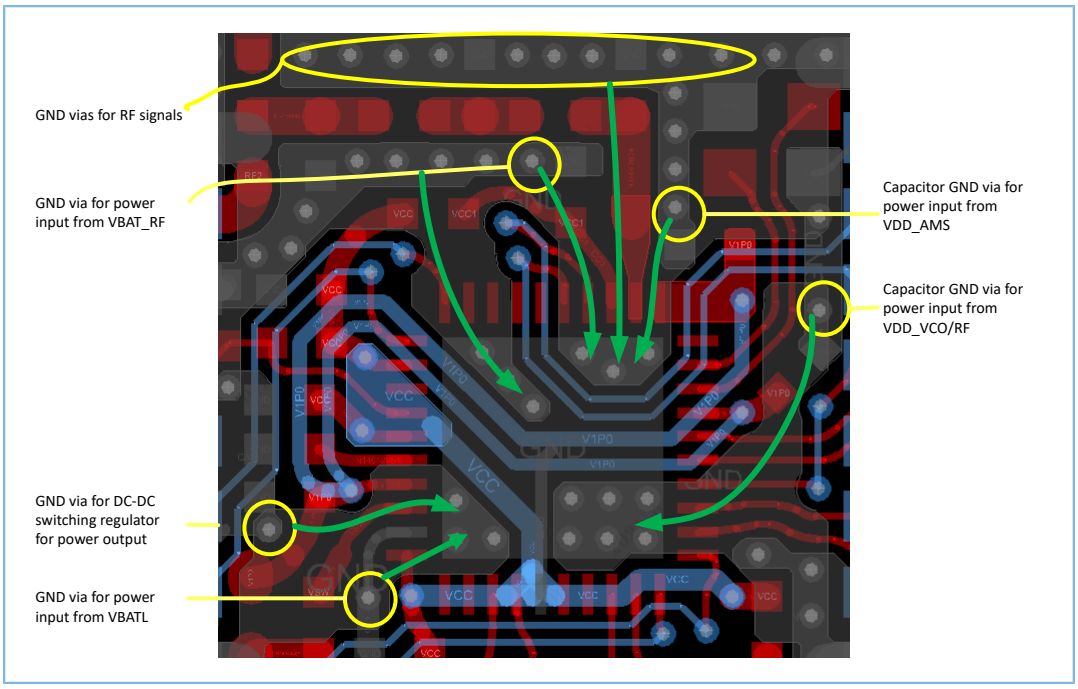



Figure 4-10 Power and GND routing reference design for 2-layer PCB

### 4.2.3 External Flash Connection for GR5525I0NI

GR5525I0NI uses external QSPI Flash with clock frequency up to 64 MHz. To avoid crosstalk from other signals, the Flash should be placed as close to the IC as possible to minimize the QSPI traces. QSPI traces should be in equal length, with the tolerance within 50 mil.

Figure 4-11 is a reference design for the PCB layout of GR5525I0NI.

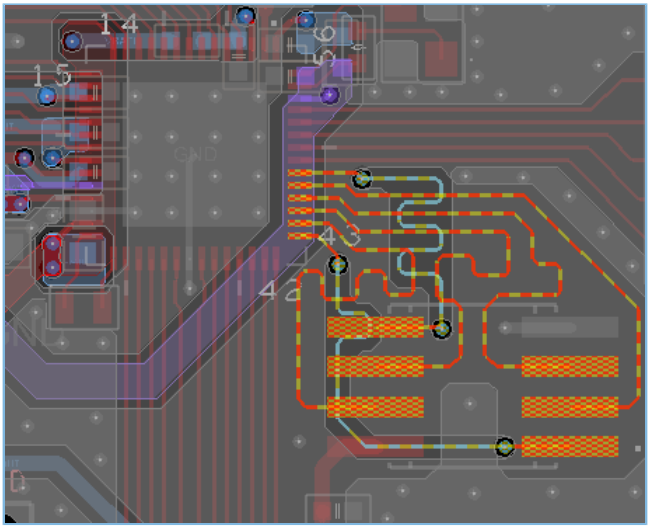


Figure 4-11 Reference design for GR5525I0NI PCB layout

# 5 FAQ

## 5.1 Why Is the Power Consumption in GR5525 Sleep Modes High?

- Description

  In power consumption tests, the power consumption of GR5525 when in sleep mode varies depending on different I/O pin configurations. How to properly configure I/O pins before GR5525 goes to sleep?

- Issue Analysis

  The power consumption of GR5525 in sleep mode is high, and it may be because I/O pins are not properly configured.

  - I/O pins are at floating state.
  - I/O pins are configured in improper pull-up or pull-down state.

  Above incorrect configurations can cause system leakage, so you need to properly configure the state of I/Os before GR5525 enters sleep mode.

- Solution

  Configure the state of I/O pins before GR5525 enters sleep mode.

  - If an I/O pin is in pull-up/pull-down state or used as a driver output, it needs no pull-up/pull-down configuration.
  - If an I/O pin is not used or works in input mode without pull-up or pull-down, it needs to be configured to internal pull-down.

## 5.2 Can the RF Matching Circuits Be Simplified or Removed?

- Description

  In designing a PCB, can I modify the recommended RF matching circuit layout due to limited space?

- Issue Analysis

  GR5525 recommends two matching circuits for RF: a matching circuit close to GR5525 and a matching circuit close to the antenna. Whether these two matching circuits can be simplified or removed needs to be treated differently.

- Solution

  The matching circuit close to GR5525 is used to match GR5525 internal PA and cannot be removed. It cannot be simplified also as its inductance and capacitance values must be kept consistent with the recommended circuit. The impedance of the RF channel from the GR5525 matching network is 50 Ω and compatible with any 2.4 GHz antenna (2400 MHz to 2484 MHz) that supports Bluetooth products.

  The matching circuit close to the antenna end is used to match the antenna, and its circuit can be changed according to the antenna you use. For the matching of the antenna, you can complete simple matching adjustment by the S11 parameter or the Smith chart from the vector network analyzer. However, for matching of

other indicators (such as antenna gain and directionality), you are recommended to seek help from professional antenna factories.

# 6 Glossary

Table 6-1 Glossary

| Name | Description |
|---|---|
| ADC | Analog to Digital Converter |
| AGC | Automatic Gain Control |
| AMS | Analog Mix Signal |
| BB | Baseband |
| Bluetooth LE | Bluetooth Low Energy |
| BUCK | Type of DC-DC Converter |
| DC-DC | DC-to-DC Converter |
| ESD | Electrostatic Discharge |
| ESR | Equivalent Series Resistance |
| Tg | Glass Transition Temperature |
| GPIO | General-Purpose Input/Output |
| LDO | Low-dropout |
| LNA | Low Noise Amplifier |
| PLL | Phase-Locked Loop |
| PMU | Power Management Unit |
| PCB | Printed Circuit Board |
| PTH | Plated Through Hole |
| QFN | Quad Flat No-Lead Package |
| QSPI | Queued Serial Peripheral Interface |
| RoHS | Restriction of Hazardous Substances Directive |
| SDK | Software Development Kit |
| SoC | System-on-Chip |
| SPI | Serial Peripheral Interface |
| SVHC | Substance of Very High Concern |
| SWD | Serial Wire Debug |
| UART | Universal Asynchronous Receiver/Transmitter |

# 7 Appendix: QFN Assembly Guideline

The GR5525 SoCs in QFN56 and QFN68 packages are qualified to MSL3 and are RoHS/green compliant. RoHS is the abbreviation of *Restriction of Hazardous Substances Directive*, which puts a limit on the amount of harmful substances in electronic devices, published by European Union in February 2003. MSL3 represents Moisture Sensitivity Level 3 which indicates that a moisture sensitive plastic device, once removed from a dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH before the solder reflow process.

GR5525 storage conditions:

- Temperature: < 40°C
- Humidity: < 90% RH
- Period: 12 months

After opening the package: go through reflow for board assembly within 48 hours.

- Temperature: < 30°C
- Humidity: < 60% RH
- Stored at: < 10% RH

Both lead-free solder and Sn/Pb solder applications use the same rules for the general PCB design. Only the board surface finish and the board material have to be considered for lead-free application due to the higher reflow temperature and lead-free solder compatibility. A number of factors may have a significant effect on mounting QFN package on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in exposed ground/thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow temperature profile.

---

**Note**:

It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort may be needed to optimize the process as per users' surface mount practices and requirements.

---

In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

Typically, the PCB pad pattern for an existing package is designed based on guidelines developed within a company or by following industry standards such as IPC-SM-782. For the purpose of this document, methodology of Association Connecting Electronics Industries (IPC) is used here for designing PCB pad pattern. However, because of exposed die paddle and the package lands on the bottom side of the package of GR5525, certain constraints are added to IPC's methodology. The pad pattern developed here includes considerations for lead and package tolerances.

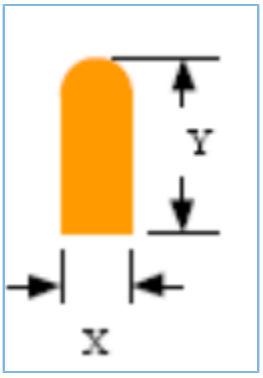



Figure 7-1 Land on the bottom side of the package

For the PCB pad design for GR5525 QFN56 package (7 mm x 7 mm, 0.4 mm pitch), it is recommended to set X = 0.25 mm and Y = 0.75 mm. The pads may also be rounded on the inner edge. Maximum pad width is set to 0.25 mm to avoid solder bridging.

It is recommended to use non-solder-mask defined (NSMD) pads. For 0.4 mm pitch parts with PCB pad width of 0.25 mm, not enough space is available for solder mask web in between the pads in GR5525 QFN56 package. In such cases, it is recommended to use “Trench” type solder mask opening where a big opening is designed around all pads on each side of the package with no solder mask in between the pads, as shown in Figure 7-2.

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**Note**:

The inner edge of the solder mask should be rounded, especially for corner leads to allow for enough solder mask web in the corner area.

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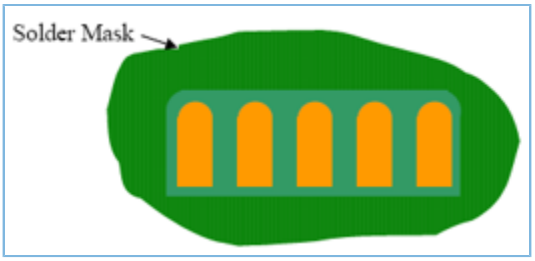


Figure 7-2 Solder mask definition for perimeter lands for 0.4 mm pitch parts

## 7.1 Package Information

This section provides comprehensive details on mechanical packaging information.

### 7.1.1 QFN68

The following table illustrates the dimensions of a device in QFN68 package, which is qualified to MSL3.

Table 7-1 QFN68 package information

| Parameter | Value | Unit | Tolerance |
|---|---|---|---|
| Package Size | 7.0 x 7.0 | mm | ±0.05 mm |

| Parameter | Value | Unit | Tolerance |
|---|---|---|---|
| QFN Pad Count | 68 | | |
| Total Thickness | 0.85 | mm | ±0.05 mm |
| QFN Pad Pitch | 0.35 | | |
| Pad Width | 0.15 | | ±0.05 mm |
| Exposed Pad Size | 5.49 x 5.49 | | ±0.1 mm |

The figure below shows the QFN68 package outlines.

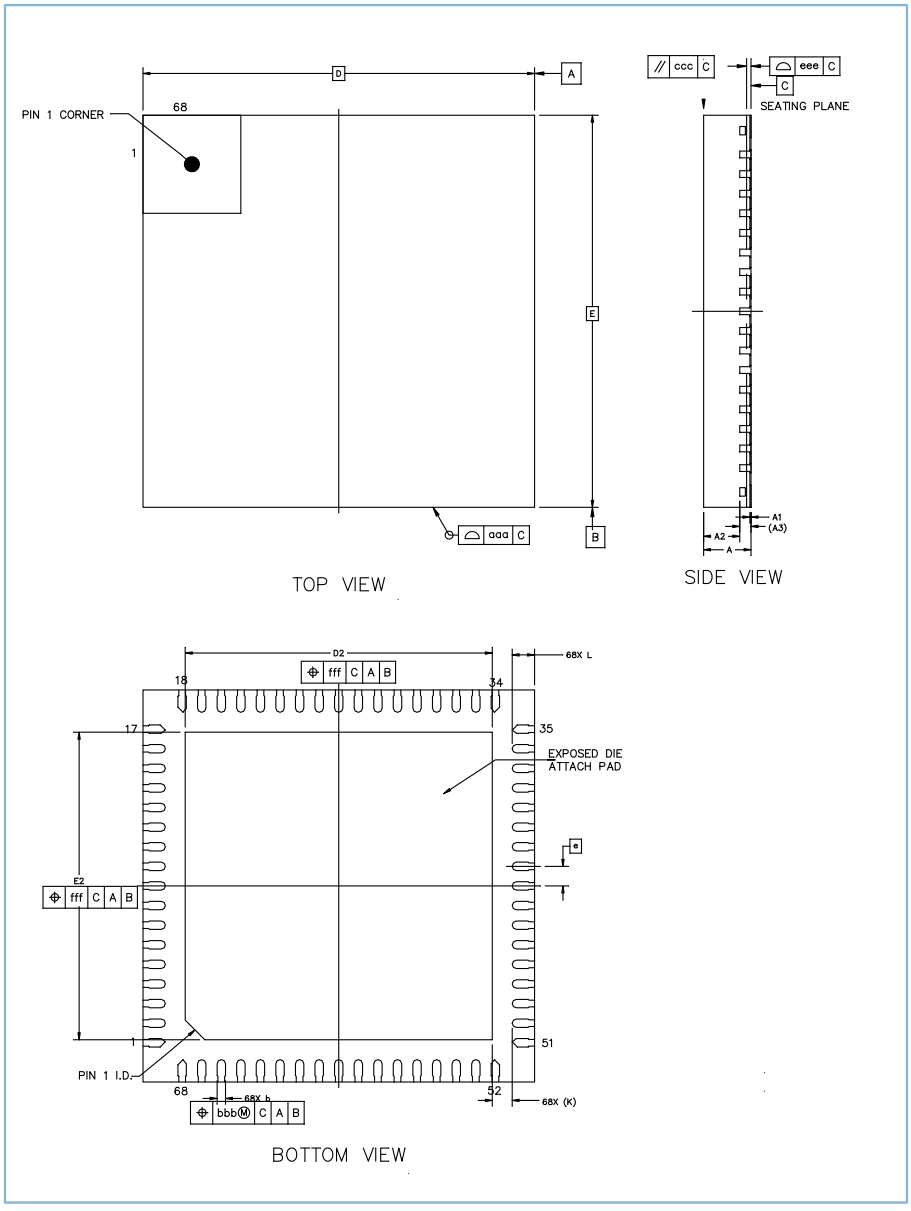


Figure 7-3 QFN68 package outlines

**Note**:

Drawing is not to scale.

Table 7-2 QFN68 package dimensions

| Symbol | Dimensions in mm | | | Dimensions in inch | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.800 | 0.850 | 0.900 | 0.031 | 0.033 | 0.035 |
| A1 | 0.000 | 0.020 | 0.050 | 0.000 | 0.001 | 0.002 |
| A2 | - | 0.650 | - | - | 0.026 | - |
| A3 | 0.203 REF. | | | 0.008 REF. | | |
| b | 0.100 | 0.150 | 0.200 | 0.004 | 0.006 | 0.008 |
| D | 7.000 BSC. | | | 0.276 BSC. | | |
| E | 7.000 BSC. | | | 0.276 BSC. | | |
| e | 0.350 BSC. | | | 0.014 BSC. | | |
| D2 | 5.390 | 5.490 | 5.590 | 0.212 | 0.216 | 0.220 |
| E2 | 5.390 | 5.490 | 5.590 | 0.212 | 0.216 | 0.220 |
| L | 0.350 | 0.400 | 0.450 | 0.014 | 0.016 | 0.018 |
| K | 0.355 REF. | | | 0.014 REF. | | |
| aaa | 0.100 | | | 0.004 | | |
| ccc | 0.100 | | | 0.004 | | |
| eee | 0.080 | | | 0.003 | | |
| bbb | 0.070 | | | 0.003 | | |
| fff | 0.100 | | | 0.004 | | |

**Note**:

Values in inches are converted from values in millimeter and rounded to three decimal digits.

## 7.1.2 QFN56

The following table illustrates the dimensions of a device in QFN56 package, which is qualified to MSL3.

Table 7-3 QFN56 package information

| Parameter | Value | Unit | Tolerance |
|---|---|---|---|
| Package Size | 7.0 x 7.0 | mm | ±0.1 mm |
| QFN Pad Count | 56 | | |
| Total Thickness | 0.75 | mm | ±0.05 mm |
| QFN Pad Pitch | 0.40 | | |

| Parameter | Value | Unit | Tolerance |
|---|---|---|---|
| Pad Width | 0.20 | | ±0.05 mm |
| Exposed Pad Size | 5.2 x 5.2 | | ±0.1 mm |

The figure below shows the QFN56 package outlines.

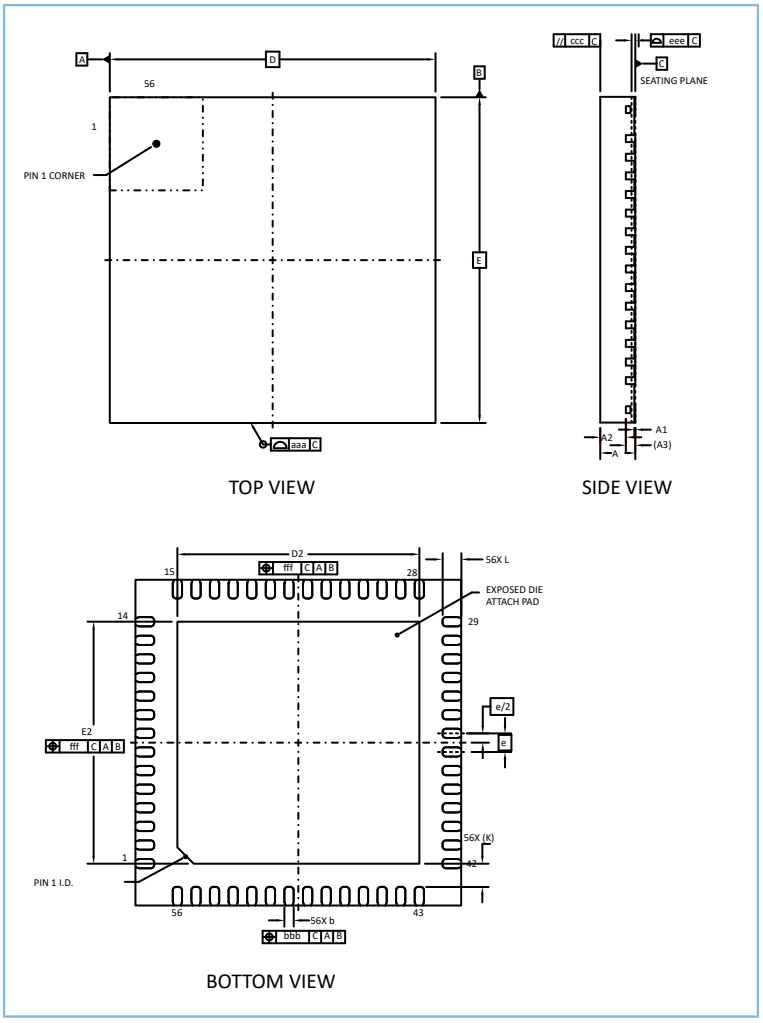


Figure 7-4 QFN56 package outlines

**Note**:

Drawing is not to scale.

Table 7-4 QFN56 package dimensions

| Symbol | Dimensions in mm | | | Dimensions in inch | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.700 | 0.750 | 0.800 | 0.028 | 0.030 | 0.032 |
| A1 | 0.000 | 0.020 | 0.050 | 0.000 | 0.001 | 0.002 |

| Symbol | Dimensions in mm | | | Dimensions in inch | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A2 | - | 0.550 | - | - | 0.022 | - |
| A3 | 0.203 REF. | | | 0.008 REF. | | |
| b | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| D | 7.000 BSC. | | | 0.276 BSC. | | |
| E | 7.000 BSC. | | | 0.276 BSC. | | |
| e | 0.400 BSC. | | | 0.016 BSC. | | |
| D2 | 5.100 | 5.200 | 5.300 | 0.201 | 0.205 | 0.209 |
| E2 | 5.100 | 5.200 | 5.300 | 0.201 | 0.205 | 0.209 |
| L | 0.300 | 0.400 | 0.500 | 0.012 | 0.016 | 0.020 |
| K | 0.500 REF. | | | 0.020 REF. | | |
| aaa | 0.100 | | | 0.004 | | |
| ccc | 0.100 | | | 0.004 | | |
| eee | 0.080 | | | 0.003 | | |
| bbb | 0.070 | | | 0.003 | | |
| fff | 0.100 | | | 0.004 | | |

**Note**:

Values in inches are converted from values in millimeter and rounded to three decimal digits.

## 7.2 Board Mounting Guideline

Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for QFN package. This is further complicated by the large grounding die pad underneath QFN packages and the proximity to the inner edges of the leads.

Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Because surface mount process varies from company to company, careful process development is recommended.

### 7.2.1 Stencil Design for Perimeter Pads

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 mils to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement.

The first step in achieving reliable solder joints is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

- Area ratio = area of aperture opening/aperture wall area

- Aspect ratio = aperture width/stencil thickness

For rectangular aperture openings, as required for GR5525 packages, these ratios are given as:

- Area ratio = LW/2T (L + W)
- Aspect ratio = W/T

L and W are the aperture length and width, and T is stencil thickness. For optimum paste release, the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release.

It is also recommended that the stencil aperture tolerances should be tightly controlled, as these tolerances can effectively reduce the aperture size. It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the center exposed pad region. See Figure 7-5 for reference solder mask design in the center of the package.

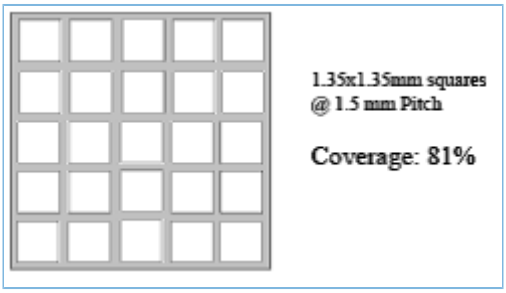


Figure 7-5 Exposed/Ground pad stencil design recommendation for QFN packages

## 7.2.2 Via Types and Solder Voiding

Voids within solder joints under the exposed grounding pad can have an adverse effect on high-speed and RF applications. Voids within this ground plane can increase the current path of the circuit.

The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any one via would not be rendered ineffectual based on any one void increasing the current path beyond the distance to the next available via.

### 7.2.2.1 Stencil Thickness and Solder Paste

The stencil thickness of 0.125 mm is recommended for 0.4 mm pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 paste (IPC standard J-STD-005) be used for mounting QFN packages. Nitrogen purge is also recommended during reflow.

The most common surface finishes that are compatible with lead-free surface mount technology (SMT) process are:

- Organic solderability preservatives (OSP)
- Electroless nickel/Immersion gold (ENIG)

 

- Immersion silver
- Immersion gold

Selection of a suitable finish will depend on end users' requirements for board design, assembly process, handling/ storage, and cost.

#### 7.2.2.2 PCB Materials

Due to the higher reflow temperature requirement of the lead-free material set, the board material with higher glass transition temperature Tg (> 170°C) is recommended.

### 7.2.3 SMT Printing Process

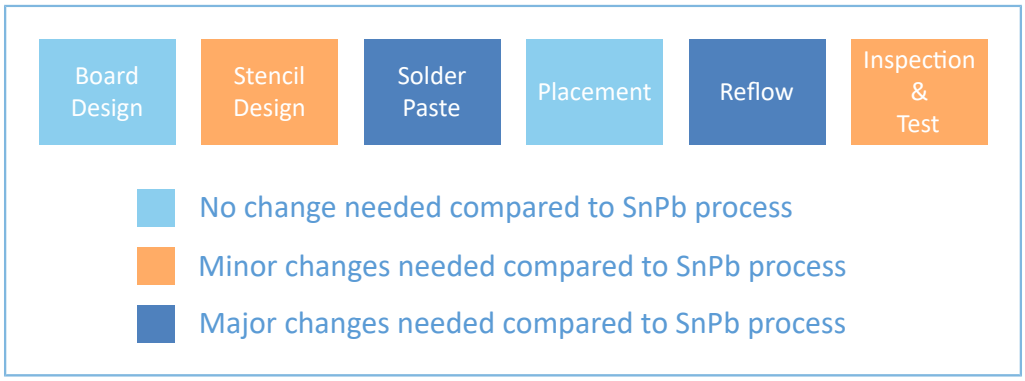


Figure 7-6 SMT printing process

- Solder Paste

  Sn-Ag-Cu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance.

- Stencil Design

  The recommended stencil is laser-cut, stainless-steel type with thickness of 5 to 7 mils and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 1 mil larger than the top can be utilized. Sn-Ag-Cu solder does not wet as well as Sn-Pb solder.

- Printing Process

  The printing process requires no significant changes, comparing with that applies Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste deposition.

- Placement

  With the self-aligning characteristic of the QFN packages during reflow, the placement accuracy is < 30% of the pad width or as long as the solder pads can touch solder paste.

## 7.3 SMT Reflow Process

The optimization of the reflow process is the most critical factor to be considered for the lead-free soldering. The development of an optimal profile should take into account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensure successful lead-free assembly, high yield and long-term solder joint reliability.

1. Temperature Profiling

   Temperature profiling should be performed for all new board designs by attaching thermocouples at the solder joints of QFN package, on the top surface of the larger components as well as at multiple locations of the boards. This is to ensure that all components are heated to temperature above the minimum reflow temperatures and the smaller components do not exceed maximum temperature limit.

   For larger or sophisticated boards with a large number of components, it is also important to minimize the temperature difference across the board to be less than 10 degree to minimize board warp. Maximum temperature at component body should not exceed the MSL3 qualification specification.

2. Reflow Profile Guideline

   The solder reflow profile should follow the recommendation from paste manufacturers and general standards such as JEDEC/IPC J-STD-20. Figure 7-7 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 7-5.

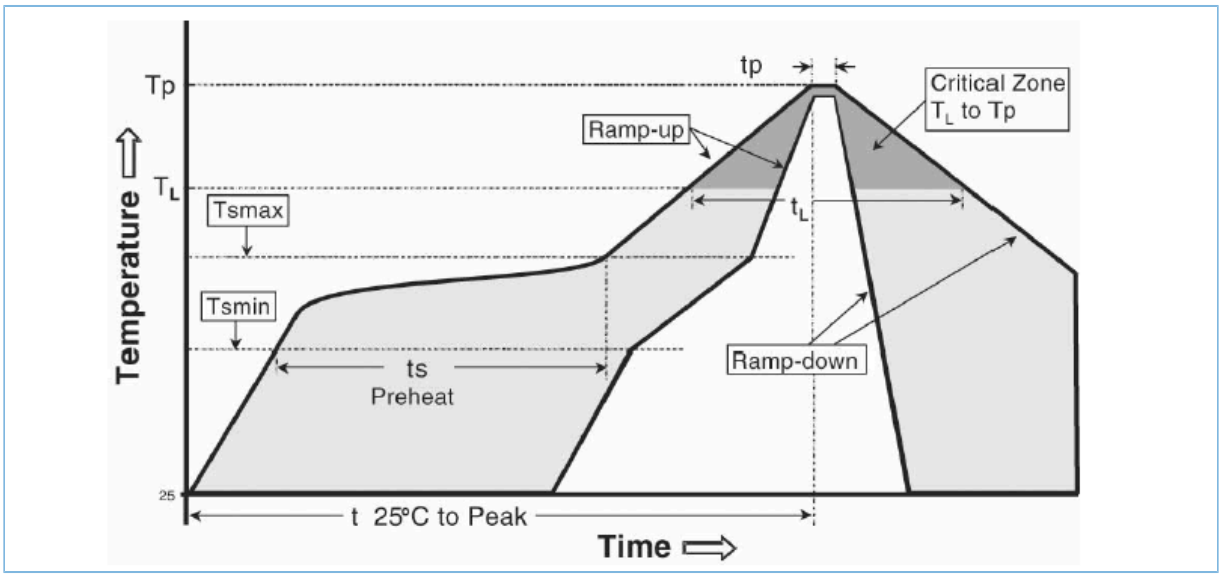


Figure 7-7 JEDEC recommended lead-free reflow profile

The GR5525 fulfills the lead-free soldering requirements from IPC/JEDEC, i.e. reflow soldering with a peak temperature up to 260°C.

The QFN40 lead frame is made of CμAg and has Matte Sn plating. This is 100% Sn and thus Pb-free. Plating thickness is 300 – 600 μin. The Matte Sn CμAg LF can withstand 3x reflow at 260°C.

Table 7-5 Reflow Profile Parameters

| Profile Parameters | Lead-Free Assembly, Convection, IR/Convection |
|---|---|
| Ramp-up rate (Tsmax to Tp) | 3°C/second (max) |
| Preheat temperature (Tsmin to Tsmax) | 150°C – 200°C |
| Preheat time (ts) | 60 seconds – 180 seconds |
| Time above $TB_L$, 217°C ($T_L$) | 60 seconds – 150 seconds |
| Time within 5°C of peak temperature (tp) | 20 seconds – 40 seconds |
| Ramp-down rate | 6°C/second (max) |
| Time 25°C to peak temperature | 8 minutes (max) |

**Note**:

All specified temperatures in Table 7-5 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 7-5 to prevent thermal damage to the package. An example of reflow profile is shown in Figure 7-8.

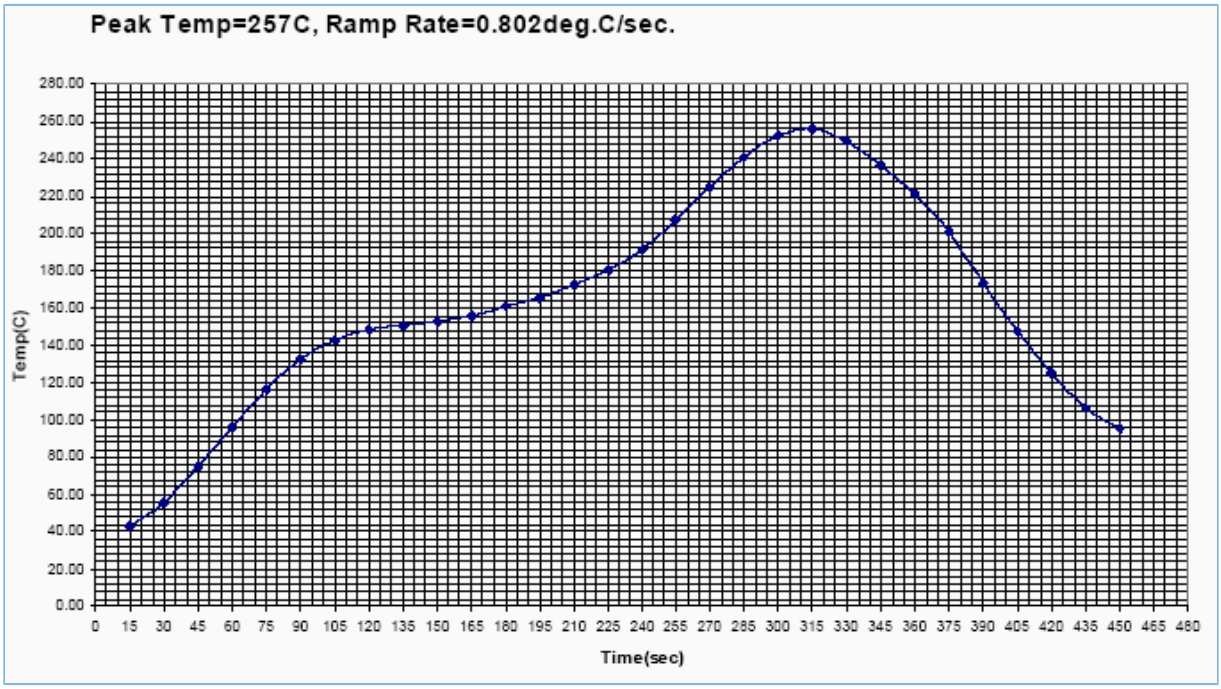


Figure 7-8 Reflow profile example with 257°C peak temperature

3. Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. An oven with more heating zones offers higher flexibility to optimize the reflow profile for complex and/or larger boards. Nitrogen atmosphere can improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

## 7.4 Rework Guideline

Because solder joints are not fully exposed for QFN package, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of QFN package can be a challenge due to their small size.

In most applications, QFN package will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Because reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for QFN packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste printing
4. Component placement
5. Component attachment

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**Note**:

Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

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### 7.4.1 Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally, the reflow profile for part removal should be the same as the one used for part attachment. However, the time above the liquidus state can be reduced as long as the reflow is complete.

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**Note**:

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and heated on the top side using hot gas or air.

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Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided because this may cause chip scale package (CSP) to skew. Air velocity of 15 – 20 liters per minute is a good starting point. Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cool down.

Because of the small size of GR5525 SoCs, the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad lift-off.

### 7.4.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and de-soldering braid. The width of the blade should match to the maximum width of

 

the footprint and the blade temperature should be low enough to prevent any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.

### 7.4.3 Solder Paste Printing

Because of their small size and finer pitches, solder paste deposition for QFN packages requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100x magnification.

The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side. A 125 microns thick stencil with aperture size and shape same as the package land should be used.

In addition, no-clean flux should be used, because small standoff of QFN packages does not leave much room for cleaning.

### 7.4.4 Component Placement

QFN packages are expected to have superior self-centering ability due to their small mass. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The alignment should also be done at 50 to 100x magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

### 7.4.5 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Because all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

## 7.5 RoHS Compliant

GR5525 is RoHS compliant, as per directive 2002/95/EC and its subsequent amendments.

## 7.6 SVHC Materials (REACH)

GR5525 is compliant with Substance of Very High Concern (SVHC) list based on the publication by European Chemicals Agency (ECHA) on October 28, 2008 Regulation (EC) No 1907/2006 concerning *Registration, Evaluation, Authorisation and Restriction of Chemicals (REACH)*.

## 7.7 Halogen Free

GR5525 is compliant with BS EN 14582: 2007 in regards to halogens: fluorine, chlorine, bromine, and iodine content.