GR5526 Datasheet Brief

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Contents

1 GR5526 Overview

The Goodix GR5526 family is a single-mode, low-power Bluetooth 5.3 System-on-Chip (SoC). It can be configured as a Broadcaster, an Observer, a Central, and a Peripheral and supports the combination of all the above roles, making it an ideal choice for Internet of Things (IoT) and smart wearable devices. In addition, it supports Bluetooth Low Energy (Bluetooth LE) direction finding: angle of arrival (AoA) and angle of departure (AoD), as well as LE Audio, made possible by LE Isochronous Channels.

Based on ARM® Cortex®-M4F CPU core, the GR5526 series integrates Bluetooth 5.3 Protocol Stack, a 2.4 GHz RF transceiver, on-chip programmable Flash memory, RAM, multiple peripherals, enhanced I2C/UART port number for sensor applications, as well as expanded I/O functionality. GR5526 delivers a feature-rich display and graphics solution by providing the choice of graphics acceleration (GPU + DC) and internal/external system-in-package (SiP) pseudostatic RAM (PSRAM) to accommodate display while still leaving plenty of space for wearable schemes.

GR5526 series comes in two package choices: BGA83 and QFN68 (as shown in the table below), that can meet diverse application scenarios.

Table 1-1 GR5526 series

Features	GR5526VGBIP	GR5526VGBI	GR5526RGNIP	GR5526RGNI
CPU	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F
RAM	512 KB	512 KB	512 KB	512 KB
SiP Flash	1 MB	1 MB	1 MB	1 MB
SiP PSRAM	8 MB	N/A	8 MB	N/A
GPU + DC	Supported	N/A	Supported	N/A
I/O number	50	50	48	48
Package (mm)	BGA83 (4.3 x 4.3 x 0.96)	BGA83 (4.3 x 4.3 x 0.96)	QFN68 (7.0 x 7.0 x 0.85)	QFN68 (7.0 x 7.0 x 0.85)

1.1 Features

- Bluetooth Low Energy 5.3 transceiver integrating Controller and Host layers
  - Supported data rates: 1 Mbps, 2 Mbps, and Long Range (500 kbps, 125 kbps)
  - TX power: -20 dBm to +7 dBm
  - -98 dBm sensitivity (in 1 Mbps mode)
  - -94 dBm sensitivity (in 2 Mbps mode)
  - -101 dBm sensitivity (in Long Range 500 kbps mode)
  - -104 dBm sensitivity (in Long Range 125 kbps mode)
  - TX current: 4.0 mA @ 0 dBm, 1 Mbps
  - RX current: 3.5 mA @ 1 Mbps
  - AoA/AoD, LE Isochronous Channels

- ARM® Cortex®-M4F 32-bit micro-processor with floating point support
  - Up to 96 MHz clock frequency
  - Built-in Memory Protection Unit (MPU) supporting eight programmable regions
  - Hardware Floating Point Unit (FPU)
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Non-maskable Interrupt (NMI) input
  - Serial Wire Debug (SWD) with 16 breakpoints, two watchpoints, and a debug timestamp counter
  - 51 µA/MHz execution from Flash @ 3.3 V, 96 MHz
- On-chip memory
  - 512 KB data SRAM with retention capabilities
  - 8 KB cache SRAM with retention capabilities
  - Stack ROM (including boot ROM and Bluetooth LE Stack)
  - 1 MB internal QSPI Flash
  - 8 MB internal PSRAM (for GR5526VGBIP and GR5526RGNIP only)
- Digital peripherals
  - Two general-purpose DMA engines, each with six channels and up to 16 handshaking interfaces
  - USB 2.0 full speed (12 Mbps) controller with on-chip PHY and dedicated DMA controller
  - Internal Octal SPI DDR interfaces to support 8 MB internal PSRAM at up to 48 MHz (for GR5526VGBIP and GR5526RGNIP only)
- Analog peripherals
  - One 13-bit Sense ADC with a sampling rate of 1 Msps. It supports up to 8 external I/O channels and 3 internal signal channels.
  - Built-in temperature and voltage sensors
  - Low-power comparator, supporting wakeup from deep sleep mode
- Flexible serial peripherals
  - 6 x UART modules up to 4 Mbps, with all modules supporting flow control and IrDA
  - 6 x I2C modules for peripheral communication, up to 3.4 MHz
  - 1 x 8-bit/16-bit/32-bit SPI master interface and 1 x SPI slave interface for host communication
  - 2 x I2S interfaces (1 I2S master interface and 1 I2S slave interface)
  - PDM interface with hardware sampling rate converter
  - 1 x ISO7816 interface

- Display/Graphics
  - 2.5D GPU for graphics acceleration (for GR5526VGBIP and GR5526RGNIP only)
  - 1 x Dual-lane SPI (DSPI) interface for display, with Mobile Industry Processor Interface (MIPI) Display Bus Interface (DBI) Type-C support
  - 3 x Quad SPI (QSPI) interfaces, up to 48 MHz; supporting direct access via memory mapping when connecting with external NOR Flash
  - Display Controller (DC) module with MIPI DBI Type-C support and 2D graphics blending integrated (for GR5526VGBIP and GR5526RGNIP only)
- Security
  - Complete secure computing engine:
    - AES 128-bit/192-bit/256-bit symmetric encryption (ECB, CBC)
    - Hash-based Message Authentication Code (HMAC-SHA256)
    - Public key cryptography (PKC)
    - True random number generator (TRNG)
  - Comprehensive security operation mechanism:
    - Secure boot
    - Encrypted firmware running directly from Flash
    - eFuse for encrypted key storage
    - Differentiate application data key and firmware key, supporting one data key per each device/product
- I/O Peripherals
  - 50 I/O pins in total
    - 34 general-purpose I/O (GPIO) pins
    - 8 always-on I/O (AON IO) pins, supporting wakeup from deep sleep mode
    - 8 mixed signal I/O (MSIO) pins, configurable to be digital/analog signal interface
- Timer
  - Two general-purpose, 32-bit timer modules
  - A timer module composed of two programmable 32-bit or 16-bit down counters
  - An internal sleep timer that can be used to wake the device up from deep sleep mode
  - Two PWM modules with edge alignment mode and center alignment mode, each with 3 channels
  - 2 x real-time counters (RTC): 1 x Calendar, 1 x RTC
- Power management

  - On-chip DC-DC to provide RF Analog voltage and supply core LDO
  - On-chip I/O LDO to provide I/O voltage and supply external components, maximum I/O LDO drive strength: 30 mA
  - Programmable thresholds for brownout detection (BOD)
  - Supply voltage: 2.4 V–4.35 V
  - I/O voltage: 1.8 V–3.6 V
- Low-power consumption modes
  - Sleep mode: 3.3 µA (Typical) at 3.3 V VBAT input with 128 KB SRAM retention on and LFXO_32K off; woken up by 8 sources of always-on domain
  - Ultra deep sleep mode: 2.4 µA (Typical); internal power (all SRAM included) and LFXO_32K removed from entire chip except always-on domain; woken up by Sleep Timer and AON GPIOs
  - OFF mode: 200 nA (Typical); nothing on except VBAT, and chip in reset mode
- Packages
  - BGA83: 4.3 x 4.3 x 0.96 (mm), 0.4 mm pitch
  - QFN68: 7.0 x 7.0 x 0.85 (mm), 0.35 mm pitch
- Operating temperature range: -40°C to +85°C

1.2 Block Diagram

The block diagram of GR5526 is shown in the figure below.

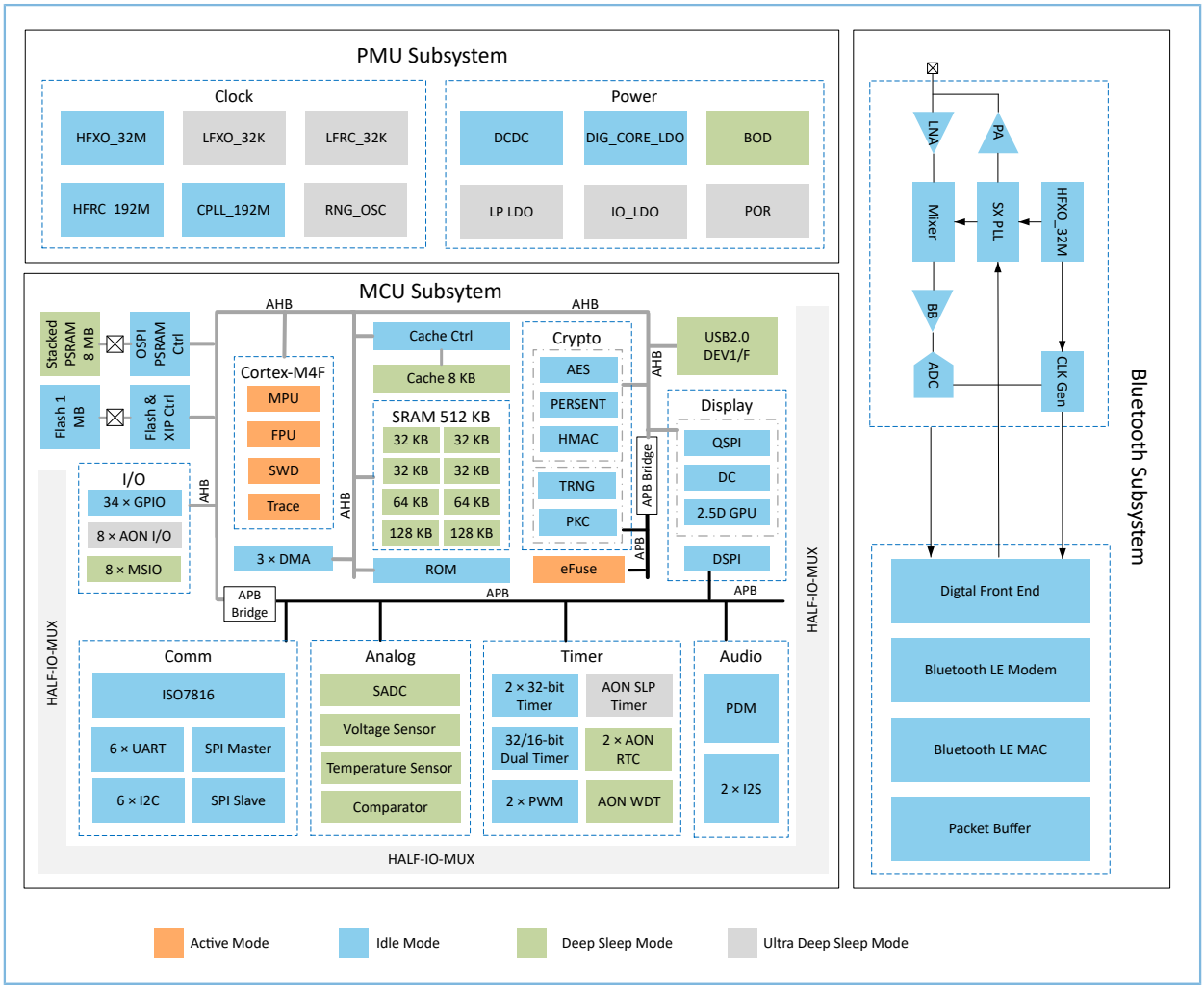

Figure 1-1 GR5526 block diagram

- Bluetooth subsystem
  - A 2.4 GHz transceiver and a digital communication core that supports Bluetooth 5.3
- MCU subsystem
  - An ARM® Cortex®-M4F with all the required memories and peripherals
  - Security cores that can be used for application security and secure boot implementation
  - GPU + DC to enhance processing capabilities
- Power management unit (PMU) subsystem
  - All the required power management modules to supply sufficient power for both internal modules and external peripherals
  - Modules required for ultra-low-power operation are in standby mode. HFRC_192M, RNG_OSC, LFRC_32K, wakeup GPIOs (Wake up), low-power comparator (LP Comp.), and power state controller (Power Sequencer) are used to control the state of different modules

1.3 Applications

The GR5526 SoC can be used in rich sets of applications. Example applications include:

- Advanced wearables
  - Sport bracelet
  - Smart watch
- Bluetooth HID devices
  - Voice remote control
  - Keyboard/Mouse
  - Gaming controller
  - Stylus pen
- IoT applications
  - Smart home
  - Electronic shelf label (ESL)
  - Beacon
  - Tire pressure monitoring system (TPMS)
  - Mesh applications
  - Asset tracking

2 Pinout

This chapter introduces GR5526 pinout available in BGA83 and QFN68 packages and provides detailed descriptions.

2.1 BGA83

The figure below shows the pins assignment (top view) of a GR5526 BGA83 package that is applicable to GR5526VGBIP and GR5526VGBI.

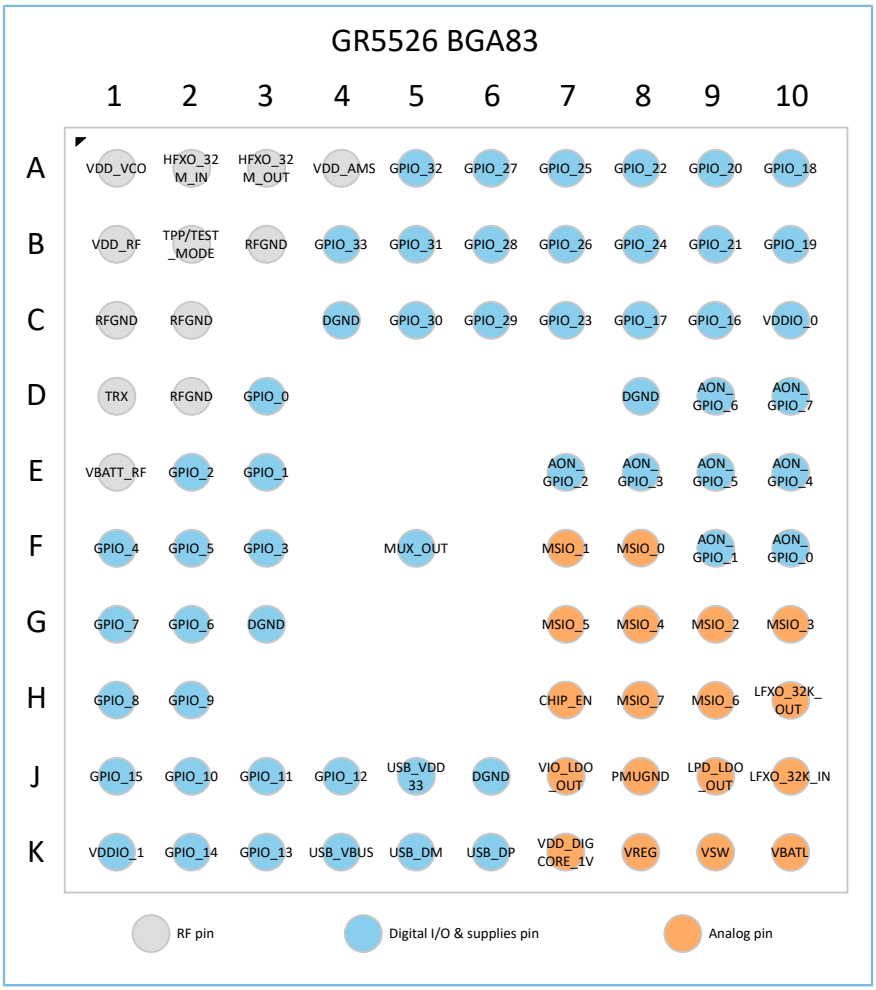

Figure 2-1 GR5526 BGA83 package pinout

The table below shows pin descriptions of a GR5526 BGA83 package.

Table 2-1 GR5526 BGA83 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A1	VDD_VCO	Analog/RF Supply	Synthesizer VCO supply; connect to VREG	
A2	HFXO_32M_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
A3	HFXO_32M_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
A4	VDD_AMS	Analog/RF Supply	AMS supply: 1.1 V; connect to VREG	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A5	GPIO_32	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A6	GPIO_27	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A7	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A8	GPIO_22	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A9	GPIO_20	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A10	GPIO_18	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B1	VDD_RF	Analog/RF supply	RF supply: 1.1 V; connect to VREG	
B2	TPP/TEST_MODE	Analog/RF	Input pin, used to set test mode for factory test. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	
B3	RFGND	RF	RF ground	
B4	GPIO_33	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B5	GPIO_31	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B6	GPIO_28	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B7	GPIO_26	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B8	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B9	GPIO_21	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B10	GPIO_19	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C1	RFGND	RF	RF ground	
C2	RFGND	RF	RF ground	
C4	DGND	Digital Ground	Digital ground	
C5	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C6	GPIO_29	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C7	GPIO_23	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C8	GPIO_17	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C9	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C10	VDDIO_0	Digital Supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO0
D1	TRX	Analog/RF	RX input and TX output	
D2	RF_GND	RF	RF ground	
D3	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 4 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
D8	DGND	Digital Ground	Digital ground	
D9	AON_GPIO_6	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
D10	AON_GPIO_7	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E1	VBATT_RF	Analog/RF Supply	Connected to VBATL	
E2	GPIO_2	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
E3	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 4 mA.	VDDIO1
E7	AON_GPIO_2	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E8	AON_GPIO_3	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E9	AON_GPIO_5	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E10	AON_GPIO_4	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
F1	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
F2	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
F3	GPIO_3	Digital I/O	General purpose I/O, configurable to be an SWO interface; pad drive level is 4 mA.	VDDIO1
F5	MUX_OUT	PMU	-	
F7	MSIO_1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
F8	MSIO_0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
F9	AON_GPIO_1	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
F10	AON_GPIO_0	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
G1	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
G2	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
G3	DGND	Digital Ground	Digital ground	
G7	MSIO_5	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G8	MSIO_4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G9	MSIO_2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G10	MSIO_3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H1	GPIO_8	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
H2	GPIO_9	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
H7	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin The high level of CHIP_EN equals VBATL.	
H8	MSIO_7	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H9	MSIO_6	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H10	LFXO_32K_OUT	PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
J1	GPIO_15	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J2	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J3	GPIO_11	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J4	GPIO_12	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J5	USB_VDD33	USB	Internal output voltage: USB 3.3 V	
J6	DGND	Digital Ground	Digital ground	
J7	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator	
J8	PMUGND	PMU	DC/DC converter supply and general battery GND	
J9	LPD_LDO_OUT	PMU	Output of low power domain LDO	
J10	LFXO_32K_IN	PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
K1	VDDIO_1	Digital Supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
K2	GPIO_14	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
K3	GPIO_13	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
K4	USB_VBUS	USB	Input voltage: USB 5 V	
K5	USB_DM	USB	USB D- Pin	
K6	USB_DP	USB	USB D+ Pin	
K7	VDD_DIGCORE_1V	PMU	On-chip LDO output for digital core	
K8	VREG	PMU	Feedback pin of switch regulator	
K9	VSW	PMU	DC/DC converter switching node	
K10	VBATL	PMU	Power supply: 2.4 V to 4.35 V	

2.2 QFN68

The figure below shows the pins assignment (top view) of a GR5526 QFN68 package that is applicable to GR5526RGNIP and GR5526RGNI.

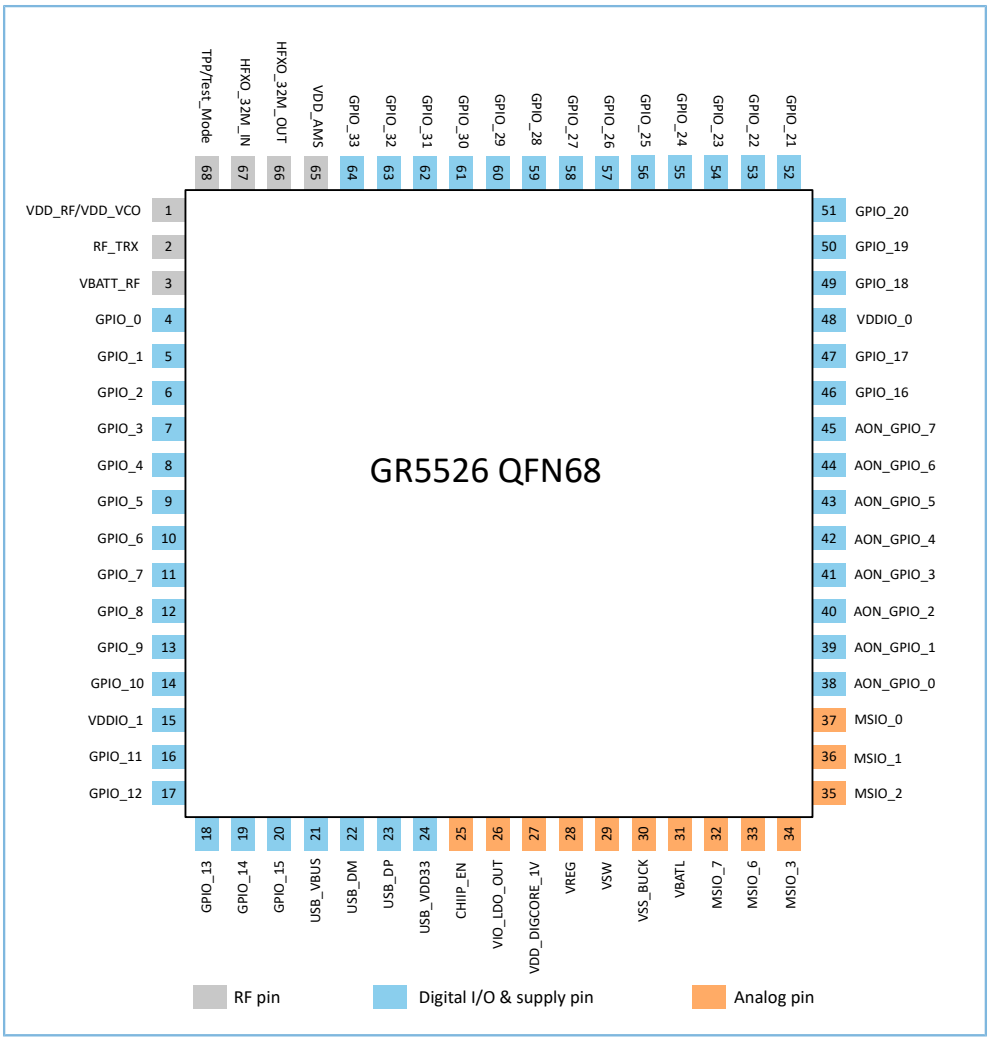

Figure 2-2 GR5526 QFN68 package pinout

The table below shows pin descriptions of a GR5526 QFN68 package.

Table 2-2 GR5526 QFN68 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG	
2	RF_TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF Supply	Connected to VBATL	
4	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 4 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
5	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 4 mA.	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O, configurable to be an SWO interface; pad drive level is 4 mA.	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
12	GPIO_8	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
13	GPIO_9	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
14	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
15	VDDIO_1	Digital I/O supply	Digital I/O supply input. Support external 1. 8 V–3.3 V input voltage.	VDDIO1
16	GPIO_11	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
17	GPIO_12	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
18	GPIO_13	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
19	GPIO_14	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
20	GPIO_15	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
21	USB_VBUS	USB	Input voltage: USB 5 V	
22	USB_DM	USB	USB D- pin	
23	USB_DP	USB	USB D+ pin	
24	USB_VDD33	USB	Internal output voltage: USB 3.3 V	
25	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL.	
26	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator	
27	VDD_DIGCORE_1V	Analog/PMU	On-chip LDO output for digital core	
28	VREG	Analog/PMU	Feedback pin of switch regulator	
29	VSW	Analog/PMU	DC/DC converter switching node	
30	VSS_BUCK	Analog/PMU	DC/DC converter supply and general battery GND	
31	VBATL	Analog/PMU	Power supply: 2.4 V to 4.35 V	
32	MSIO_7	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); multiplexed by LFXO_32K_IN; pad drive level is 2 mA.	VBATL

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
33	MSIO_6	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); multiplexed by LFXO_32K_OUT; pad drive level is 2 mA.	VBATL
34	MSIO_3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
35	MSIO_2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
36	MSIO_1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
37	MSIO_0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
38	AON_GPIO_0	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
39	AON_GPIO_1	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
40	AON_GPIO_2	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
41	AON_GPIO_3	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
42	AON_GPIO_4	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
43	AON_GPIO_5	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
44	AON_GPIO_6	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
45	AON_GPIO_7	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
46	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
47	GPIO_17	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
48	VDDIO_0	Digital I/O supply	Digital I/O supply input. Support external 1.8 V–3.3 V input voltage.	VDDIO0
49	GPIO_18	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
50	GPIO_19	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
51	GPIO_20	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
52	GPIO_21	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
53	GPIO_22	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
54	GPIO_23	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
55	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
56	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
57	GPIO_26	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
58	GPIO_27	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
59	GPIO_28	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
60	GPIO_29	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
61	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
62	GPIO_31	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
63	GPIO_32	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
64	GPIO_33	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
65	VDD_AMS	Analog/RF	AMS supply: 1.1 V. Connect to VREG.	
66	HFXO_32M_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
67	HFXO_32M_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
68	TPP/TEST_MODE	Analog/RF	Input pin, used to set test mode for factory test. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	

3 Pin Mux

3.1 Introduction

GR5526 series has a configurable pin multiplexing module (Pin Mux) which can bring different peripherals on different GPIOs.

3.2 Functional Description

The pin multiplexing choices for all pads are shown in:

- Table 3-1 and Table 3-2 (GPIO_0–GPIO_15)
- Table 3-3 and Table 3-4 (GPIO_16–GPIO_33)
- Table 3-5 (AON_GPIO_0–AON_GPIO_7)
- Table 3-6 (MSIO_0–MSIO_7)

There are eight mux choices (from MUX_0 to MUX_7) in the pin mux tables as follows.

Table 3-1 Pin multiplexing for GPIO_0–GPIO_7

IO Name	MUX_0	MUX_1	MUX_2	MUX_3	MUX_4	MUX_5	MUX_6	MUX_7
GPIO_0	SWD_CLK	I2C1_SCL	UART0_TX	UART1_CTS	PWM1_C	PWM0_C	PDM_CLKO	GPIO_A0
GPIO_1	SWD_IO	I2C1_SDA	UART0_RX	UART1_RTS	PWM1_B	PWM0_B	PDM_DI	GPIO_A1
GPIO_2	I2C0_SCL	PDM_CLKO	UART0_CTS	UART1_TX	PWM1_A	PWM0_A	iso_sync1_p	GPIO_A2
GPIO_3	I2C0_SDA	PDM_DI	UART0_RTS	UART1_RX	FERP_GPIO_Trig	SWV	iso_sync0_p	GPIO_A3
GPIO_4	I2C4_SCL	SPI_M_CLK	PWM0_A	UART3_TX	PDM_CLKO	df_ant_switch_sel_0	UART2_CTS	GPIO_A4
GPIO_5	I2C4_SDA	SPI_M_MOSI	PWM0_B	UART3_RX	PDM_DI	df_ant_switch_sel_1	UART2_RTS	GPIO_A5
GPIO_6	I2C3_SCL	SPI_M_MISO	PWM0_C	I2S_WS	iso_sync1_p	SPI_S_CLK	SIM_PRESENCE	GPIO_A6
GPIO_7	I2C3_SDA	SPI_M_CS0_N	PWM1_A	I2S_TX_SDO	iso_sync0_p	SPI_S_MISO	SIM_RST_N	GPIO_A7

Table 3-2 Pin multiplexing for GPIO_8–GPIO_15

IO Name	MUX_0	MUX_1	MUX_2	MUX_3	MUX_4	MUX_5	MUX_6	MUX_7
GPIO_8	I2C5_SCL	UART2_TX	PWM1_B	I2S_RX_SDI	UART3_CTS	SPI_S_MOSI	SIM_IO	GPIO_A8
GPIO_9	I2C5_SDA	UART2_RX	PWM1_C	I2S_SCLK	UART3_RTS	SPI_S_CS_N	SIM_CLK	GPIO_A9
GPIO_10	QSPI_M1_CS_N	I2S_S_WS	SPI_M_CS0_N	UART4_CTS	UART5_RX	PWM1_A	SPI_S_MOSI	GPIO_A10
GPIO_11	QSPI_M1_IO_3	I2S_S_TX_SDO	I2C3_SCL	UART4_RTS	UART5_TX	PWM1_B	SPI_S_CLK	GPIO_A11
GPIO_12	QSPI_M1_IO_2	I2S_S_RX_SDI	I2C3_SDA	UART4_TX	UART5_CTS	PWM1_C	SPI_S_MISO	GPIO_A12
GPIO_13	QSPI_M1_IO_1	I2S_S_SCLK	SPI_M_MISO	UART4_RX	UART5_RTS	FERP_GPIO_Trig	SPI_S_CS_N	GPIO_A13
GPIO_14	QSPI_M1_IO_0	I2C5_SCL	SPI_M_MOSI	PDM_CLKO	df_ant_switch_sel_2	UART0_TX	iso_sync1_p	GPIO_A14
GPIO_15	QSPI_M1_CLK	I2C5_SDA	SPI_M_CLK	PDM_DI	df_ant_switch_sel_3	UART0_RX	iso_sync0_p	GPIO_A15

Table 3-3 Pin multiplexing for GPIO_16–GPIO_23

IO Name	MUX_0	MUX_1	MUX_2	MUX_3	MUX_4	MUX_5	MUX_6	MUX_7
GPIO_16	QSPI_M2_CLK	DC_CLK	DSPI_SCK	SPI_M_CLK	UART4_TX	PWM0_C	I2C0_SCL	GPIO_B0
GPIO_17	QSPI_M2_IO_0	DC_IO_0	DSPI_MOSI	SPI_M_MOSI	UART2_TX	UART3_CTS	I2C0_SDA	GPIO_B1
GPIO_18	QSPI_M2_IO_1	DC_IO_1	DSPI_MISO	SPI_M_MISO	UART2_RX	UART3_RTS	PWM1_A	GPIO_B2
GPIO_19	QSPI_M2_IO_2	DC_IO_2	DSPI_DCX	SPI_M_CS0_N	UART2_CTS	UART3_TX	PWM1_B	GPIO_B3
GPIO_20	QSPI_M2_IO_3	DC_IO_3	DSPI_CSS	SPI_M_CS1_N	UART2_RTS	UART3_RX	PWM1_C	GPIO_B4
GPIO_21	QSPI_M0_CLK	SPI_M_CLK	SIM_CLK	I2S_SCLK	I2S_S_SCLK	SPI_S_CLK	I2C3_SCL	GPIO_B5
GPIO_22	QSPI_M0_IO_0	SPI_M_MOSI	SIM_IO	I2S_RX_SDI	I2S_S_TX_SDO	SPI_S_MISO	I2C3_SDA	GPIO_B6
GPIO_23	QSPI_M0_IO_1	SPI_M_MISO	SIM_RST_N	I2S_TX_SDO	I2S_S_RX_SDI	SPI_S_MOSI	I2C2_SCL	GPIO_B7

Table 3-4 Pin multiplexing for GPIO_24–GPIO_33

IO Name	MUX_0	MUX_1	MUX_2	MUX_3	MUX_4	MUX_5	MUX_6	MUX_7
GPIO_24	QSPI_M0_IO_2	SPI_M_CS0_N	SIM_PRESENCE	I2S_WS	I2S_S_WS	SPI_S_CS_N	I2C2_SDA	GPIO_B8
GPIO_25	QSPI_M0_IO_3	SPI_M_CS1_N	FERP_GPIO_Trig	UART4_RX	I2C3_SCL	I2C1_SCL	PWM0_A	GPIO_B9
GPIO_26	QSPI_M0_CS_N	SPI_M_CS0_N	UART0_CTS	SPI_M_CLK	I2C3_SDA	I2C1_SDA	PWM0_B	GPIO_B10
GPIO_27	QSPI_M2_CS_N	DC_CS_N	UART0_RTS	SPI_M_MOSI	I2C2_SCL	I2C0_SCL	PWM0_C	GPIO_B11
GPIO_28	PDM_CLKO	iso_sync1_p	UART0_TX	SPI_M_MISO	I2C2_SDA	I2C0_SDA	SPI_M_CLK	GPIO_B12
GPIO_29	PDM_DI	iso_sync0_p	UART0_RX	SPI_M_CS0_N	FERP_GPIO_Trig	DC_DCX	SPI_M_MOSI	GPIO_B13
GPIO_30	SPI_S_MOSI	I2S_SCLK	I2S_S_WS	I2C1_SCL	UART1_CTS	I2C5_SCL	SPI_M_MISO	GPIO_B14
GPIO_31	SPI_S_CLK	I2S_RX_SDI	I2S_S_TX_SDO	I2C1_SDA	UART1_RTS	I2C5_SDA	SPI_M_CS0_N	GPIO_B15
GPIO_32	SPI_S_MISO	I2S_TX_SDO	I2S_S_RX_SDI	PDM_CLKO	UART1_TX	PWM0_B	I2C0_SCL	GPIO_C0
GPIO_33	SPI_S_CS_N	I2S_WS	I2S_S_SCLK	PDM_DI	UART1_RX	PWM0_A	I2C0_SDA	GPIO_C1

Table 3-5 Pin multiplexing for AON_GPIO_0–AON_GPIO_7

IO Name	MUX_0	MUX_1	MUX_2	MUX_3	MUX_4	MUX_5	MUX_6	MUX_7
AON_GPIO_0	UART4_CTS	I2C4_SCL	PWM0_A	SIM_PRESENCE	PWM0_C	UART2_TX		AON_GPIO_0
AON_GPIO_1	UART4_RTS	I2C4_SDA	PWM0_B	SIM_RST_N	PWM1_A	UART2_RX		AON_GPIO_1
AON_GPIO_2	UART4_TX	I2C1_SCL	PWM0_C	SIM_IO	PWM1_B	iso_sync_p		AON_GPIO_2
AON_GPIO_3	UART4_RX	I2C1_SDA	PWM1_A	SIM_CLK	PWM1_C			AON_GPIO_3
AON_GPIO_4	PWM0_A	UART5_RX	I2C0_SCL	PWM1_B	SIM_CLK	coex_ble_tx		AON_GPIO_4
AON_GPIO_5	PWM0_B	UART5_TX	I2C0_SDA	PWM1_C	iso_sync_p	coex_ble_rx		AON_GPIO_5
AON_GPIO_6	PWM0_C	UART5_CTS	I2C5_SCL	PDM_CLKO	UART1_RX	coex_wlan_tx		AON_GPIO_6
AON_GPIO_7	PWM1_A	UART5_RTS	I2C5_SDA	PDM_DI	UART1_TX	coex_wlan_rx		AON_GPIO_7

Table 3-6 Pin multiplexing for MSIO_0–MSIO_7

IO Name	MUX_0	MUX_1	MUX_2	MUX_3	MUX_4	MUX_5	MUX_6	MUX_7
MSIO_0	PWM0_A	SIM_CLK	UART3_RX	I2S_SCLK	I2S_S_SCLK	PDM_DI		MSIO_A0
MSIO_1	PWM0_B	SIM_IO	UART3_TX	I2S_RX_SDI	I2S_S_RX_SDI	PDM_CLKO		MSIO_A1
MSIO_2	PWM0_C	SIM_RST_N	UART3_RTS	I2S_TX_SDO	I2S_S_TX_SDO	coex_wlan_rx		MSIO_A2
MSIO_3	PWM1_A	SIM_PRESENCE	UART3_CTS	I2S_WS	I2S_S_WS	coex_wlan_tx		MSIO_A3
MSIO_4	UART2_RTS	PWM1_B	I2C3_SDA		I2C0_SDA	coex_ble_rx	iso_sync0_p	MSIO_A4
MSIO_5	UART2_CTS	PWM1_C	I2C3_SCL		I2C0_SCL	coex_ble_tx	iso_sync1_p	MSIO_A5
MSIO_6	UART2_RX	PWM1_B	I2C4_SDA		I2C1_SDA	iso_sync0_p		MSIO_A6
MSIO_7	UART2_TX	PWM1_C	I2C4_SCL		I2C1_SCL	iso_sync1_p		MSIO_A7

4 Package Information

GR5526 offers BGA83 and QFN68 packages to support different environmental requirements.

4.1 BGA83

GR5526 BGA83, including GR5526VGBIP BGA83 and GR5526VGBI BGA83, is an 83-pin and 4.3 x 4.3 x 0.96 (mm) package. It is qualified to MSL 3.

Table 4-1 BGA83 package information

Parameter	Value	Unit	Tolerance
Package Size	4.3 x 4.3	mm	±0.1 mm
BGA Ball Count	83		
Total Thickness	0.96	mm	±0.1 mm
BGA Ball Pitch	0.40		
Ball Diameter	0.20		±0.05 mm
Ball Height	0.14		±0.05 mm

The figure below shows the BGA83 package outlines.

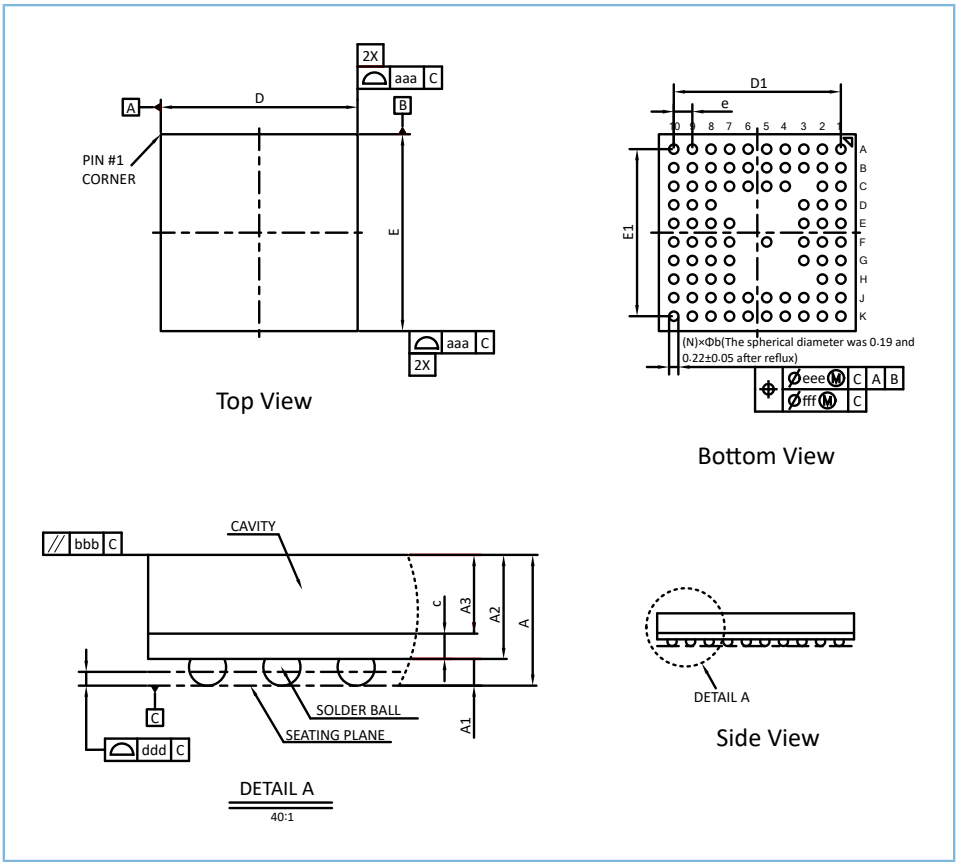

Figure 4-1 BGA83 package outlines

Note:

Drawing is not to scale.

Table 4-2 BGA83 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.860	0.960	1.060	0.034	0.038	0.042
A1	0.090	0.140	0.190	0.004	0.006	0.007
A2	0.770	0.820	0.870	0.030	0.032	0.034
A3	0.620	0.650	0.680	0.024	0.026	0.027
c	0.140	0.170	0.200	0.006	0.007	0.008
D	4.200	4.300	4.400	0.165	0.169	0.173
E	4.200	4.300	4.400	0.165	0.169	0.173
D1	-	3.600	-	-	0.142	-
E1	-	3.600	-	-	0.142	-
e	-	0.400	-	-	0.016	-
b	0.150	0.200	0.250	0.006	0.008	0.010
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

4.2 QFN68

GR5526 QFN68, including GR5526RGNIP QFN68 and GR5526RGNI QFN68, is a 68-pin and 7 x 7 x 0.85 (mm) package. It is qualified to MSL 3.

Table 4-3 QFN68 package information

Parameter	Value	Unit	Tolerance
Package Size	7.0 x 7.0	mm	±0.05 mm
QFN Pad Count	68		
Total Thickness	0.85	mm	±0.05 mm
QFN Pad Pitch	0.35		

Parameter	Value	Unit	Tolerance
Pad Width	0.15		±0.05 mm
Exposed Pad Size	5.49 x 5.49		±0.1 mm

The figure below shows the QFN68 package outlines.

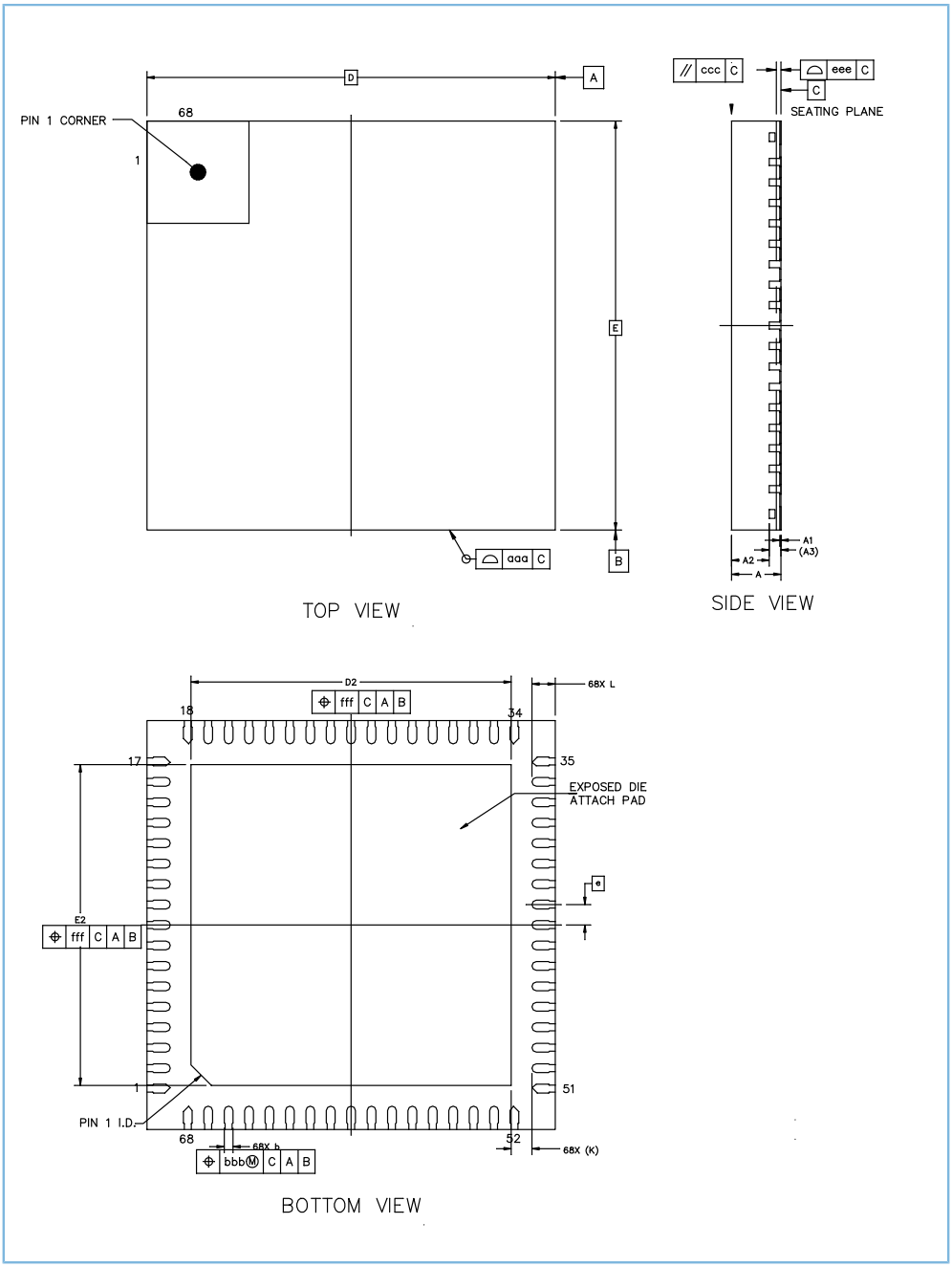

Figure 4-2 QFN68 package outlines

Note:

Drawing is not to scale.

Table 4-4 QFN68 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.800	0.850	0.900	0.031	0.033	0.035
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.650	-	-	0.026	-
A3	0.203 REF.			0.008 REF.		
b	0.100	0.150	0.200	0.004	0.006	0.008
D	7.000 BSC.			0.276 BSC.		
E	7.000 BSC.			0.276 BSC.		
e	0.350 BSC.			0.014 BSC.		
D2	5.390	5.490	5.590	0.212	0.216	0.220
E2	5.390	5.490	5.590	0.212	0.216	0.220
L	0.350	0.400	0.450	0.014	0.016	0.018
K	0.355 REF.			0.014 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

5 Glossary

Table 5-1 Glossary

Name	Description
ADC	Analog to Digital Converter
AMS	Analog Mix Signal
AON	Always-on
AONWDG	Always-on Watchdog Timer
AoA/AoD	Angle of Arrival/Angle of Departure
Bluetooth LE	Bluetooth Low Energy
DC	DisplayControl
DSI	Display Serial Interface
DSPI	Dual-lane SPI
ESL	Electronic Shelf Label
IoT	Internetof Things
MIPI	MobileIndustry Processor Interface
MPU	Hardware Floating Point Unit
NMI	Non-maskable Interrupt
NVIC	Built-in Nested Vectored Interrupt Controller
LDO	Low Dropout
MPU	Built-in Memory Protection Unit
PMU	Power Management Unit
QSPI	Quad SPI
RNG	RING Oscillator
RTC	Real-time Counters
SoC	System-on-Chip
TPMS	Tire Pressure Monitor System
XIP	Execute-In-Place
XO	Crystal Oscillator

6 Legal and Contact Information

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7 Revision History

Table 7-1 Revision history

Version	Date	Description
1.0	2022-06-24	Initial release
1.1	2023-01-10	Updated "Block Diagram".