GR5526 Hardware Design Guidelines

Version: 1.1

Release Date: 2023-01-10

Shenzhen Goodix Technology Co., Ltd.

Trademarks and Permissions

GOODiX and other Goodix trademarks are trademarks of Shenzhen Goodix Technology Co., Ltd. All other trademarks and trade names mentioned in this document are the property of their respective holders.

Disclaimer

Information contained in this document is intended for your convenience only and is subject to change without prior notice. It is your responsibility to ensure its application complies with technical specifications.

Shenzhen Goodix Technology Co., Ltd. (hereafter referred to as “Goodix”) makes no representation or guarantee for this information, express or implied, oral or written, statutory or otherwise, including but not limited to representation or guarantee for its application, quality, performance, merchantability or fitness for a particular purpose. Goodix shall assume no responsibility for this information and relevant consequences arising out of the use of such information.

Without written consent of Goodix, it is prohibited to use Goodix products as critical components in any life support system. Under the protection of Goodix intellectual property rights, no license may be transferred implicitly or by any other means.

Shenzhen Goodix Technology Co., Ltd.

Headquarters: Floor 12-13, Phase B, Tengfei Industrial Building, Futian Free Trade Zone, Shenzhen, China

TEL: +86-755-33338828 Zip Code: 518000

Website: www.goodix.com

Preface

Purpose

This document presents the necessary circuit required for proper operation of GR5526 Bluetooth System-on-Chips (SoCs). Recommended chip interfaces, peripherals, schematic diagram, and PCB layout guidelines of the GR5526 SoC family are provided.

This *Hardware Design Guidelines* intends to help system designers build minimal Bluetooth Low Energy (Bluetooth LE) hardware circuits and develop Bluetooth products.

Audience

This document is intended for:

- GR5526 user
- GR5526 tester
- Bluetooth product engineer
- Bluetooth LE system designer

Release Notes

This document is the second release of *GR5526 Hardware Design Guidelines*, corresponding to GR5526 SoC series.

Revision History

Version	Date	Description
1.0	2022-06-24	Initial release
1.1	2023-01-10	Updated "Block Diagram", "Pinout", "RF Scheme" and "Reference Schematic Diagram".

Contents

1 GR5526 Overview

The Goodix GR5526 family is a single-mode, low-power Bluetooth 5.3 System-on-Chip (SoC). It can be configured as a Broadcaster, an Observer, a Central, and a Peripheral and supports the combination of all the above roles, making it an ideal choice for Internet of Things (IoT) and smart wearable devices. In addition, it supports Bluetooth Low Energy (Bluetooth LE) direction finding: angle of arrival (AoA) and angle of departure (AoD), as well as LE Audio, made possible by LE Isochronous Channels.

Based on ARM® Cortex®-M4F CPU core, the GR5526 series integrates Bluetooth 5.3 Protocol Stack, a 2.4 GHz RF transceiver, on-chip programmable Flash memory, RAM, multiple peripherals, enhanced I2C/UART port number for sensor applications, as well as expanded I/O functionality. GR5526 delivers a feature-rich display and graphics solution by providing the choice of graphics acceleration (GPU + DC) and internal/external system-in-package (SiP) pseudostatic RAM (PSRAM) to accommodate display while still leaving plenty of space for wearable schemes.

GR5526 series comes in two package choices: BGA83 and QFN68 (as shown in the table below), that can meet diverse application scenarios.

Table 1-1 GR5526 series

Features	GR5526VGBIP	GR5526VGBI	GR5526RGNIP	GR5526RGNI
CPU	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F	Cortex®-M4F
RAM	512 KB	512 KB	512 KB	512 KB
SiP Flash	1 MB	1 MB	1 MB	1 MB
SiP PSRAM	8 MB	N/A	8 MB	N/A
GPU + DC	Supported	N/A	Supported	N/A
I/O number	50	50	48	48
Package (mm)	BGA83 (4.3 x 4.3 x 0.96)	BGA83 (4.3 x 4.3 x 0.96)	QFN68 (7.0 x 7.0 x 0.85)	QFN68 (7.0 x 7.0 x 0.85)

1.1 Features

- Bluetooth Low Energy 5.3 transceiver integrating Controller and Host layers
  - Supported data rates: 1 Mbps, 2 Mbps, and Long Range (500 kbps, 125 kbps)
  - TX power: -20 dBm to +7 dBm
  - -98 dBm sensitivity (in 1 Mbps mode)
  - -94 dBm sensitivity (in 2 Mbps mode)
  - -101 dBm sensitivity (in Long Range 500 kbps mode)
  - -104 dBm sensitivity (in Long Range 125 kbps mode)
  - TX current: 4.0 mA @ 0 dBm, 1 Mbps
  - RX current: 3.5 mA @ 1 Mbps
  - AoA/AoD, LE Isochronous Channels

- ARM® Cortex®-M4F 32-bit micro-processor with floating point support
  - Up to 96 MHz clock frequency
  - Built-in Memory Protection Unit (MPU) supporting eight programmable regions
  - Hardware Floating Point Unit (FPU)
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Non-maskable Interrupt (NMI) input
  - Serial Wire Debug (SWD) with 16 breakpoints, two watchpoints, and a debug timestamp counter
  - 51 µA/MHz execution from Flash @ 3.3 V, 96 MHz
- On-chip memory
  - 512 KB data SRAM with retention capabilities
  - 8 KB cache SRAM with retention capabilities
  - Stack ROM (including boot ROM and Bluetooth LE Stack)
  - 1 MB internal QSPI Flash
  - 8 MB internal PSRAM (for GR5526VGBIP and GR5526RGNIP only)
- Digital peripherals
  - Two general-purpose DMA engines, each with six channels and up to 16 handshaking interfaces
  - USB 2.0 full speed (12 Mbps) controller with on-chip PHY and dedicated DMA controller
  - Internal Octal SPI DDR interfaces to support 8 MB internal PSRAM at up to 48 MHz (for GR5526VGBIP and GR5526RGNIP only)
- Analog peripherals
  - One 13-bit Sense ADC with a sampling rate of 1 Msps. It supports up to 8 external I/O channels and 3 internal signal channels.
  - Built-in temperature and voltage sensors
  - Low-power comparator, supporting wakeup from deep sleep mode
- Flexible serial peripherals
  - 6 x UART modules up to 4 Mbps, with all modules supporting flow control and IrDA
  - 6 x I2C modules for peripheral communication, up to 3.4 MHz
  - 1 x 8-bit/16-bit/32-bit SPI master interface and 1 x SPI slave interface for host communication
  - 2 x I2S interfaces (1 I2S master interface and 1 I2S slave interface)
  - PDM interface with hardware sampling rate converter
  - 1 x ISO7816 interface

- Display/Graphics
  - 2.5D GPU for graphics acceleration (for GR5526VGBIP and GR5526RGNIP only)
  - 1 x Dual-lane SPI (DSPI) interface for display, with Mobile Industry Processor Interface (MIPI) Display Bus Interface (DBI) Type-C support
  - 3 x Quad SPI (QSPI) interfaces, up to 48 MHz; supporting direct access via memory mapping when connecting with external NOR Flash
  - Display Controller (DC) module with MIPI DBI Type-C support and 2D graphics blending integrated (for GR5526VGBIP and GR5526RGNIP only)
- Security
  - Complete secure computing engine:
    - AES 128-bit/192-bit/256-bit symmetric encryption (ECB, CBC)
    - Hash-based Message Authentication Code (HMAC-SHA256)
    - Public key cryptography (PKC)
    - True random number generator (TRNG)
  - Comprehensive security operation mechanism:
    - Secure boot
    - Encrypted firmware running directly from Flash
    - eFuse for encrypted key storage
    - Differentiate application data key and firmware key, supporting one data key per each device/product
- I/O Peripherals
  - 50 I/O pins in total
    - 34 general-purpose I/O (GPIO) pins
    - 8 always-on I/O (AON IO) pins, supporting wakeup from deep sleep mode
    - 8 mixed signal I/O (MSIO) pins, configurable to be digital/analog signal interface
- Timer
  - Two general-purpose, 32-bit timer modules
  - A timer module composed of two programmable 32-bit or 16-bit down counters
  - An internal sleep timer that can be used to wake the device up from deep sleep mode
  - Two PWM modules with edge alignment mode and center alignment mode, each with 3 channels
  - 2 x real-time counters (RTC): 1 x Calendar, 1 x RTC
- Power management

  - On-chip DC-DC to provide RF Analog voltage and supply core LDO
  - On-chip I/O LDO to provide I/O voltage and supply external components, maximum I/O LDO drive strength: 30 mA
  - Programmable thresholds for brownout detection (BOD)
  - Supply voltage: 2.4 V–4.35 V
  - I/O voltage: 1.8 V–3.6 V
- Low-power consumption modes
  - Sleep mode: 3.3 µA (Typical) at 3.3 V VBAT input with 128 KB SRAM retention on and LFXO_32K off; woken up by 8 sources of always-on domain
  - Ultra deep sleep mode: 2.4 µA (Typical); internal power (all SRAM included) and LFXO_32K removed from entire chip except always-on domain; woken up by Sleep Timer and AON GPIOs
  - OFF mode: 200 nA (Typical); nothing on except VBAT, and chip in reset mode
- Packages
  - BGA83: 4.3 x 4.3 x 0.96 (mm), 0.4 mm pitch
  - QFN68: 7.0 x 7.0 x 0.85 (mm), 0.35 mm pitch
- Operating temperature range: -40°C to +85°C

1.2 Block Diagram

The block diagram of GR5526 is shown in the figure below.

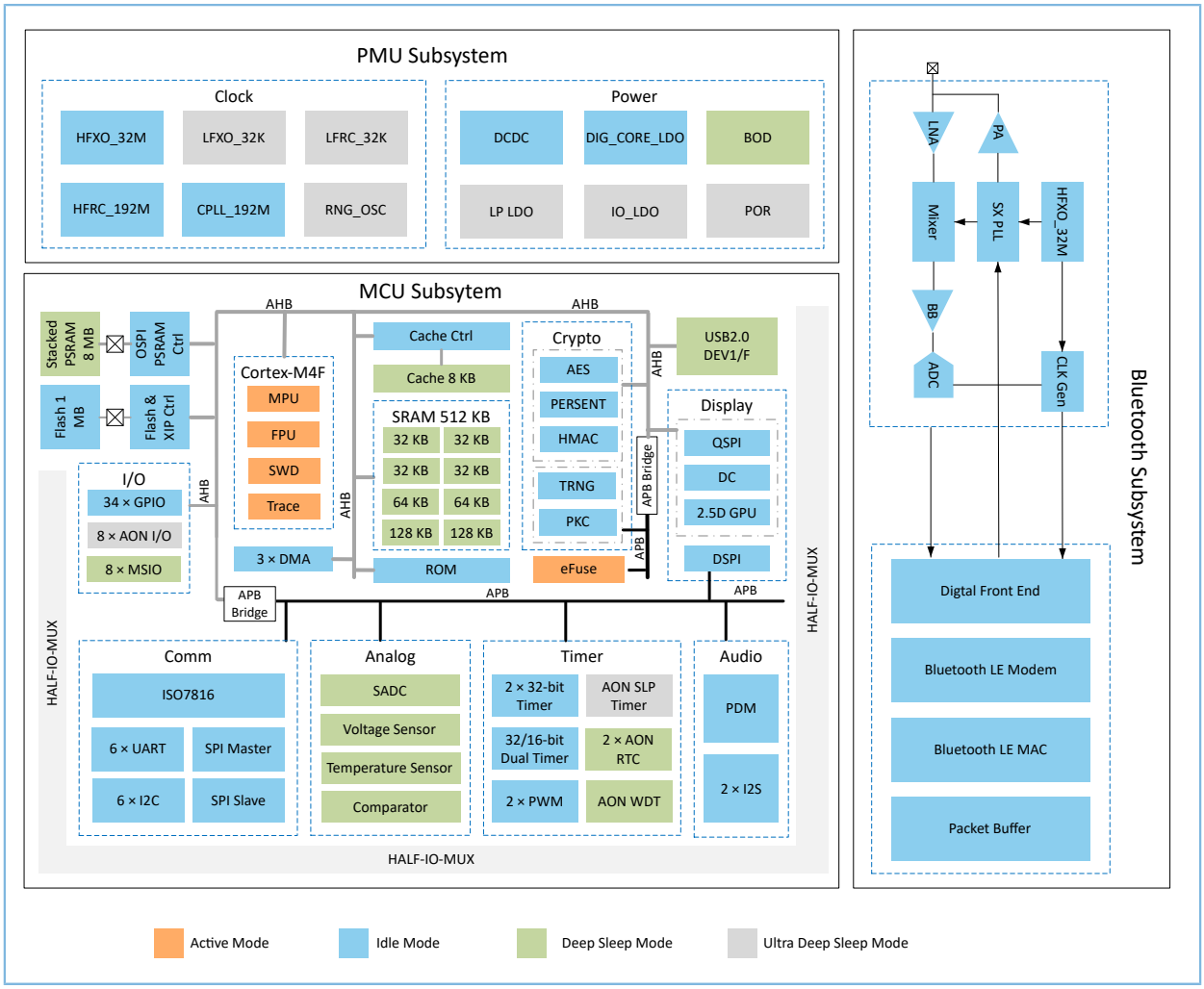

Figure 1-1 GR5526 block diagram

- Bluetooth subsystem
  - A 2.4 GHz transceiver and a digital communication core that supports Bluetooth 5.3
- MCU subsystem
  - An ARM® Cortex®-M4F with all the required memories and peripherals
  - Security cores that can be used for application security and secure boot implementation
  - GPU + DC to enhance processing capabilities
- Power management unit (PMU) subsystem
  - All the required power management modules to supply sufficient power for both internal modules and external peripherals
  - Modules required for ultra-low-power operation are in standby mode. HFRC_192M, RNG_OSC, LFRC_32K, wakeup GPIOs (Wake up), low-power comparator (LP Comp.), and power state controller (Power Sequencer) are used to control the state of different modules

2 Pinout

This chapter introduces GR5526 pinout available in BGA83 and QFN68 packages and provides detailed descriptions.

2.1 BGA83

The figure below shows the pins assignment (top view) of a GR5526 BGA83 package that is applicable to GR5526VGBIP and GR5526VGBI.

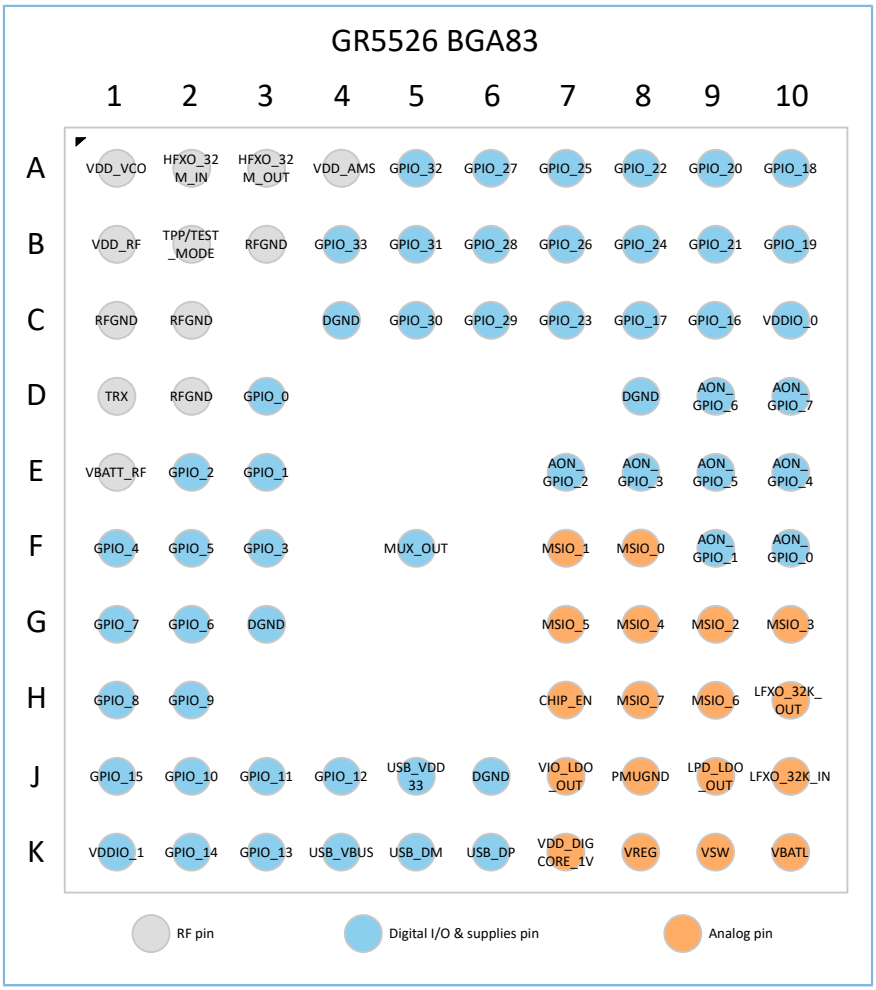

Figure 2-1 GR5526 BGA83 package pinout

The table below shows pin descriptions of a GR5526 BGA83 package.

Table 2-1 GR5526 BGA83 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A1	VDD_VCO	Analog/RF Supply	Synthesizer VCO supply; connect to VREG	
A2	HFXO_32M_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
A3	HFXO_32M_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
A4	VDD_AMS	Analog/RF Supply	AMS supply: 1.1 V; connect to VREG	

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
A5	GPIO_32	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A6	GPIO_27	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A7	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A8	GPIO_22	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A9	GPIO_20	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
A10	GPIO_18	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B1	VDD_RF	Analog/RF supply	RF supply: 1.1 V; connect to VREG	
B2	TPP/TEST_MODE	Analog/RF	Input pin, used to set test mode for factory test. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	
B3	RFGND	RF	RF ground	
B4	GPIO_33	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B5	GPIO_31	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B6	GPIO_28	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B7	GPIO_26	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B8	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B9	GPIO_21	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
B10	GPIO_19	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C1	RFGND	RF	RF ground	
C2	RFGND	RF	RF ground	
C4	DGND	Digital Ground	Digital ground	
C5	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C6	GPIO_29	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C7	GPIO_23	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C8	GPIO_17	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C9	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
C10	VDDIO_0	Digital Supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO0
D1	TRX	Analog/RF	RX input and TX output	
D2	RF_GND	RF	RF ground	
D3	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 4 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
D8	DGND	Digital Ground	Digital ground	
D9	AON_GPIO_6	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
D10	AON_GPIO_7	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E1	VBATT_RF	Analog/RF Supply	Connected to VBATL	
E2	GPIO_2	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
E3	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 4 mA.	VDDIO1
E7	AON_GPIO_2	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E8	AON_GPIO_3	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E9	AON_GPIO_5	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
E10	AON_GPIO_4	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
F1	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
F2	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
F3	GPIO_3	Digital I/O	General purpose I/O, configurable to be an SWO interface; pad drive level is 4 mA.	VDDIO1
F5	MUX_OUT	PMU	-	
F7	MSIO_1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
F8	MSIO_0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
F9	AON_GPIO_1	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
F10	AON_GPIO_0	Digital I/O	Always-on GPIO; pad drive level is 4 mA.	VDDIO0
G1	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
G2	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
G3	DGND	Digital Ground	Digital ground	
G7	MSIO_5	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G8	MSIO_4	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G9	MSIO_2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
G10	MSIO_3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H1	GPIO_8	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
H2	GPIO_9	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
H7	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin The high level of CHIP_EN equals VBATL.	
H8	MSIO_7	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H9	MSIO_6	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
H10	LFXO_32K_OUT	PMU	Output of inverting amplifier connected to 32.768 kHz crystal	
J1	GPIO_15	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J2	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J3	GPIO_11	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J4	GPIO_12	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
J5	USB_VDD33	USB	Internal output voltage: USB 3.3 V	
J6	DGND	Digital Ground	Digital ground	
J7	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator	
J8	PMUGND	PMU	DC/DC converter supply and general battery GND	
J9	LPD_LDO_OUT	PMU	Output of low power domain LDO	
J10	LFXO_32K_IN	PMU	Input of inverting amplifier connected to 32.768 kHz crystal	
K1	VDDIO_1	Digital Supply	I/O supply voltage. Support external 1.8 V–3.3 V input voltage.	VDDIO1
K2	GPIO_14	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
K3	GPIO_13	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
K4	USB_VBUS	USB	Input voltage: USB 5 V	
K5	USB_DM	USB	USB D- Pin	
K6	USB_DP	USB	USB D+ Pin	
K7	VDD_DIGCORE_1V	PMU	On-chip LDO output for digital core	
K8	VREG	PMU	Feedback pin of switch regulator	
K9	VSW	PMU	DC/DC converter switching node	
K10	VBATL	PMU	Power supply: 2.4 V to 4.35 V	

2.2 QFN68

The figure below shows the pins assignment (top view) of a GR5526 QFN68 package that is applicable to GR5526RGNIP and GR5526RGNI.

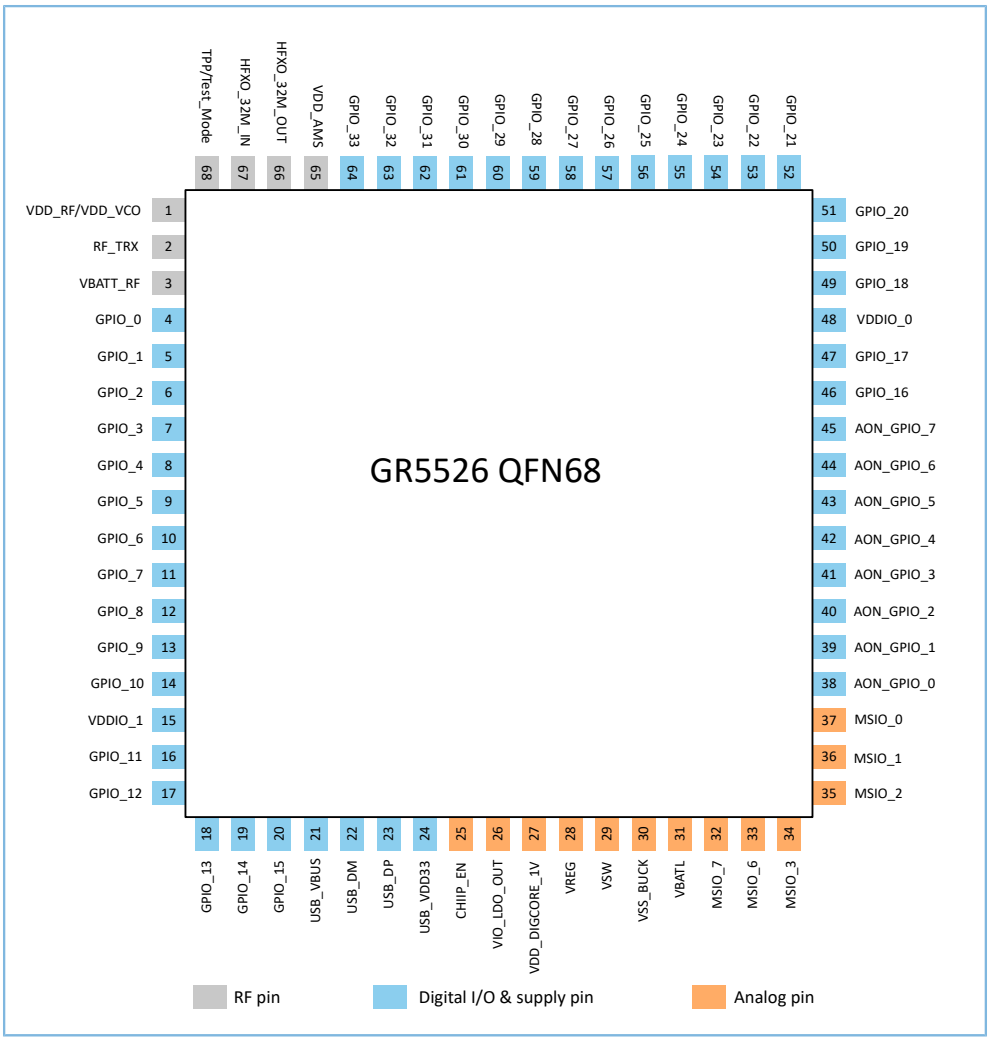

Figure 2-2 GR5526 QFN68 package pinout

The table below shows pin descriptions of a GR5526 QFN68 package.

Table 2-2 GR5526 QFN68 package pin descriptions

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
1	VDD_VCO/VDD_RF	Analog/RF supply	Synthesizer VCO supply/RF supply: 1.1 V; connect to VREG	
2	RF_TRX	Analog/RF	RX input and TX output	
3	VBATT_RF	Analog/RF Supply	Connected to VBATL	
4	GPIO_0	Digital I/O	General purpose I/O; default: SWD_CLK; pad drive level is 4 mA.	VDDIO1

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
5	GPIO_1	Digital I/O	General purpose I/O; default: SWD_IO; pad drive level is 4 mA.	VDDIO1
6	GPIO_2	Digital I/O	General purpose I/O, configurable to be an SWO interface; pad drive level is 4 mA.	VDDIO1
7	GPIO_3	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
8	GPIO_4	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
9	GPIO_5	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
10	GPIO_6	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
11	GPIO_7	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
12	GPIO_8	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
13	GPIO_9	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
14	GPIO_10	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
15	VDDIO_1	Digital I/O supply	Digital I/O supply input. Support external 1. 8 V–3.3 V input voltage.	VDDIO1
16	GPIO_11	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
17	GPIO_12	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
18	GPIO_13	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
19	GPIO_14	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
20	GPIO_15	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO1
21	USB_VBUS	USB	Input voltage: USB 5 V	
22	USB_DM	USB	USB D- pin	
23	USB_DP	USB	USB D+ pin	
24	USB_VDD33	USB	Internal output voltage: USB 3.3 V	
25	CHIP_EN	Mixed Signal IN	Master Enable for chip reset pin. The high value of CHIP_EN equals VBATL.	
26	VIO_LDO_OUT	PMU	Output of on-chip I/O supply regulator	
27	VDD_DIGCORE_1V	Analog/PMU	On-chip LDO output for digital core	
28	VREG	Analog/PMU	Feedback pin of switch regulator	
29	VSW	Analog/PMU	DC/DC converter switching node	
30	VSS_BUCK	Analog/PMU	DC/DC converter supply and general battery GND	
31	VBATL	Analog/PMU	Power supply: 2.4 V to 4.35 V	
32	MSIO_7	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); multiplexed by LFXO_32K_IN; pad drive level is 2 mA.	VBATL

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
33	MSIO_6	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); multiplexed by LFXO_32K_OUT; pad drive level is 2 mA.	VBATL
34	MSIO_3	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
35	MSIO_2	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
36	MSIO_1	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
37	MSIO_0	Mixed Signal I/O	Configurable to be a GPIO mixed signal (SNSADC interface); pad drive level is 2 mA.	VBATL
38	AON_GPIO_0	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
39	AON_GPIO_1	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
40	AON_GPIO_2	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
41	AON_GPIO_3	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
42	AON_GPIO_4	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
43	AON_GPIO_5	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
44	AON_GPIO_6	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
45	AON_GPIO_7	Digital I/O	Always-on general purpose I/O; pad drive level is 4 mA.	VDDIO0
46	GPIO_16	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
47	GPIO_17	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
48	VDDIO_0	Digital I/O supply	Digital I/O supply input. Support external 1.8 V–3.3 V input voltage.	VDDIO0
49	GPIO_18	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
50	GPIO_19	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
51	GPIO_20	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
52	GPIO_21	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
53	GPIO_22	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
54	GPIO_23	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
55	GPIO_24	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
56	GPIO_25	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
57	GPIO_26	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
58	GPIO_27	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
59	GPIO_28	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
60	GPIO_29	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0

Pin #	Pin Name	Pin Type	Description/Default Function	Voltage Domain
61	GPIO_30	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
62	GPIO_31	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
63	GPIO_32	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
64	GPIO_33	Digital I/O	General purpose I/O; pad drive level is 4 mA.	VDDIO0
65	VDD_AMS	Analog/RF	AMS supply: 1.1 V. Connect to VREG.	
66	HFXO_32M_OUT	Analog/RF	Output of inverting amplifier connected to 32 MHz crystal	
67	HFXO_32M_IN	Analog/RF	Input of inverting amplifier connected to 32 MHz crystal	
68	TPP/TEST_MODE	Analog/RF	Input pin, used to set test mode for factory test. • If TEST_MODE = 1, the chip is in test mode for factory test. • If TEST_MODE = 0, the chip is in normal operation mode.	

3 Minimal Design for GR5526 SoC

The absolute necessary sections required for the GR5526 SoC minimal system operation include

- Power supply
- Clock
- RF
- I/O pins
- SWD interfaces

To ensure the proper operation of a GR5526 SoC, the design guidelines for the schematic diagram and the PCB layout are illustrated in the following sections.

3.1 Schematic Design Guideline

For the minimal schematic for a GR5526 SoC, see "Section 4.1 Reference Schematic Diagram".

3.1.1 Power Supply

3.1.1.1 Introduction

GR5526 SoCs are powered by external power sources through VBATL (voltage range: 2.4 V to 4.35 V).

To avoid the switch overshoot caused by battery welding, connect the battery to a resistor (0.39 Ω – 1 Ω) and VBATL in series when powering on a GR5526 SoC in operation. It is recommended to convert the battery voltage to 3.3 V with LDO or DC-DC before supplying VBATL.

3.1.1.2 Time Sequence

1. During cold boot, after GR5526 is powered on, the time for VBATL rising from 0 V to the operating voltage is within 50 ms.

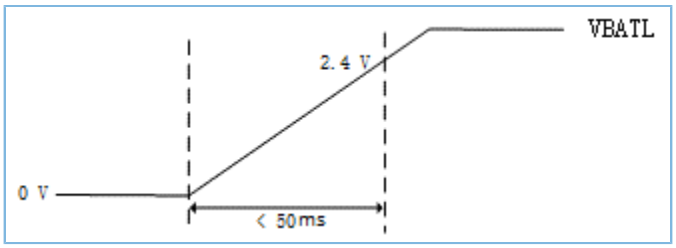

Figure 3-1 VBATL rising time

2. CHIP_EN shall not be powered on earlier than VBATL.

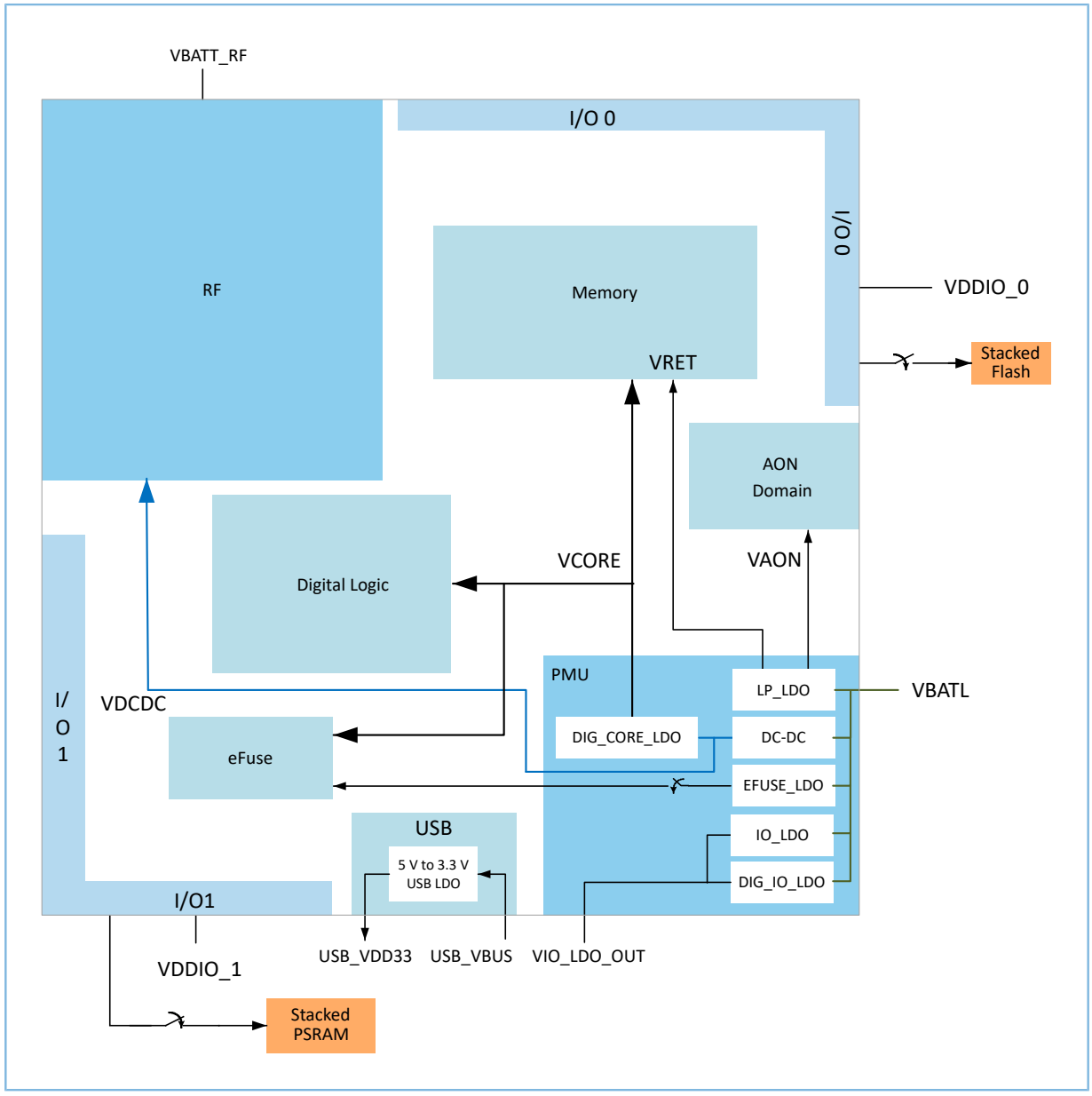

Figure 3-2 Power architecture

As shown in Figure 3-2, power architecture is based on a PMU (Power Management Unit), which is connected to an external supply VBATL and generates the following supplies:

- VDDIO0: supply for I/O0 group, connected to stacked Flash and set to voltage required by Flash
- VDDIO1: supply for I/O1 group, connected to stacked PSRAM and set to voltage required by PSRAM
- VAON: supply for AON domain
- VRET: retention supply for memory instances
- VCORE: supply for digital core
- VDCDC: supply for RF

The USB analog module is powered by a 5 V external power supply through USB_VBUS. The embedded USB LDO converts 5 V to 3.3 V, which is needed for level translation of internal USB differential pair signaling.

3.1.1.3 Power Supply Scheme

GR5526 SoCs are equipped with a complete set of power management modules which guarantee the smooth and secure functioning of the GR5526 SoCs. This section introduces the GR5526 reference circuit design by taking a GR5526 SoC mounting BGA83 package as an example (see Figure 3-3).

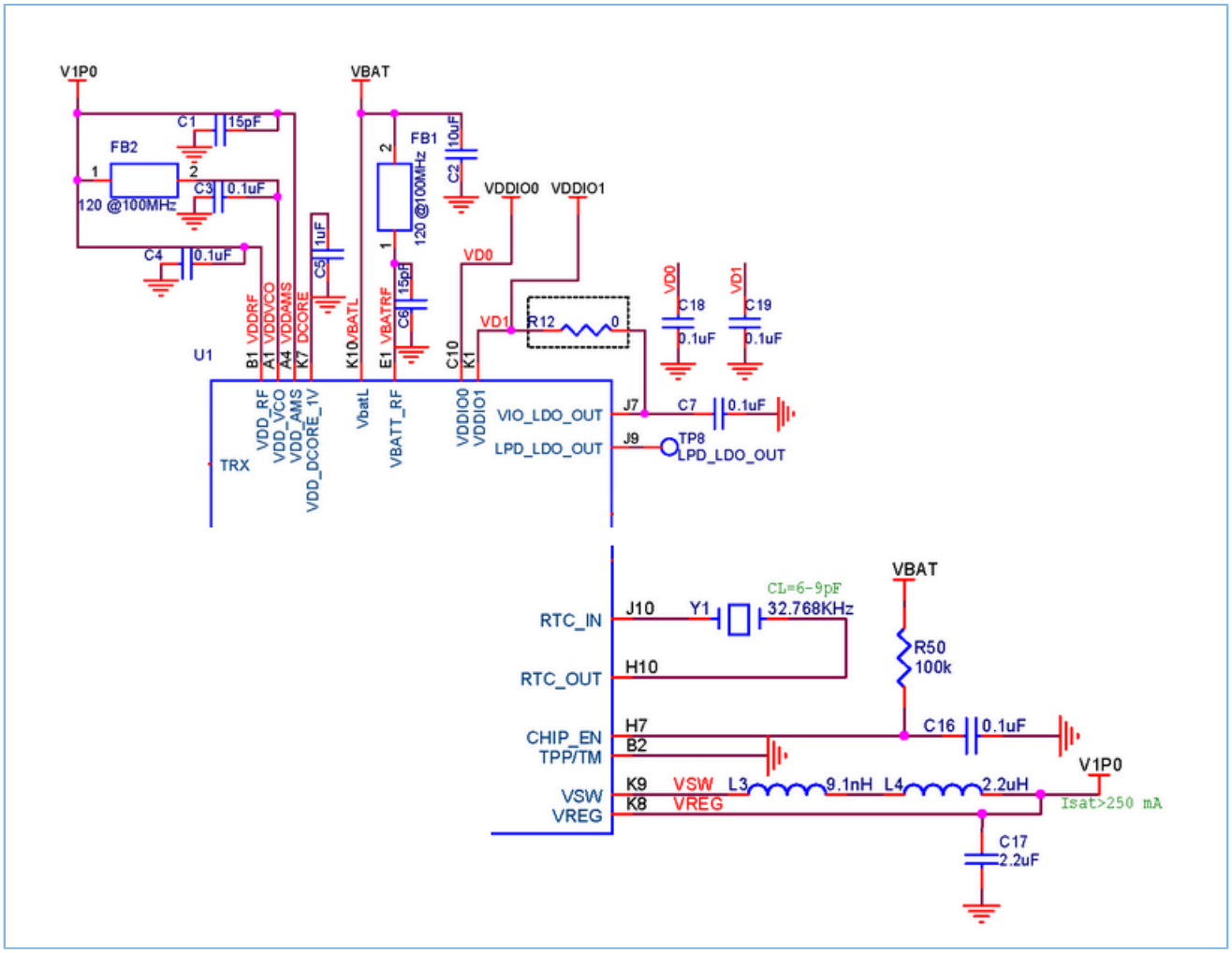

Figure 3-3 Power section of GR5526

The detailed pin descriptions and connection guidance are as follows:

- **VDD_RF:** internal RF block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 0.1 µF filter capacitor
- **VDD_VCO:** internal VCO block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 0.1 µF filter capacitor
- **VDD_AMS:** internal analog block supply, connected to V1P0 (output power net of DC-DC switching regulator) and a 15 pF filter capacitor

- **VDD_DIGCORE_1V:** output of digital LDO, which supplies the digital core logic. Place a 1 µF filter capacitor on this pin
- **VBATL:** input supply for chip – ranging from 2.4 V to 4.35 V; connected to a 10 µF filter capacitor; the ripple noise of the power supply does not exceed 40 mV
- **VBATT_RF:** connected to VBATL
- **VIO_LDO_OUT:** output of the on-chip VDDIO LDO regulator. It can supply the VDDIO pins and external sensors with up to 30 mA load current. Connected to a 0.1 µF decoupling capacitor
- **VSW:** DC-DC switching regulator output, connected to two inductors in series: a 9.1 nH inductor for reducing RF interference caused by switching noise and a 2.2 µH power inductor, as well as a 2.2 µF capacitor, to supply the SoC from V1P0 as a complete DC-DC circuit. The pin is also connected to VDD_RF, VDD_AMS, and VDD_VCO through external circuits
- **VREG:** feedback pin from the DC-DC switching regulator output, connected to V1P0
- **VDDIO0:** supply for I/O0 voltage domain, supplied from VIO_LDO_OUT or external regulator, connected to a 0.1 µF filter capacitor and stacked Flash with voltage set as required by Flash
- **VDDIO1:** supply for I/O1 voltage domain, supplied from VIO_LDO_OUT or external regulator, connected to a 0.1 µF filter capacitor and stacked PSRAM and set to 1.8 V as required by PSRAM

Recommended capacitors, ferrite beads, and inductors are listed in Table 3-1 and Table 3-2.

Table 3-1 Recommended decoupling capacitors and ferrite beads for the power section

Reference	Description	Value	Package	Mfg Part #
C17	CAP CER X5R 10% 6.3 V	2.2 µF	0603	Murata GRM188R61C225KE15D
C3, C4, C7, C8, C16	CAP CER X7R 10% 10 V	0.1 µF	0402	Murata GRM155R71A104KA01D
C5	CAP CER X5R 10% 6.3 V	1 µF	0402	Samsung CL05A105KO5NNNC
C2	CAP CER X5R 20% 10 V	10 µF	0603	Murata GRM188R61A106ME69
C1, C6	CAP CER NPO ±5% 50 V	15 pF	0402	Murata GRM1555C1H150JA01D
FB1, FB2	Ferrite Bead, 120 Ω @ 100 MHz, 400 mA, 500 mohm, 0603	120 Ω @ 100 MHz	0603	Murata BLM18AG121SN1

Table 3-2 DC-DC inductor (9.1 nH) recommended for use

Reference	Value	DC Resistance (Max.)	Saturation Current	Size L x W x H (mm)	Mfg Part #
L3	9.1 nH	0.32 Ω	300 mA	1.0 x 0.5 x 0.5	Murata LQG15HS9N1J02D

Table 3-3 DC-DC inductors (2.2 µH) recommended for use

Reference	Value	DC Resistance (Typ.)	Saturation Current	Size L x W x H (mm)	Mfg Part #
L4	2.2 µH ± 20%	0.3 Ω	250 mA	1.6 x 0.8 x 0.8	Sunlord MPH160809S2R2
		0.2 Ω	250 mA	1.6 x 0.8 x 0.8	Murata LQM18PN2R2MGH
		0.38 Ω	300 mA	1.6 x 0.8 x 0.8	Murata LQM18PN2R2MFH

The 2.2 µH DC-DC inductors are adopted in DC-DC buck converter circuits in Pulse Skip Mode (PSM) and play a crucial role in these circuits. The saturation current of the circuit shall be higher than 250 mA. To ensure secure operation and to improve the performance of GR5526, inductors with higher saturation current and lower direct current resistance are preferred, because a higher direct current resistance means higher power consumption.

3.1.1.4 I/O LDO

The GR5526 has an on-chip linear LDO regulator that is used to supply a nominal 1.8 V (default value) for use in supplying the on-chip PSRAM. Additionally, this regulator can supply external components (sensors) which interface to the GR5526. The LDO is capable of supplying up to 30 mA load current.

The output of this regulator is the VIO_LDO_OUT pin. A 0.1 µF decoupling capacitor should be placed close to this pin.

Three I/O voltage domains are provided for GR5526: two digital voltage domains (VDDIO0 and VDDIO1), as well as one mixed signal I/O domain MSIO, corresponding to reference voltage levels at VDDIO0, VDDIO1, and VBATL respectively. Figure 3-4 is a circuit diagram showing the connection between VIO_LDO_OUT and the I/O domains.

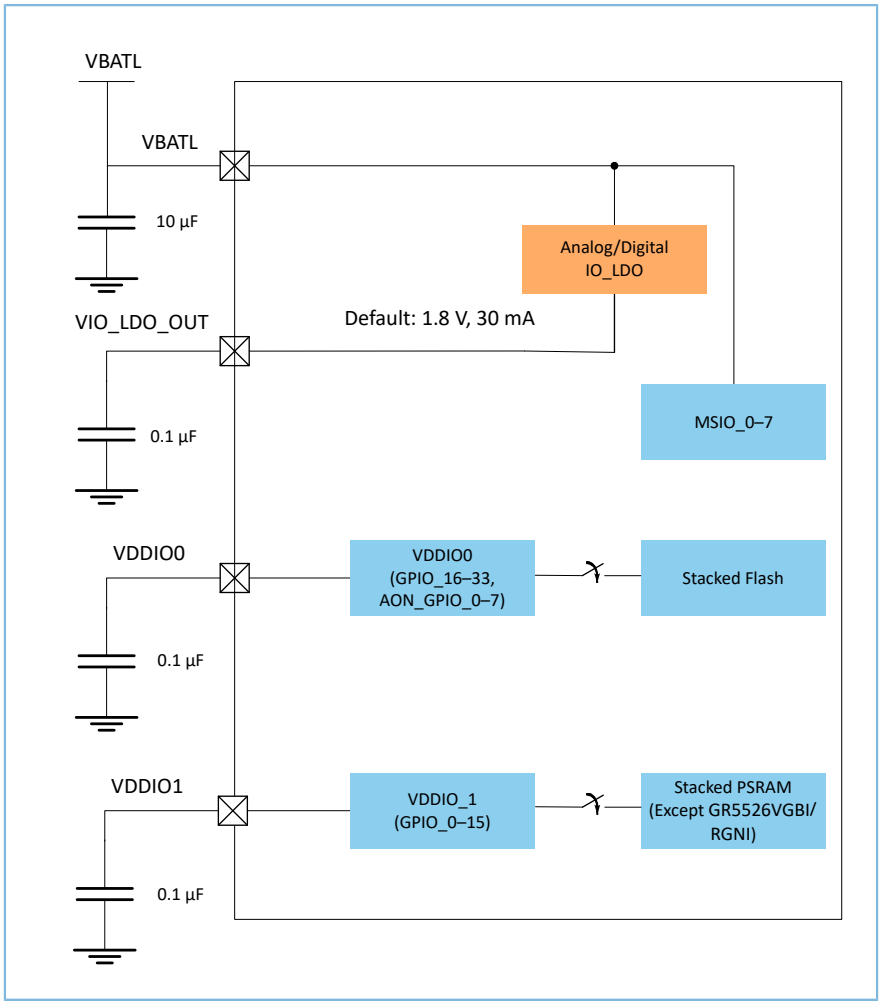

Figure 3-4 Connection between VIO_LDO_OUT and I/O domains

Note:

- For GR5526VGBIP and GR5526RGNIP, VDDIO0 input voltage ranges from 1.8 V to 3.6 V, and VDDIO1 input voltage is 1.8 V only.
- For GR5526VGBI and GR5526RGNI, input voltages for both VDDIO0 and VDDIO1 range from 1.8 V and 3.6 V.

3.1.2 Clock

3.1.2.1 Introduction

GR5526's clock source is generated by an external 32 MHz crystal oscillator, and the real-time clock (RTC) by an external 32.768 kHz crystal oscillator.

3.1.2.2 HFXO_32M

The system clock, or CPU clock, is based on a 32 MHz crystal oscillator. Table 3-4 shows the specification for the crystals that can be used for these applications, and Table 3-5 shows some recommended component examples.

Table 3-4 GR5526 crystal specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Crystal Freq	Crystal oscillator frequency			32		MHz
ESR	Equivalent series resistance				100	ohm
C_{load}	Load capacitance		6		8	pF
f-Xtal	Crystal frequency initial tolerance				±50	ppm
f-Xtal	Crystal frequency tolerance – over temperature				±30	ppm
f-Xtal	Crystal frequency tolerance – aging over life of product				±10	ppm
P_{DRV}	Max drive power				100	µW

Table 3-5 Recommended 32 MHz crystal examples

Part Number	Abracon ABM10W-32.0000MHZ-6-D1X-T3	TAITIEN G0068-X-006-3	Murata XRCGB32M000F5N10R0	TXC 8Z32000004
Frequency	32 MHz	32 MHz	32 MHz	32 MHz
Initial tolerance	±10 ppm	±40 ppm	±50 ppm	±10 ppm
Tolerance over Temp.	±20 ppm	±30 ppm	±30 ppm	±20 ppm
Load capacitance	6 pF	6 pF	6 pF	8 pF
ESR	70 ohm	30 ohm	≤ 100 Ω	≤ 60 Ω
Temperature range	–40°C to +85°C	–40°C to +105°C	-40°C to +85°C	-40°C to +85°C
Size (L x W x H, mm)	2.5 x 2.0 x 0.60	2.5 x 2.0 x 0.60	2.0 x 1.6 x 0.60	2.5 x 2.0 x 0.60

Note:

To ensure system stability and low power consumption, load capacitance of the 32 MHz crystal oscillator shall be within the range from 6 pF to 8 pF. The 32 MHz crystal oscillator does not need to be connected with load capacitors, but it needs to use the production tool for frequency offset calibration. When designing an application circuit, you shall reserve the interface or test points (SWDCLK, SWDIO, CLK_TRIM (any GPIOs except MSIOs), GND, VBAT) required by the mass production tool.

3.1.2.3 LFXO_32K

GR5526 uses a low-power, low-frequency clock in deep sleep modes, which also extends battery lifespan. An external 32.768 kHz crystal oscillator is recommended, to ensure tighter timing and better accuracy, as well as lower overall power consumption.

Note:

For applications that require less accurate RTCs, use an internal LFRC_32K instead of an external 32.768 kHz crystal oscillator to save device cost.

GR5526 integrates an adjustable load capacitance, and typically no external load capacitors are required.

The external crystal must meet the recommended operating conditions as indicated in Table 3-6, and Table 3-7 shows examples of crystals that meet the specifications.

Table 3-6 32.768 kHz crystal oscillator recommended operating conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Crystal Freq	Crystal oscillator frequency			32.768		kHz
ESR	Equivalent series resistance				100,000	ohm
Cload	Load capacitance		6		9	pF
f-Xtal	Crystal frequency initial tolerance				±50	ppm
f-Xtal	Crystal frequency tolerance – over temperature and aging				±250	ppm
PDRV	Max drive power				0.5	µW

Table 3-7 32.768 kHz crystal oscillator example specifications

Part Number	Abracon ABS05-32.768KHZ-9-T
Frequency	32.768 kHz
Initial tolerance	±20 ppm
Tolerance over Temp.	±250 ppm
Load capacitance	9 pF
ESR	90,000 ohm
Temperature range	–40°C to +85°C
Size (L x W x H, mm)	1.6 x 1.0 x 0.50

Note:

To ensure system stability and low power consumption, load capacitance of the 32.768 kHz crystal oscillator shall be within the range from 6 pF to 9 pF.

3.1.3 RF

3.1.3.1 Introduction

Figure 3-5 shows the functional block diagram of a GR5526 transceiver.

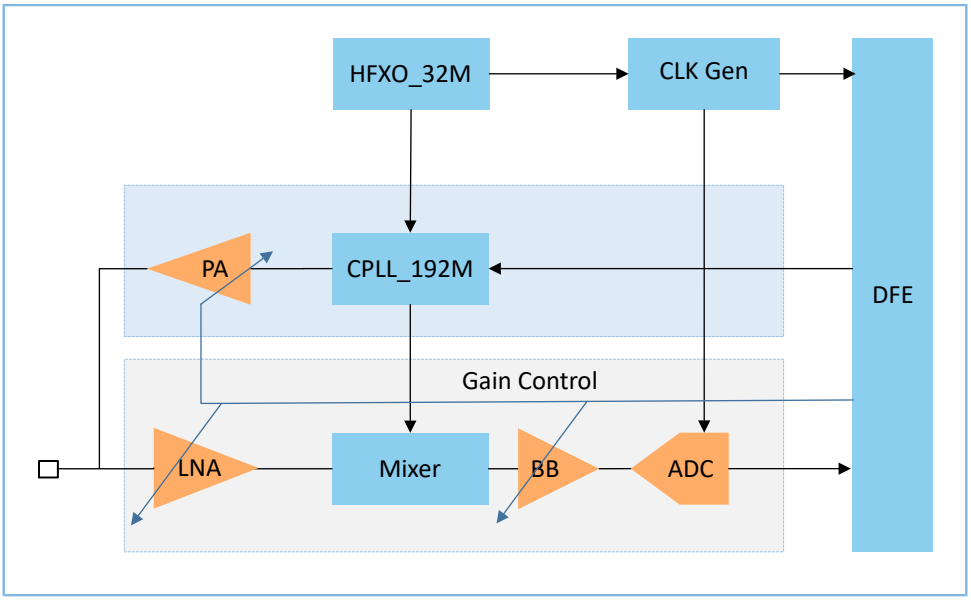

Figure 3-5 GR5526 transceiver architecture

Operating mechanisms:

- On the receiver side:
  1. After the antenna receives an RF signal, the receiver digitizes the signal in a path: Low noise amplifier (LNA) > Mixer > Baseband (BB) amplifier > an analog-to-digital converter (ADC).
  2. The digitized signals are sent to the digital frontend (DFE) for demodulation.
  3. The digital frontend provides Automatic Gain Control (AGC) feedback signals to adjust the gain of the LNA and BB amplifier to maximize the signal-to-noise ratio (SNR) at the demodulation.
- On the transmitter side:
  1. The digital signal from the DFE is transmitted to an SX PLL phase-locked loop (CPLL_192M) for modulation.
  2. The modulated carrier wave is delivered to a power amplifier (PA) with amplification factor configurable by the digital gain settings.
  3. The modulated carrier is transmitted to the antenna through a low-power or high-power PA path. The antenna radiates the amplified carrier wave through electromagnetic waves.

Note:

RF and digital clocks are generated from the HFXO_32M.

3.1.3.2 RF Scheme

The following figure is the recommended RF matching circuit in the GR5526 SoC minimal system.

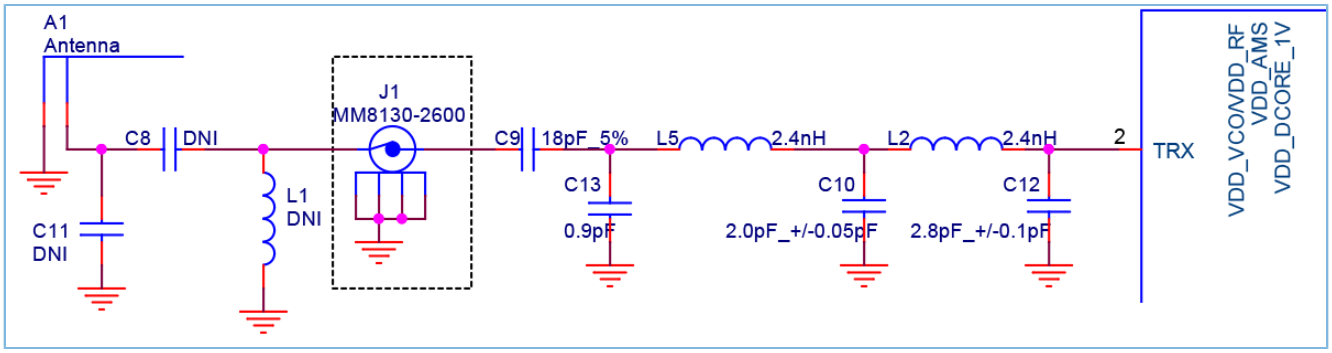

Figure 3-6 RF scheme

In the circuit, the left PI matching network (composed of the inductor L1 plus capacitors C8 and C11) matches the antenna; C9 is a DC blocking capacitor; the right PI type matching network (composed of the inductor L2 and L5 plus capacitors C10, C12 and C13) matches the internal PA of GR5526. The network connects to the TRX pin of the chip.

Recommended configurations of capacitors C9, C10, C12, C13, and the inductor L2, L5 are displayed in Table 3-8.

Table 3-8 Recommended components for the RF section

Reference	Description	Value	Package Size	Mfg Part #
C9	CAP, CER, 18 pF, ±2%, NPO, 0201, 50 V, -55°C to +125°C	18 pF	0201	Murata GRM0335C1H180GA01
C10	CAP, CER, 2.0 pF, +/-0.1 pF, NPO, 0201, 50 V, -55°C to +125°C	2.0 pF	0201	Murata GRM0335C1H2R0WA01D
C12	CAP, CER, 2.8 pF, +/-0.1pF, NPO, 0201, 50 V, -55°C to +125°C	2.8 pF	0201	Murata GRM0335C1H2R8BA01D
C13	CAP, CER, 0.9 pF, ±0.05 pF, NPO, 0201, 50 V, -55°C to +125°C	0.9 pF	0201	Murata GRM0335C1ER90WA01D
L2, L5	Inductors, Wirewound, 2.4 nH, +/-0.1 nH, 50 mohm, Q = 20@250 MHz, -55°C to +125°C, 0201	2.4 nH	0201	Murata LQP03TG2N4B02

3.1.4 I/O Pins

The GR5526 has software-configurable I/O pin assignment where different peripherals can be multiplexed out on different chip pins. When configured to GPIOs, they can be set as input, output, with configurable pull-up or pull-down resistors. I/O pins retain their last state when system enters the sleep or deep sleep mode, except GPIO_10 – GPIO_25, GPIO_32, and GPIO_33. Only AON_GPIOs can be used to wake up the system from sleep/deep sleep mode.

Note:

- For more details of pin mux, refer to *GR5526 Datasheet*.
- Note that MSIO pins do not support hardware interrupt when allocating I/O functions during designing PCB applications.
- Two PWM modules (PWM0 and PWM1) are provided, with each containing three separate output channels: PWMA, PWMB, and PWMC. Frequencies of the three PWM channels in one group are the same, and individual frequency control is not supported. Phase and duty cycle of each channel can be configured via registers.
- Recommended I/O connections for peripherals involving three QSPI channels: For SoCs supporting both GPU and DC (such as GR5526RGNIP and GR5526VGBIP), connect the display to QSPI M2. For scenarios involving QSPI Flash, QSPI PSRAM, and QSPI LCD, connect QSPI M0 to the Flash, QSPI M1 to the PSRAM, and QSPI M2 to the display.
- GPIO_10–GPIO_25, GPIO_32, and GPIO_33 cannot be used for output during sleep. In this case, the GPIOs remain in high impedance and can be pulled up or pulled down.

3.1.5 SWD Interfaces

GR5526 connects to J-Link for modulation by using Serial Wire Debug (SWD) interfaces.

Table 3-9 shows the pins to which the SWD interfaces connect in QFN and BGA packages.

Table 3-9 Pin matching for SWCLK and SWDIO in QFN and BGA packages

SWD	Pin # (BGA83)	Pin # (QFN68)
SWCLK	Pin D3	Pin 4
SWDIO	Pin E3	Pin 5

The pins can be multiplexed as GPIOs when the SWD interfaces are not in use.

3.2 PCB Design and Layout Guideline

3.2.1 PCB Layer Stackup

A 6-layer PCB layout is recommended for GR5526 BGA83 package. A recommended layer stackup (thickness: 1.6 mm) is shown below.

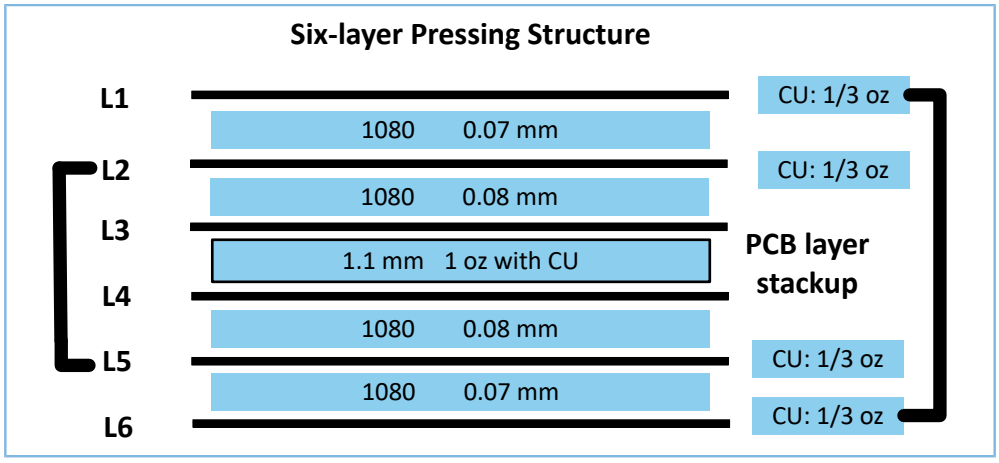

Figure 3-7 GR5526 PCB layer stackup (BGA83 package)

L1: top layer, where components, RF transmission lines, and key signal lines are placed

L2: internal ground plane layer, used for both the ground return path and the reference plane for the 50 ohm RF transmission line, as well as a small number of signal lines

L3: internal routing layer, where a large number of signal lines are placed

L4: internal routing layer for signal lines and power lines

L5: internal ground plane layer, used for ground return path signal lines

L6: bottom layer where components and signal lines are placed

A 4-layer PCB layout is recommended for GR5526 QFN68 package. A recommended layer stackup (thickness: 1.6 mm) is shown below.

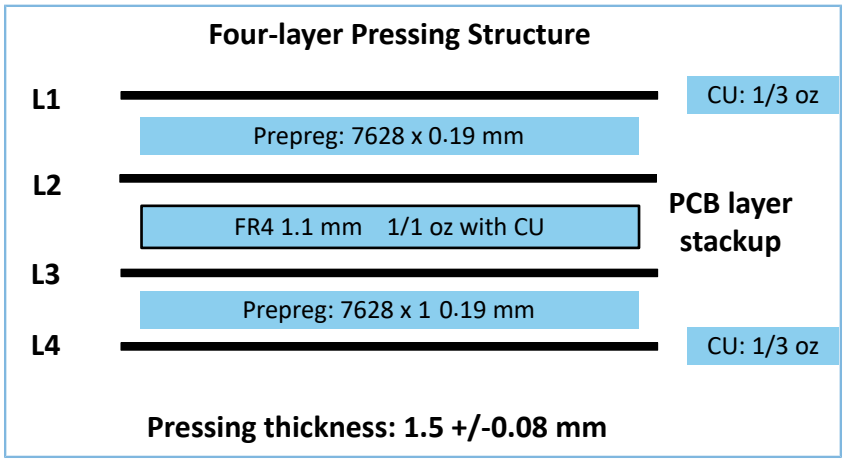

Figure 3-8 GR5526 PCB layer stackup (QFN68 package)

L1: top layer where components, RF transmission lines, and key signal lines are placed

L2: internal ground plane layer, used for both the ground return path and the reference plane for the 50 ohm RF transmission line

L3: internal routing layer, used to split power domains and place a small number of signal lines

L4: bottom layer where components and signal lines are placed

3.2.2 Components Layout

All components operating at high frequency should have their layout made as compact as possible. This will prevent the cross-coupling between lines and also minimize the parasitic effects which will have a negative impact on the operating parameters.

When designing the layout, make sure the main chip is as close to the antenna interface as possible, and no other components are under the RF routing if possible (the layout and routing of RF components are of higher priority).

3.2.3 Power Supply

Power supply is essential to ensure proper operation of an SoC, and therefore special attention should be paid on the layout and routing of the key power systems, which are DC-DC switching regulator and RF input power supply. To avoid system-level issues (such as poor performance in ESD protection and radiation off limits) caused by improper power design, abide by the design guides described in the two following sections.

3.2.3.1 DC-DC Switching Regulator

Take BGA83 for example. The chip includes a DC-DC switching regulator. To design the PCB layout involving a DC-DC switching regulator,

1. Components (L3: 9.1 nH inductor, L4: 2.2 µH inductor, and C17: 2.2 µF capacitor) connected to DC-DC switching regulator should be placed as close to VSW and VREG of the chip as possible. A distance within 3 mm is recommended.
2. The net of VSW radiates stronger interference before VSW signals passing through the inductors, and thus should be placed at a minimum distance of 0.2 mm from other power nets and signals, especially V1P0 and DIGCORE.
3. Placing L4 perpendicular to L3 is recommended, to avoid inductive coupling. C17 should be placed behind L4, and VREG network is connected to the power supply after capacitor filtering.
4. GND pin of C17 should be placed as close to VSS_BUCK of the chip as possible. Vias of C17 GND pin should be placed as close to the GND pin as possible. It is recommended to connect the C17 GND pin to VSS_BUCK by using GND Polygon Plane, so that the return path of the power can be kept minimal.

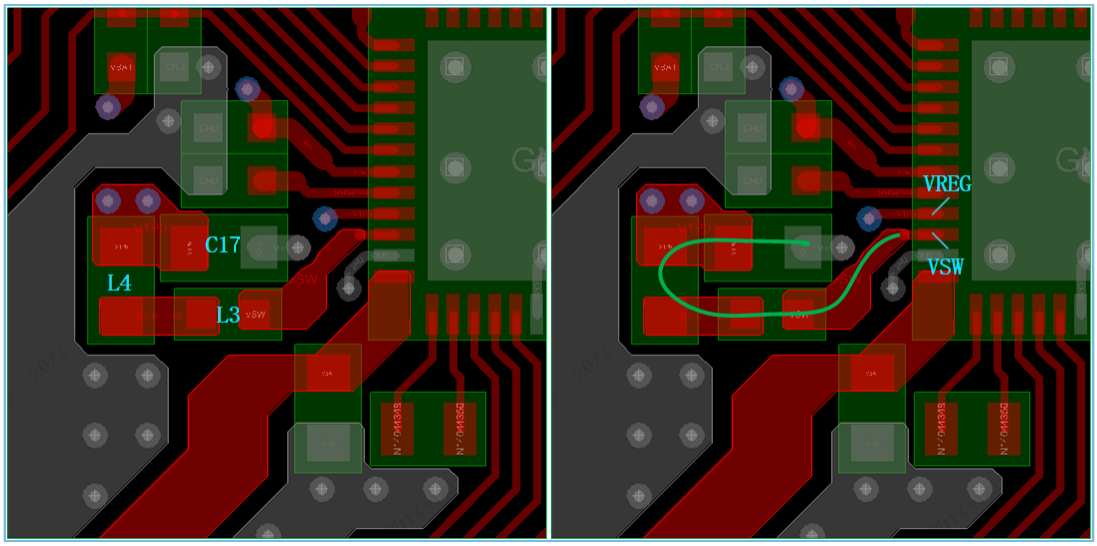

Figure 3-9 Reference layout and routing for DC-DC switching regulator

Note:

The green line in the right figure of Figure 3-9 indicates the power output path.

3.2.3.2 RF Input Power Supply

Make sure the following instructions are met when designing RF input power supply in PCB layout, to ensure optimal performance and to avoid excessively high radiation.

1. Decoupling capacitors (highlighted in yellow rectangles in Figure 3-10) connected to VDD_RF, VDD_VCO, and VDD_AMS should be as close to the corresponding pin as possible (around 1 mm is recommended, and shall not exceed 3 mm). Place the capacitors on the same layer with the pins if possible, and make sure the wiring path goes through the capacitors first and then connected to the chip power pins. In case the capacitors are not placed on the same layer with the pins, the vias should be located close to the decoupling capacitors.
2. The power trace should be as short as possible, and at least 0.2 mm wide. A minimum distance at 0.2 mm from other signals should be guaranteed.

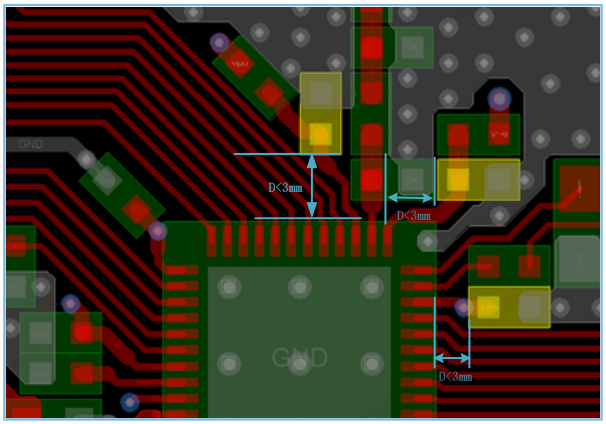

Figure 3-10 Reference layout and routing for RF input power supply

3.2.4 Clock

Place the crystal as close as possible to the IC (recommended distance: ≤4 mm). This will minimize any additional capacitive load on the input pins and reduce the chance of crosstalk and interference with other signals on the board. Make sure there is no other trace route next to/under the crystal or the crystal routes.

It is recommended to shield the routes of the 32 MHz crystal. If the ground below the crystal is clean and no crosstalk or interference is involved, provide openings on the pad underneath the crystal (as shown in Figure 3-12), which helps to reduce parasitic capacitance.

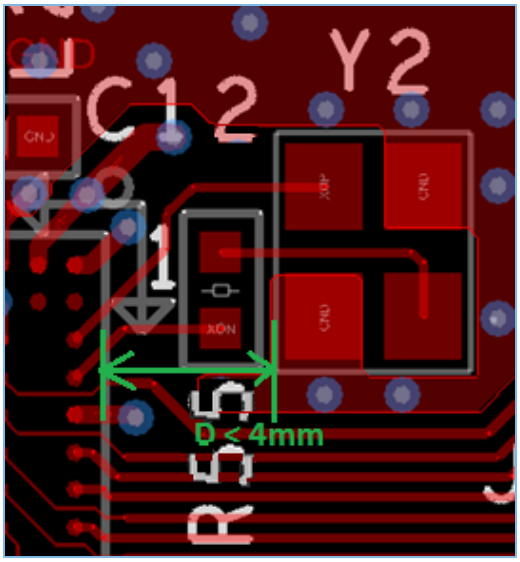

Figure 3-11 Clock PCB Ref of BGA83 (reference)

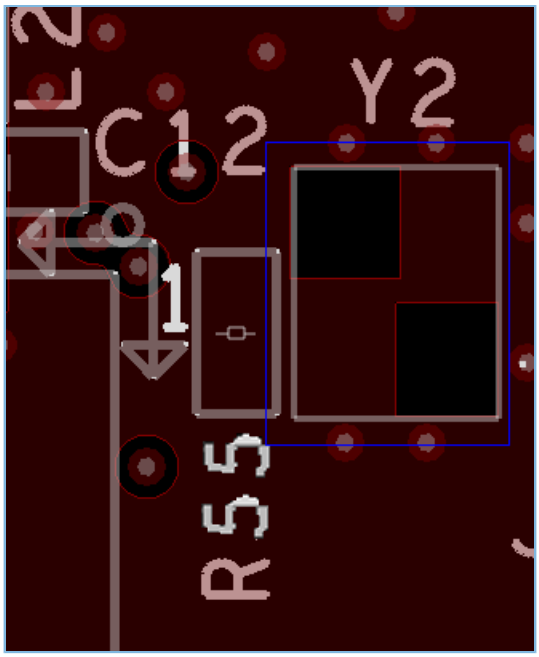

Figure 3-12 Openings on PCB pad for clock crystal of BGA83

3.2.5 RFIO Port

The GR5526 provides a single-ended RFIO port. A copper RFIO trace with a characteristic impedance of 50 Ω interconnects the RF port and the antenna. Because the impedance of RFIO port is not 50 Ω, a matching network is required to match the port impedance between the RF port and the 50 Ω transmission line.

Components in this network must be placed as close as possible to the RFIO pin. Try to place the first component no further than 1 mm from the RFIO pin. Figure 3-13 shows the PCB layout of the RF port.

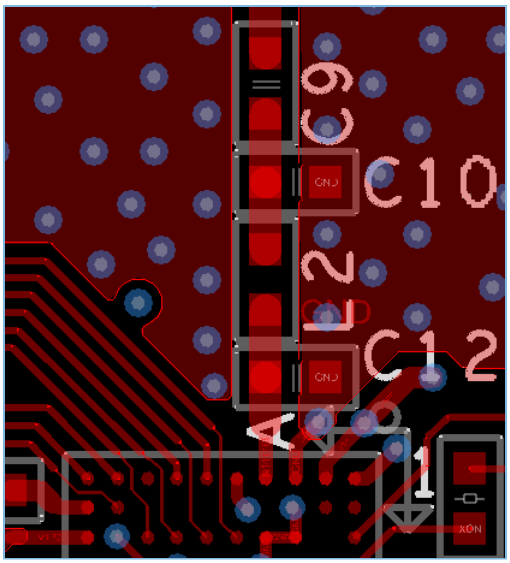

Figure 3-13 GR5526 routing on a PCB

Note:

The RF route should be straight and as short as possible. If a curving route is necessary for a specific structure, an inverted arc is required for a turning, and angles at or less than 90◦ are not allowed.

RF routing at the PCB surface (the top layer or the bottom layer) helps avoid using vias or switching layers, and is therefore preferred. Stub routes should be avoided, and the reference ground plane underneath the RF route shall be complete. The RF route shall be of the same width as the component pad. This ensures there will not be discontinuities in the 50 Ω transmission line due to a mismatch between the component pad size and trace size.

Taking the 4-layer PCB layout design as an example, the transmission line is routed as a coplanar waveguide using layer-2 ground as the reference plane. The dimensions are:

- Trace width: 559 µm
- Spacing from trace to top layer: 178 µm
- Spacing from top layer to layer 2: 432 µm

The design uses FR-4 dielectric and 0.5 ounce copper on the outer layer. In actual design, PCB manufacturers are required to provide single-ended RFIO traces with an impedance of 50 Ω (+/–10%).

Ground vias should be placed along the transmission line every 1.25 mm and right next to the ground pads of the matching components.

A PI-network should be placed close to the antenna feedpoint for antenna matching purposes. The matching network value of antenna is adjusted according to the actual antenna used. It is recommended to use mature antenna schemes and recommended values of antenna factories.

3.2.6 Grounding

Always provide a solid grounding for the radio IC of GR5526. Use as many vias as possible to create a solid GND under the IC itself and connect it to inner and bottom GND layers.

For the center ground paddle (at the package bottom) of QFN packages, use a matrix of 3 x 3, 4 x 4, or other vias to the ground-plane.

The GND of the 10 µF filter capacitor connecting to VBATL shall be close to the main GND pin, and apply copper pouring if possible (see "Section 3.2.3 Power Supply"). The ground return path of the GND pin (VSS_BUCK) of DC-DC power shall be in good condition, which guarantees stable and secure operation of ICs.

QSPI peripherals running at a high-speed clock, such as QSPI PSRAM, will encounter ground noise interference during toggling of I/O data pins, resulting in RF performance degradation. Therefore, it is of critical importance to properly ground these peripherals. Follow the rules below:

- The reference planes for all signals (SO0–SO3, CLK, and CS) shall be continuous and complete.

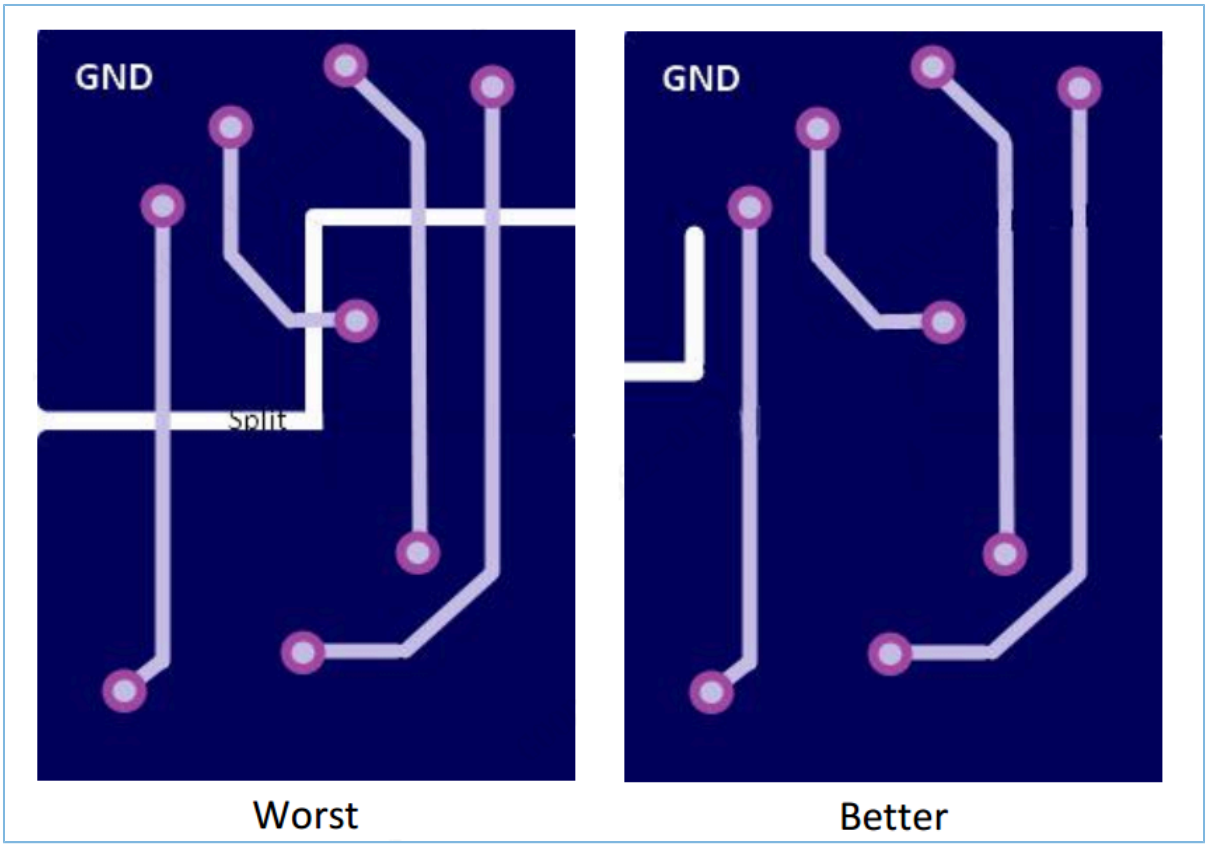

Figure 3-14 The worst and better ground routing

- Connect the QSPI GND to the decoupling capacitor GND to prevent noise from being coupled into the system.

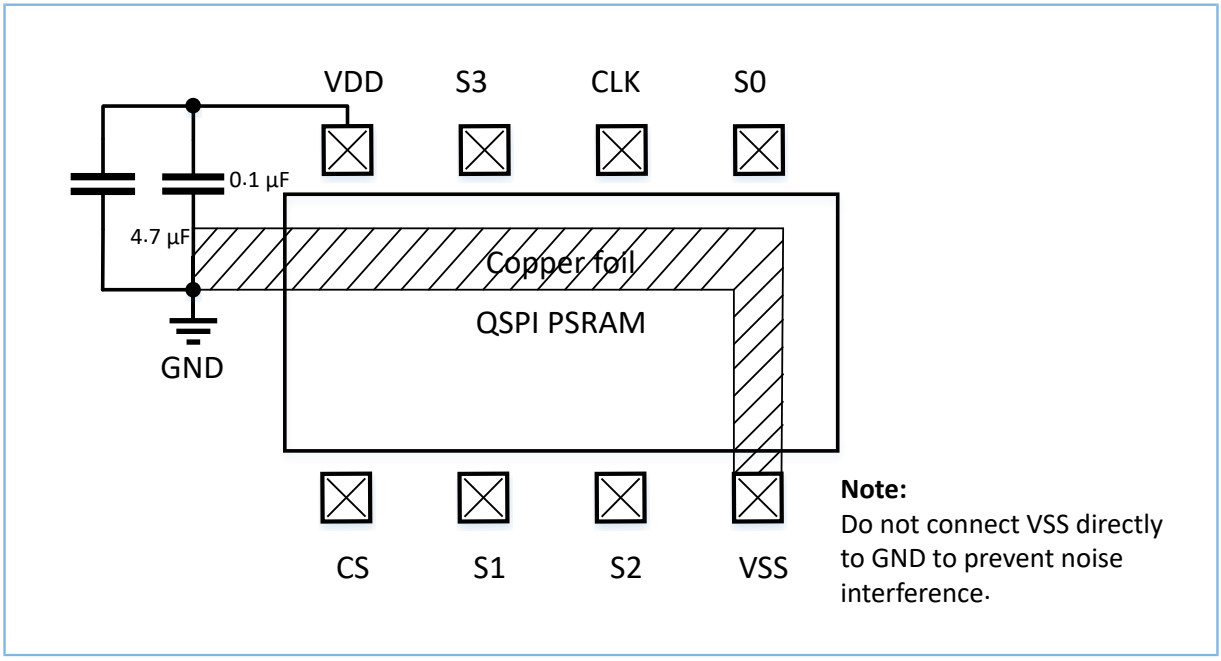

Figure 3-15 Connecting the QSPI GND to the decoupling capacitor GND

Note:

- Make sure the ground-pad shape follows the shape of the paddle on chip, including the exposed paddle parts (for QFN package).
- Make sure a ground via is placed right next to the TRX pin.
- For the BGA package, place ground vias as close as possible to the ground balls.

3.2.7 ESD Protection Design

3.2.7.1 System-level ESD Design

System efficient electrostatic discharge (ESD) design is crucial for any circuits, and requires users to follow the design guidelines (including schematic diagrams, PCB layout, and product structural designs) provided in the sections below.

3.2.7.1.1 ESD Schematic Design

1. GR5526 series is powered by an independent external LDO regulator (see “Section 3.1.1 Power Supply” for details).
2. To suppress static voltages, connect a ferrite bead to each of the two charging pads (CHAR+ and CHAR-) in series, and apply a proper transient voltage suppressor (TVS) diode at each ferrite bead to found the basis of the ESD protection scheme, as shown in the figure below.

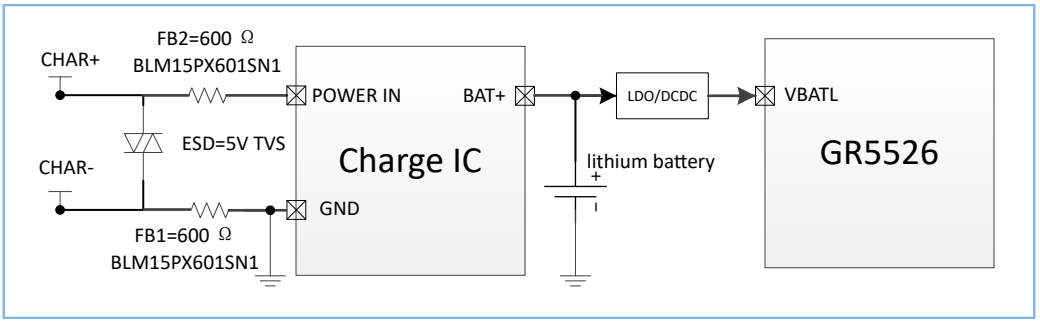

Figure 3-16 ESD protection scheme at charging pads

Recommended models of TVS diodes and ferrite beads, as well as model selection requirements, are listed in the tables below.

Table 3-10 Model selection for TVS diodes

Parameters	Description	Min.	Typ.	Max.
V_{RwM} (V)	Reverse working maximum voltage	-	5 V	-
V_{BR} (V)	Breakdown voltage	-	7 V	-
V_{clamp} (V)	Clamp voltage	-	6 V	-
V_{ESD} (kV)	ESD prevention performance	• Contact discharge: ±10 kV • Air discharge: ±12 kV	-	-

Table 3-11 Model selection for ferrite beads

Parameters	Description	Min.	Typ.	Max.
Impedance@100 MHz (Ω)	Impedance @ 100 MHz	-	600 Ω	-
I_R (mA)	Rated operating current	-	900 mA	-
R_{DC} Max. (mΩ)	Maximum DC resistance	-	230 mΩ	-

Table 3-12 Recommended TVS diodes

Part Number	V_{RwM} (V)	V_{BR} (V)	V_{clamp} (V)	Operating Temperature	V_{ESD} (kV)	Package	Manufacturer
AZ5C25-01B	5	9	6	–55°C – 85°C	• Contact discharge: ±13 kV • Air discharge: ±16 kV	0201	Amazing Micro.
OVE38E32S1M	6.5	7	10	–55°C – 85°C	• Contact discharge: ±25 kV • Air discharge: ±25 kV	0402	OVREG

Table 3-13 Recommended ferrite beads

Part Number	Impedance @100 MHz	Rated Current	Max. DC Resistance	Operating Temperature	Package	Manufacturer
BLM15PX601SN1	600 Ω	900 mA	230 mΩ	-55°C – 125°C	0402	Murata
WLBD1005HCU601TL	600 Ω	900 mA	230 mΩ	-55°C – 125°C	0402	Walsin

3. To protect products with metal shell against ESD, connect ferrite beads between metal shell GND and the GND on motherboard.

3.2.7.1.2 PCB Layout Design

1. Live by the following rules for GR5526 PCB grounding:
   - PCB with six layers or above is recommended for SoCs in BGA83 package, whereas PCB with four layers or above is recommended for SoCs in QFN68 package. A GR5526 SoC is adjacent to the GND layer. The GND layer shall be solid and complete, so as to effectively prevent static from setting in.
   - Connect GR5526 GND pin to the GND pin on the top layer, and then connect the GR5526 SoC GND pin to the GND pins on the other layers through vias.
   - For GR5526 in QFN package, VSS_BUCK shall be placed close to the GND pin of the input capacitor (10 µF), and be connected to EPAD on other layers through at least two vias near VSS_BUCK. The trace from VSS_BUCK to the input capacitor should be 0.25 mm wide or above, so as to reduce power/GND loop impedance.
2. To design the layout for charging pads,
   - It is recommended not to place pads of charging pads (CHAR+ and CHAR-) and GR5526 SoC on the same layer. However, if the pads and GR5526 SoC are on the same layer, the spacing between the charging pads (CHAR+ and CHAR-) and GR5526 SoC should be greater than 4 mm (for BGA83 package, the spacing needs to be greater than 8 mm), and the farther the better.

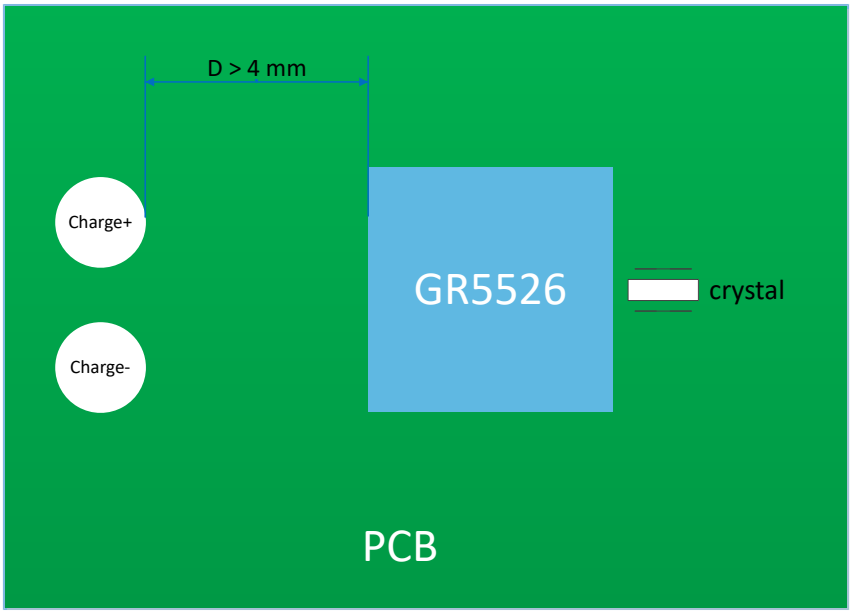

Figure 3-17 Design of charging pads

- Pads of the charging pads shall not be placed close to ESD-sensitive signals (including clock, reset, and communication signals), the crystal oscillator, or VDD_AMS pin, especially in BGA83 package. Those signals shall also be shielded with ground traces.

3. Place filter capacitors as close to the power pins of GR5526 as possible, to keep the power return path minimal, so as to enhance filtering performance.

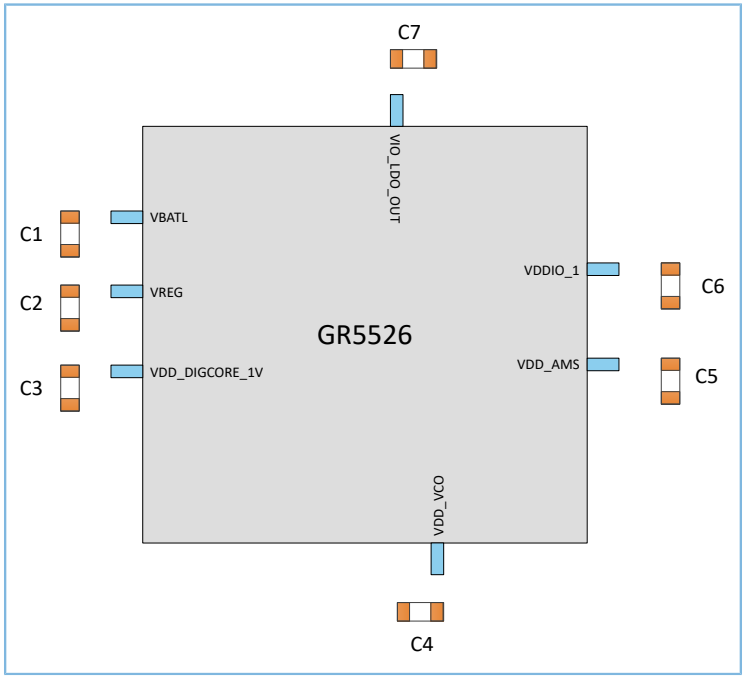

Figure 3-18 Filter capacitor layout for power supply

4. It is recommended to place communication signals neither on the top layer nor the bottom layer in the PCB stack-up, due to the ESD susceptibility of I/O pins. Avoid routing signals susceptible to ESD events (such as clocks and reset pins) at the edge of the board. It is recommended to shield the I/O pins and ESD susceptible signals with GND traces.

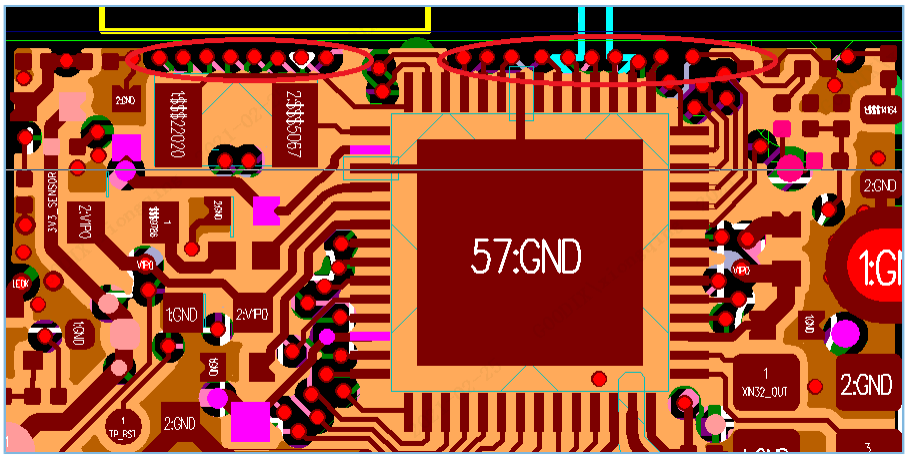

Figure 3-19 Improper I/O routing at board edge (not shielded by GND traces)

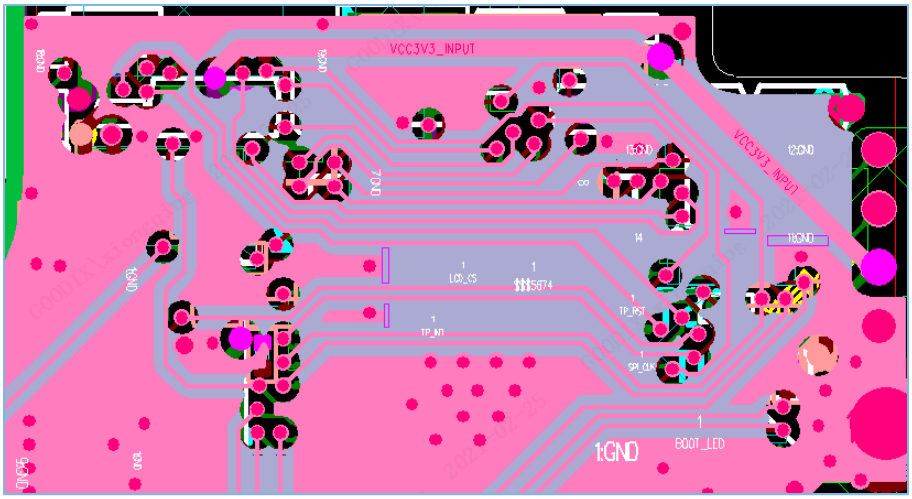

Figure 3-20 Proper routing of I/O pins

5. The capacitors or ESD protection devices should be routed through the pad. Using long wires to connect the capacitors/ESD protection devices to pad undermines filtering/protection performance, and is therefore not recommended.

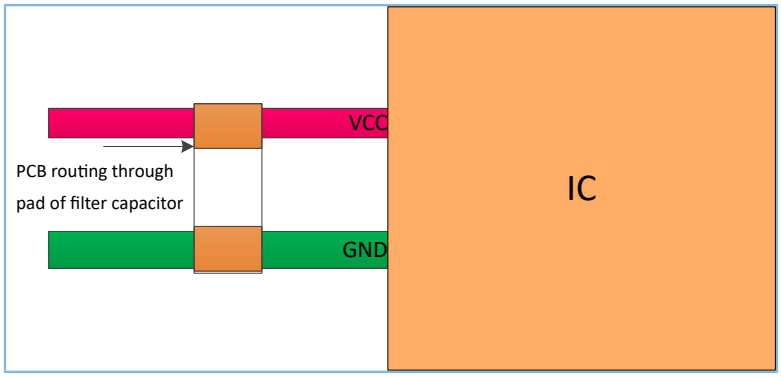

Figure 3-21 Proper routing for a capacitor (as an example)

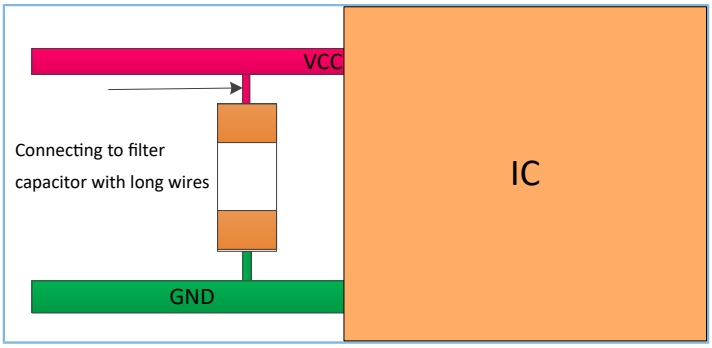

Figure 3-22 Improper routing for a capacitor (as an example)

3.2.7.1.3 Product Structural Design

- Shell gaps shall be sealed to prevent static electricity from setting in.
- Connect ferrite beads in series to the GND pins on the metal shell, and connect the GND pins to the GND circuit on the motherboard, to protect the motherboard from static electricity transmitted through the metal shell.
- Suspended metal structure is not allowed. The steel stiffener of sensors (such as touch/display sensors) shall be grounded.
- Try to avoid close contact with the overlapped area between the FPC on the motherboard and the FPC on touch/display sensor module. It is recommended to apply heat resistant adhesives on the exposed area of motherboard connectors, to prevent short circuit or static electricity from setting in.
- Use ESD protections (such as TVS diodes) for exposed pins such as I/Os and RF.

3.2.7.2 ESD Considerations in Production, Transport, and Debugging

To steer away from ESD events, stringent ESD control is also required during production, transport, debugging, and other relevant phases.

- Wear antistatic wrist strap in these processes. Touching the SoC with bare hands or using metal tweezers is forbidden.
- Use an antistatic bag/tray to hold the SoC.

- Countermeasures against ESD are essential for soldering irons, welding tables, and test instruments.
- Strictly comply with ESD preventive requirements for the production line during production and transport.

4 Reference Design

4.1 Reference Schematic Diagram

The figure below is the reference schematic for GR5526VGBIP BGA83.

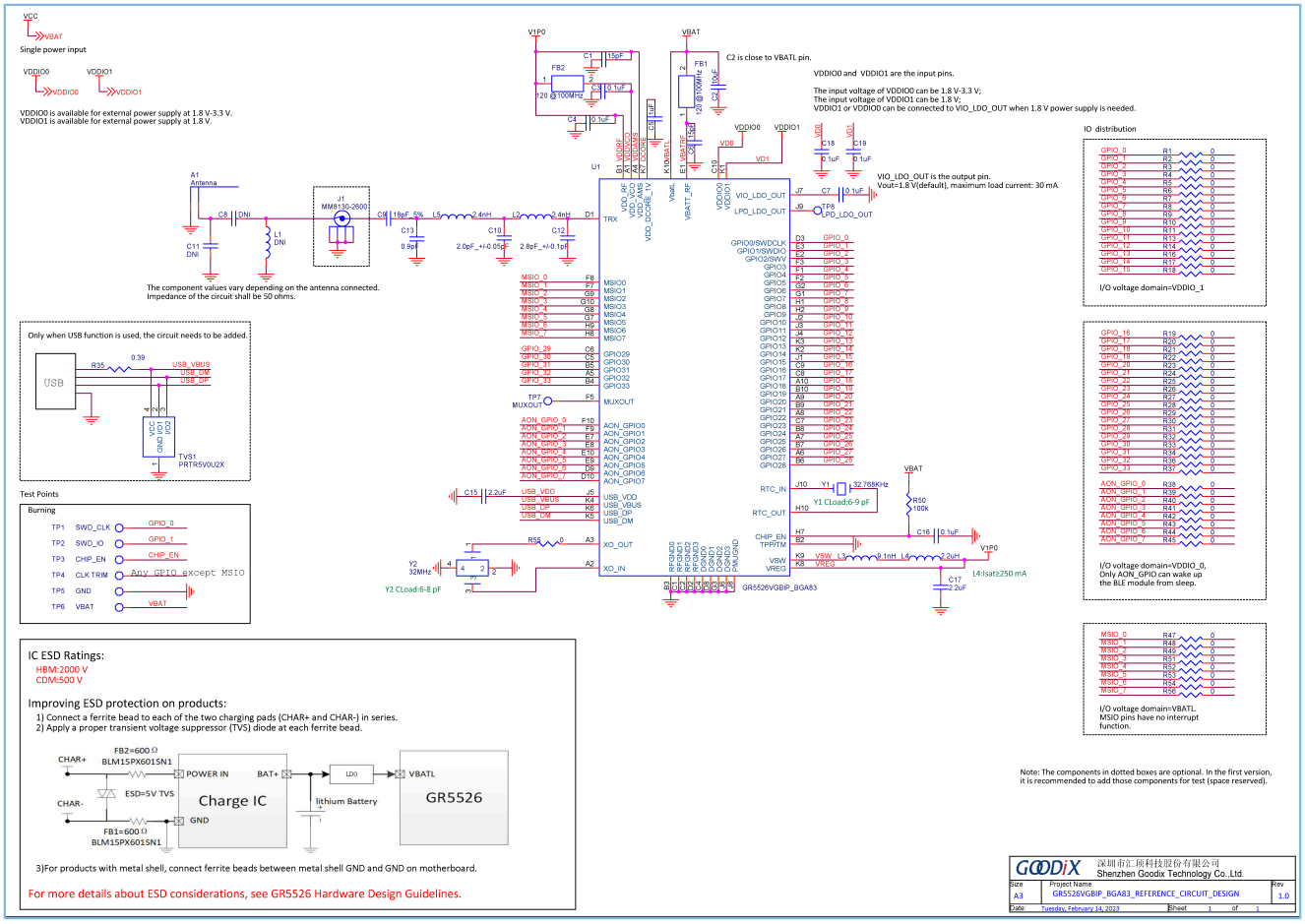

Figure 4-1 Reference schematic for GR5526VGBIP BGA83

The figure below is the reference schematic for GR5526VGBI BGA83.

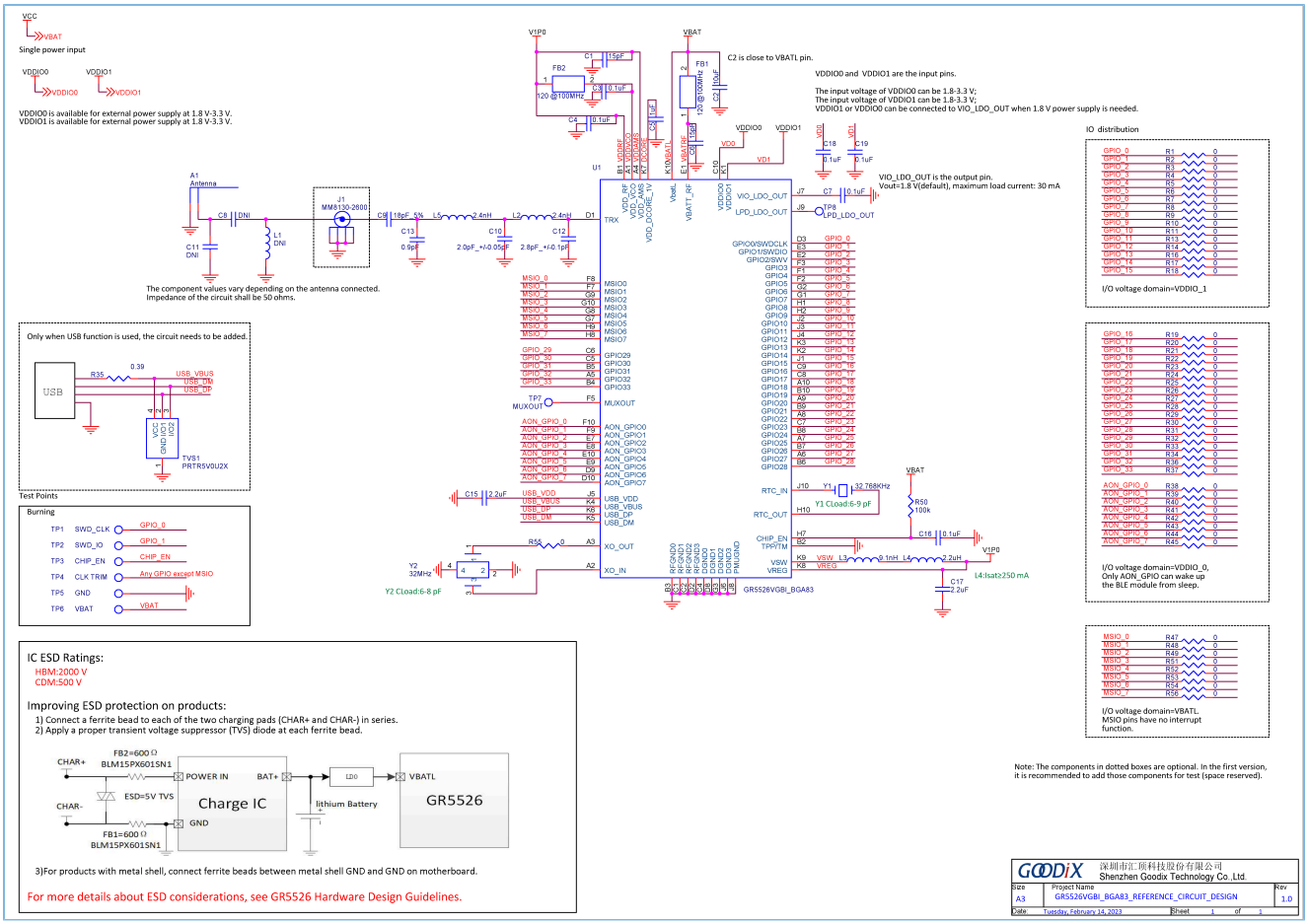

Figure 4-2 Reference schematic for GR5526VGBI BGA83

The figure below is the reference schematic for GR5526RGNIP QFN68.

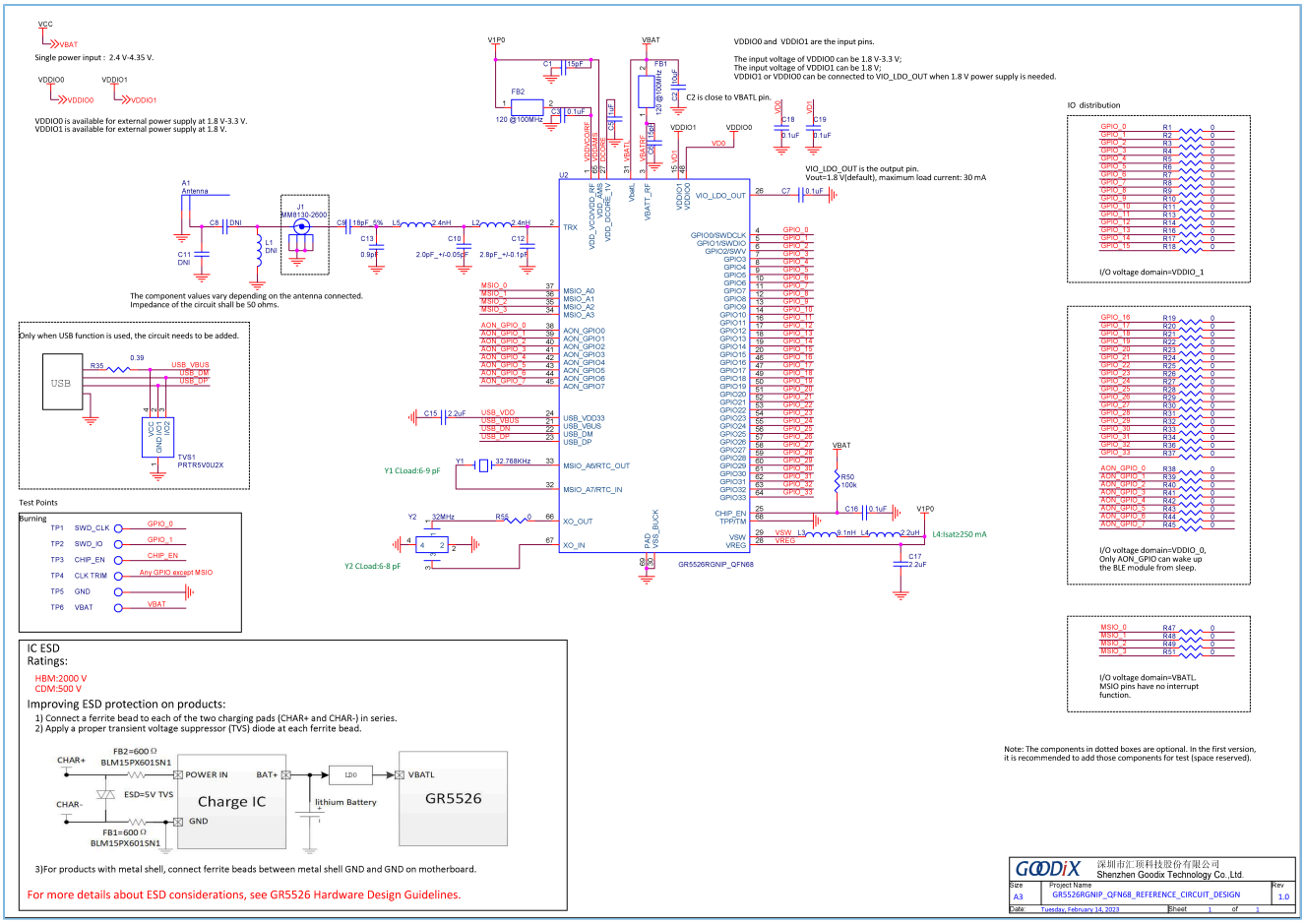

Figure 4-3 Reference schematic for GR5526RGNIP QFN68

The figure below is the reference schematic for GR5526RGNI QFN68.

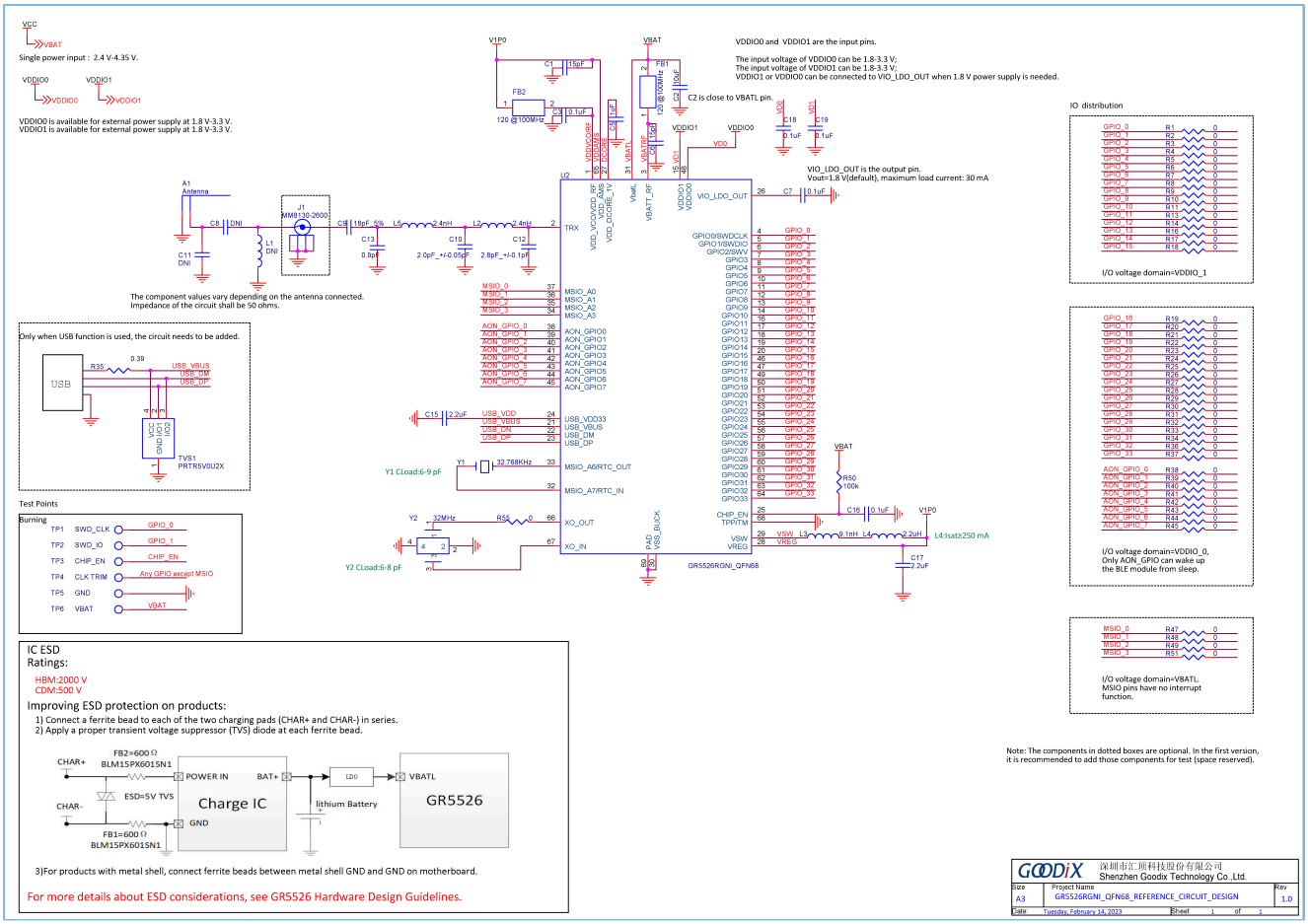

Figure 4-4 Reference schematic for GR5526RGNI QFN68

5 FAQ

5.1 Why Is the Power Consumption in GR5526 Sleep Modes High?

- Description

  In power consumption tests, the power consumption of GR5526 when in sleep mode varies depending on different I/O pin configurations. How to properly configure I/O pins before GR5526 goes to sleep?

- Issue Analysis

  The power consumption of GR5526 in sleep mode is high, and it may be because I/O pins are not properly configured.

  - I/O pins are at floating state.
  - I/O pins are configured in improper pull-up or pull-down state.

  Above incorrect configurations can cause system leakage, so you need to properly configure the state of I/Os before GR5526 enters sleep mode.

- Solution

  Configure the state of I/O pins before GR5526 enters sleep mode.

  - If an I/O pin is in pull-up/pull-down state or used as a driver output, it needs no pull-up/pull-down configuration.
  - If an I/O pin is not used or works in input mode without pull-up or pull-down, it needs to be configured to internal pull-down.

For sleep mode configurations, see *GR5526 Power Mode and Power Consumption Measurement Application Note*.

5.2 Can the RF PI Circuits Be Simplified or Removed?

- Description

  In designing a PCB, can I modify the recommended RF PI circuit layout due to limited space?

- Issue Analysis

  GR5526 recommends two PI circuits for RF: a PI circuit close to GR5526 and a PI circuit close to the antenna. Whether these two PI circuits can be simplified or removed needs to be treated differently.

- Solution

  The PI circuit close to GR5526 is used to match GR5526 internal PA and cannot be removed. It cannot be simplified also as its inductance and capacitance values must be kept consistent with the recommended circuit. The impedance of the RF channel from the GR5526 PI is 50 Ω and compatible with any 2.4 GHz antenna (2400 MHz to 2484 MHz) that supports Bluetooth products.

  The PI circuit close to the antenna end is used to match the antenna, and its circuit can be changed according to the antenna you use. For the matching of the antenna, you can complete simple matching adjustment by the S11 parameter or the Smith chart from the vector network analyzer. However, for matching of other indicators (such as antenna gain and directionality), you are recommended to seek help from professional antenna factories.

6 Glossary

Table 6-1 Glossary

Name	Description
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AMS	Analog Mix Signal
AoA	Angle of Arrival
AoD	Angle of Departure
BB	Baseband
BGA	Ball Grid Array Package
Bluetooth LE	Bluetooth Low Energy
BUCK	Type of DC-DC Converter
CPLL_192M	192 MHz Phase-Locked Loop
DC	Display Controller
DC-DC	DC-to-DC Converter
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
GPIO	General-purpose Input/Output
GPU	Graphics Processing Unit
LDO	Low-dropout
LNA	Low Noise Amplifier
MPU	Memory Protection Unit
NMI	Non-maskable Interrupt
PCB	Printed Circuit Board
PMU	Power Management Unit
PSM	Pulse Skip Mode
PSRAM	Pseudostatic RAM
QFN	Quad Flat No-Lead Package
QSPI	Queued Serial Peripheral Interface
RoHS	Restriction of Hazardous Substances Directive
SiP	System-in-Package
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SVHC	Substance of Very High Concern

Name	Description
SWD	Serial Wire Debug
SWO	Serial Wire Output
Tg	Glass Transition Temperature
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
HFXO_32M	External 32 MHz Crystal Oscillator

7 Appendix: QFN and BGA Assembly Guideline

The QFN and BGA packages are qualified to MSL 3 and are RoHS/green compliant. RoHS is the abbreviation of *Restriction of Hazardous Substances Directive*, which puts a limit on the amount of harmful substances in electronic devices, published by European Union in February 2003. MSL 3 represents Moisture Sensitivity Level 3 which indicates that a moisture sensitive plastic device, once removed from a dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH before the solder reflow process.

GR5526 storage conditions:

- Temperature: < 40°C
- Humidity: < 90% RH
- Period: 12 months

After opening the package: go through reflow for board assembly within 48 hours.

- Temperature: < 30°C
- Humidity: < 60% RH
- Stored at: < 10% RH

In BGA83 package outlines, both lead-free solder and Sn/Pb solder applications use the same rules for the general PCB design. Only the board surface finish and the board material have to be considered for lead-free application due to the higher reflow temperature and lead-free solder compatibility. A number of factors may have a significant effect on mounting QFN or BGA packages on the board and the quality of solder joints. Some of these factors include amount of solder paste coverage in exposed ground/thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow temperature profile.

Note:

It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort may be needed to optimize the process as per users' surface mount practices and requirements.

In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

Typically, the PCB pad pattern for an existing package is designed based on guidelines developed within a company or by following industry standards such as IPC-SM-782. For the purpose of this document, methodology of Association Connecting Electronics Industries (IPC) is used here for designing PCB pad pattern. However, because of exposed die paddle and the package lands on the bottom side of the package of GR5526, certain constraints are added to IPC's methodology. The pad pattern developed here includes considerations for lead and package tolerances.

7.1 Package Information

GR5526 offers BGA83 and QFN68 packages to support different environmental requirements.

7.1.1 BGA83

GR5526 BGA83, including GR5526VGBIP BGA83 and GR5526VGBI BGA83, is an 83-pin and 4.3 x 4.3 x 0.96 (mm) package. It is qualified to MSL 3.

Table 7-1 BGA83 package information

Parameter	Value	Unit	Tolerance
Package Size	4.3 x 4.3	mm	±0.1 mm
BGA Ball Count	83		
Total Thickness	0.96	mm	±0.1 mm
BGA Ball Pitch	0.40		
Ball Diameter	0.20		±0.05 mm
Ball Height	0.14		±0.05 mm

The figure below shows the BGA83 package outlines.

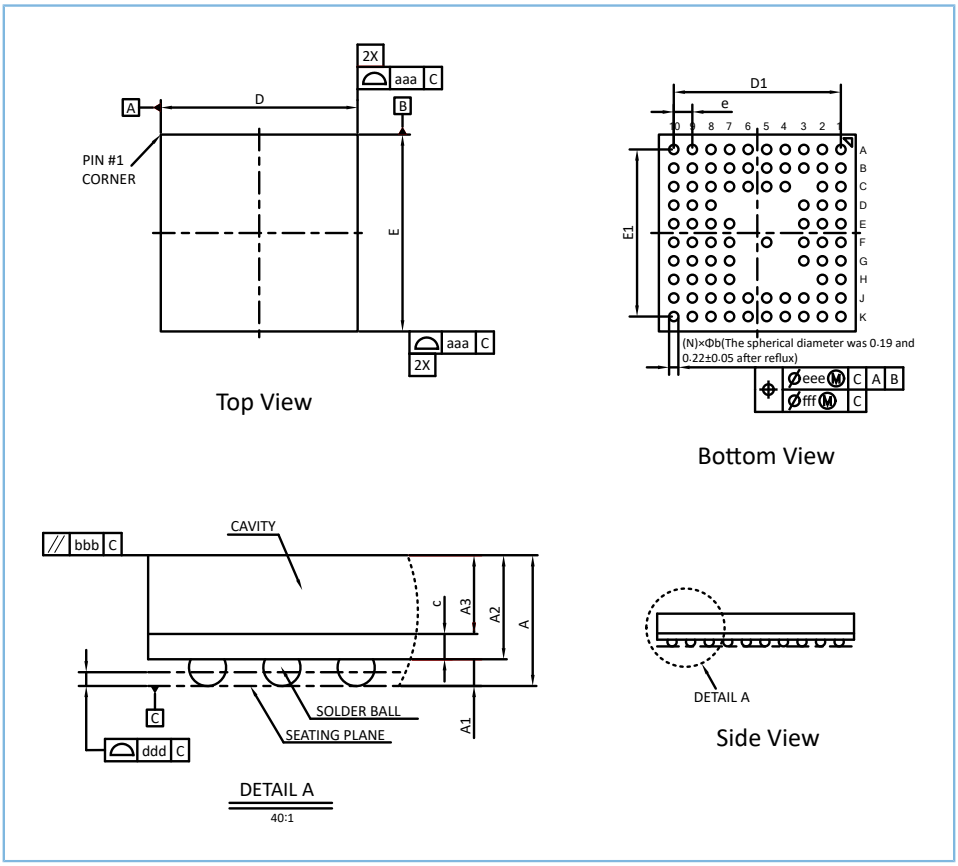

Figure 7-1 BGA83 package outlines

Note:

Drawing is not to scale.

Table 7-2 BGA83 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.860	0.960	1.060	0.034	0.038	0.042
A1	0.090	0.140	0.190	0.004	0.006	0.007
A2	0.770	0.820	0.870	0.030	0.032	0.034
A3	0.620	0.650	0.680	0.024	0.026	0.027
c	0.140	0.170	0.200	0.006	0.007	0.008
D	4.200	4.300	4.400	0.165	0.169	0.173
E	4.200	4.300	4.400	0.165	0.169	0.173
D1	-	3.600	-	-	0.142	-
E1	-	3.600	-	-	0.142	-
e	-	0.400	-	-	0.016	-
b	0.150	0.200	0.250	0.006	0.008	0.010
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

7.1.2 QFN68

GR5526 QFN68, including GR5526RGNIP QFN68 and GR5526RGNI QFN68, is a 68-pin and 7 x 7 x 0.85 (mm) package. It is qualified to MSL 3.

Table 7-3 QFN68 package information

Parameter	Value	Unit	Tolerance
Package Size	7.0 x 7.0	mm	±0.05 mm
QFN Pad Count	68		
Total Thickness	0.85	mm	±0.05 mm
QFN Pad Pitch	0.35		
Pad Width	0.15		±0.05 mm
Exposed Pad Size	5.49 x 5.49		±0.1 mm

The figure below shows the QFN68 package outlines.

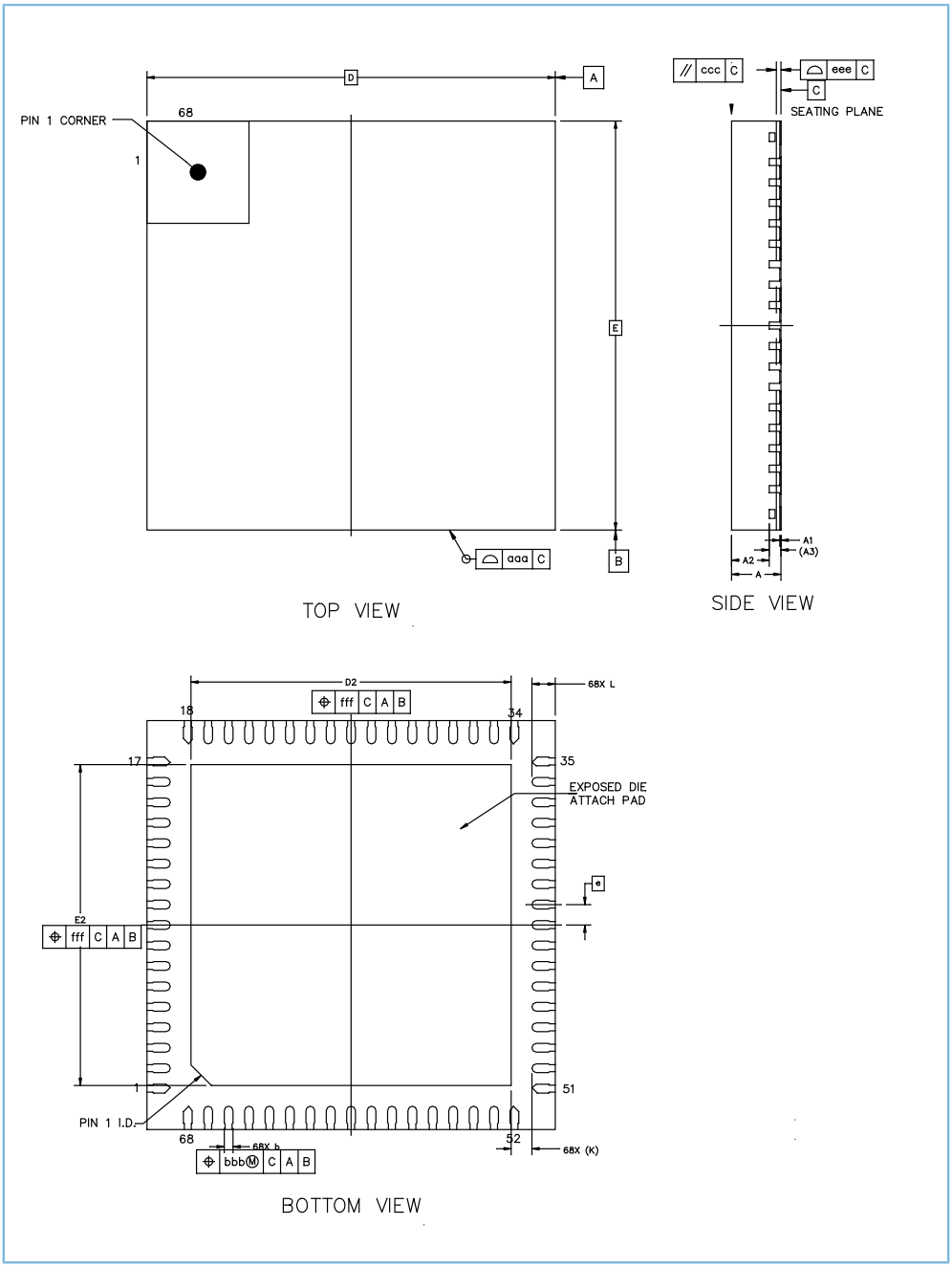

Figure 7-2 QFN68 package outlines

Note:

Drawing is not to scale.

Table 7-4 QFN68 package dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.800	0.850	0.900	0.031	0.033	0.035
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	-	0.650	-	-	0.026	-
A3	0.203 REF.			0.008 REF.		
b	0.100	0.150	0.200	0.004	0.006	0.008
D	7.000 BSC.			0.276 BSC.		
E	7.000 BSC.			0.276 BSC.		
e	0.350 BSC.			0.014 BSC.		
D2	5.390	5.490	5.590	0.212	0.216	0.220
E2	5.390	5.490	5.590	0.212	0.216	0.220
L	0.350	0.400	0.450	0.014	0.016	0.018
K	0.355 REF.			0.014 REF.		
aaa	0.100			0.004		
ccc	0.100			0.004		
eee	0.080			0.003		
bbb	0.070			0.003		
fff	0.100			0.004		

Note:

Values in inches are converted from values in millimeter and rounded to 3 decimal digits.

7.2 Board Mounting Guideline

Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for QFN and BGA packages. This is further complicated by the large grounding die pad underneath QFN package and the proximity to the inner edges of the leads.

Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Because surface mount process varies from company to company, careful process development is recommended.

7.2.1 Stencil Design for Perimeter Pads

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 mils to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement.

The first step in achieving reliable solder joints is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

- Area ratio = area of aperture opening/aperture wall area
- Aspect ratio = aperture width/stencil thickness

For rectangular aperture openings, as required for GR5526 packages, these ratios are given as:

- Area ratio = L x W/2T (L + W)
- Aspect ratio = W/T

L and W are the aperture length and width, and T is stencil thickness. For optimum paste release, the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release.

It is also recommended that the stencil aperture tolerances should be tightly controlled, as these tolerances can effectively reduce the aperture size. It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the center exposed pad region. See Figure 7-3 for reference solder mask design in the center of the package.

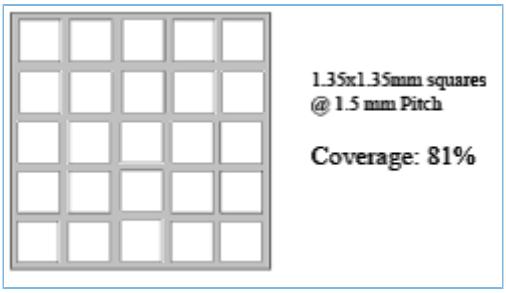

Figure 7-3 Exposed/Ground pad stencil design recommendation for QFN package

7.2.2 Via Types and Solder Voiding

Voids within solder joints under the exposed grounding pad can have an adverse effect on high-speed and RF applications. Voids within this ground plane can increase the current path of the circuit.

The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any one via would not be rendered ineffectual based on any one void increasing the current path beyond the distance to the next available via.

7.2.2.1 Stencil Thickness and Solder Paste

The stencil thickness of 0.125 mm is recommended for 0.35 mm pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 paste (IPC standard J-STD-005) be used for mounting QFN package. Nitrogen purge is also recommended during reflow.

The most common surface finishes that are compatible with lead-free surface mount technology (SMT) process are:

- Organic solderability preservatives (OSP)
- Electroless nickel/Immersion gold (ENIG)
- Immersion silver
- Immersion gold

Selection of a suitable finish will depend on end users' requirements for board design, assembly process, handling/ storage, and cost.

7.2.2.2 PCB Materials

Due to the higher reflow temperature requirement of the lead-free material set, the board material with higher glass transition temperature Tg (> 170°C) is recommended.

7.2.3 SMT Printing Process

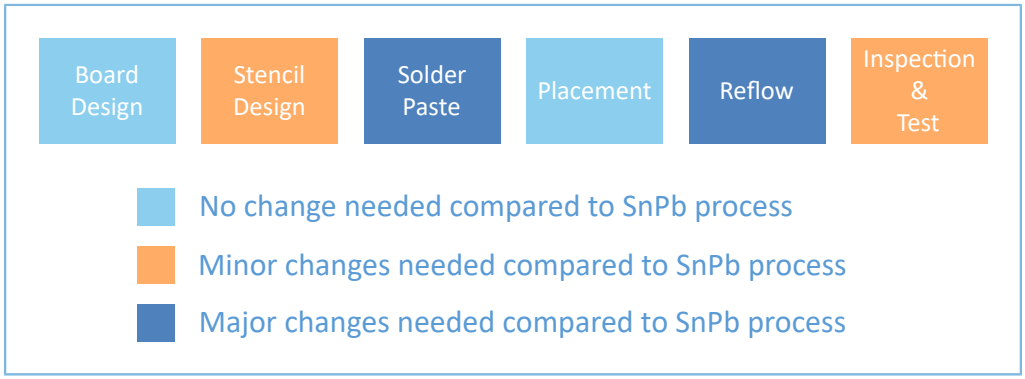

Figure 7-4 SMT printing process

- Solder Paste

  Sn-Ag-Cu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance.

- Stencil Design

  The recommended stencil is laser-cut, stainless-steel type with thickness of 5 to 7 mils and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 1 mil larger than the top can be utilized. Sn-Ag-Cu solder does not wet as well as Sn-Pb solder.

- Printing Process

  The printing process requires no significant changes, comparing with that applies Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste deposition.

- Placement

  With the self-aligning characteristic of the QFN packages during reflow, the placement accuracy is < 30% of the pad width or as long as the solder pads can touch solder paste.

7.3 SMT Reflow Process

The optimization of the reflow process is the most critical factor to be considered for the lead-free soldering. The development of an optimal profile should take into account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensure successful lead-free assembly, high yield and long-term solder joint reliability.

1. Temperature Profiling

   Temperature profiling should be performed for all new board designs by attaching thermocouples at the solder joints of QFN and BGA package, on the top surface of the larger components as well as at multiple locations of the boards. This is to ensure that all components are heated to temperature above the minimum reflow temperatures and the smaller components do not exceed maximum temperature limit.

   For larger or sophisticated boards with a large number of components, it is also important to minimize the temperature difference across the board to be less than 10 degrees to minimize board warp. Maximum temperature at component body should not exceed the MSL 3 qualification specification.

2. Reflow Profile Guideline

   The solder reflow profile should follow the recommendation from paste manufacturers and general standards such as JEDEC/IPC J-STD-20. Figure 7-5 shows the range of temperature profiles of the J-STD-20 specification. The profile parameters and component peak temperature guidelines are listed in Table 7-5.

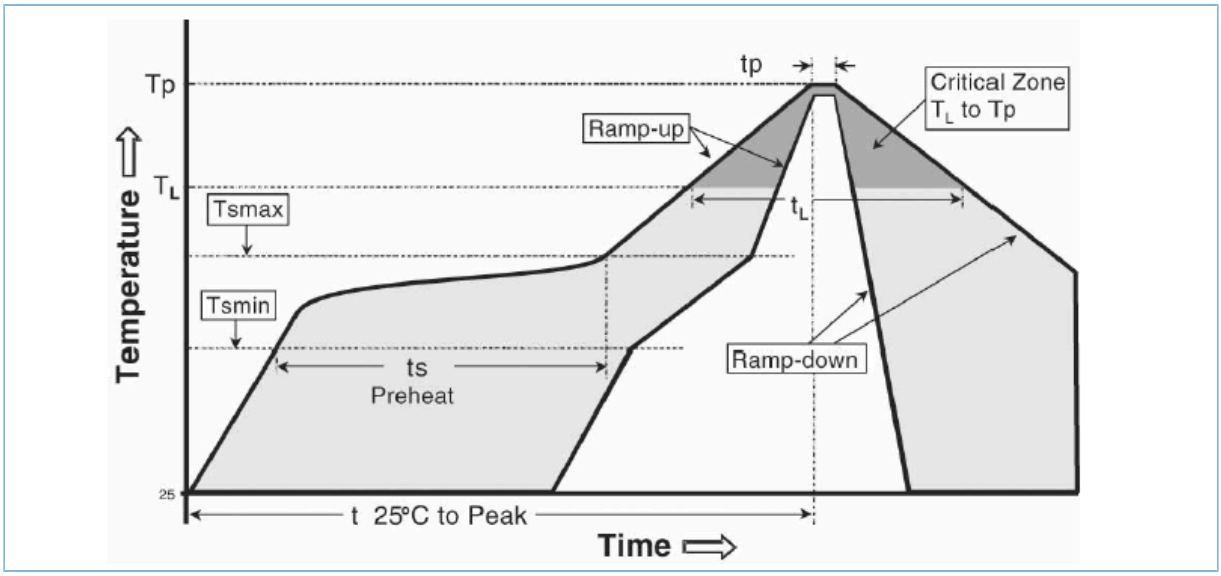

Figure 7-5 JEDEC recommended lead-free reflow profile

The GR5526 fulfills the lead-free soldering requirements from IPC/JEDEC, i.e. reflow soldering with a peak temperature up to 260°C.

The QFN68 lead frame is made of CμAg and has Matte Sn plating. This is 100% Sn and thus Pb-free. Plating thickness is 300 – 600 μin. The Matte Sn CμAg LF can withstand 3x reflow at 260°C.

Table 7-5 Reflow Profile Parameters

Profile Parameters	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate (Tsmax to Tp)	3°C/second (max)
Preheat temperature (Tsmin to Tsmax)	150°C – 200°C
Preheat time (ts)	60 seconds – 180 seconds
Time above TBL, 217°C (TL)	60 seconds – 150 seconds
Time within 5°C of peak temperature (tp)	20 seconds – 40 seconds
Ramp-down rate	6°C/second (max)
Time 25°C to peak temperature	8 minutes (max)

Note:

All specified temperatures in Table 7-5 refer to the temperatures measured on the top surface of the package.

It is very important to control the peak reflow temperature below the maximum temperatures specified in Table 7-5 to prevent thermal damage to the package. An example of reflow profile is shown in Figure 7-6.

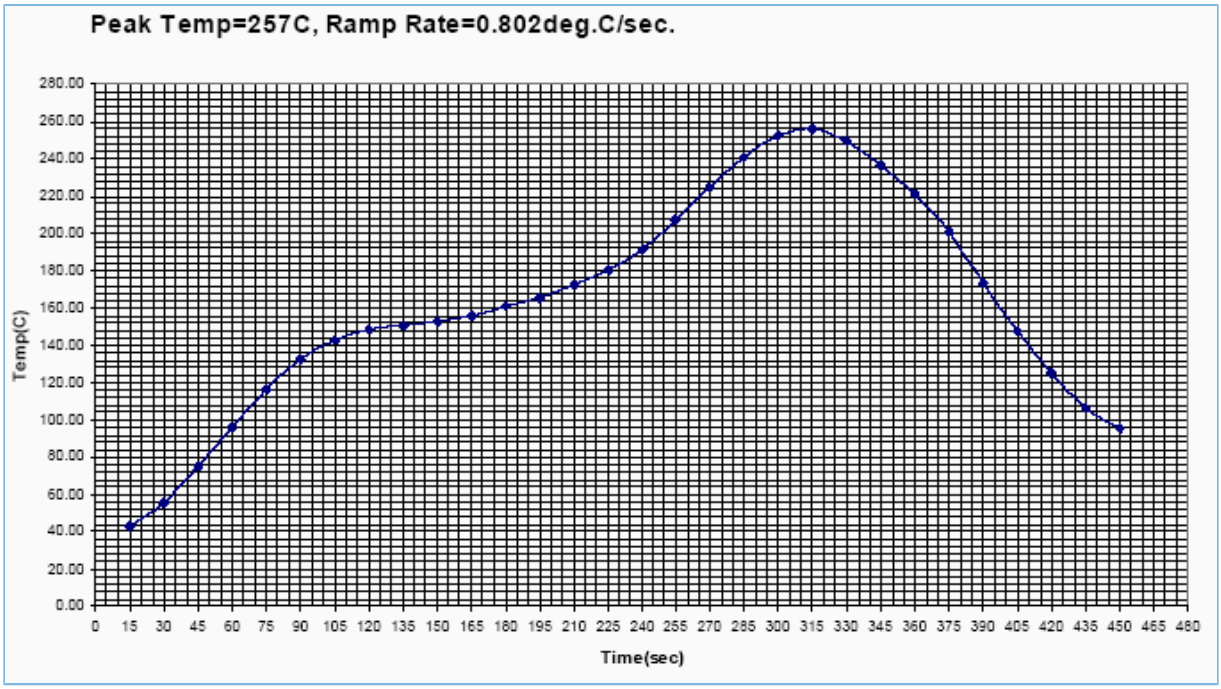

Figure 7-6 Reflow profile example with 257°C peak temperature

3. Reflow Oven

   It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. An oven with more heating zones offers higher flexibility to optimize the reflow profile for complex and/or larger boards. Nitrogen atmosphere can improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

7.4 Rework Guideline

Because solder joints are not fully exposed for QFN and BGA packages, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of QFN and BGA packages can be a challenge due to their small size.

In most applications, QFN and BGA packages will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Because reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for QFN package.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste printing
4. Component placement

5. Component attachment

Note:

Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

7.4.1 Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally, the reflow profile for part removal should be the same as the one used for part attachment. However, the time above the liquidus state can be reduced as long as the reflow is complete.

Note:

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and heated on the top side using hot gas or air.

Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided because this may cause chip scale package (CSP) to skew. Air velocity of 15 – 20 liters per minute is a good starting point. Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cool down.

Because of the small size of GR5526 SoCs, the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad lift-off.

7.4.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and de-soldering braid. The width of the blade should match to the maximum width of the footprint and the blade temperature should be low enough to prevent any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer’s recommendations should be followed.

7.4.3 Solder Paste Printing

Because of their small size and finer pitches, solder paste deposition for QFN packages requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100x magnification.

The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side. A 125 microns thick stencil with aperture size and shape same as the package land should be used.

In addition, no-clean flux should be used, because small standoff of QFN package does not leave much room for cleaning.

7.4.4 Component Placement

QFN package is expected to have superior self-centering ability due to their small mass. The placement of QFN packages should be similar to that of BGAs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The alignment should also be done at 50 to 100x magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

7.4.5 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Because all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

7.5 RoHS Compliant

GR5526 is RoHS compliant, as per directive 2002/95/EC and its subsequent amendments.

7.6 SVHC Materials (REACH)

GR5526 is compliant with Substance of Very High Concern (SVHC) list based on the publication by European Chemicals Agency (ECHA) on October 28, 2008 Regulation (EC) No 1907/2006 concerning *Registration, Evaluation, Authorisation and Restriction of Chemicals (REACH)*.

7.7 Halogen Free

GR5526 is compliant with BS EN 14582: 2007 in regards to halogens: fluorine, chlorine, bromine, and iodine content.