

# **GRPLT Lite Config Tool User Manual**

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Shenzhen Goodix Technology Co., Ltd.

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# Preface

#### Purpose

This document introduces how to install and use GRPLT Lite Config Tool, to help users quickly get started with testing GR5xx System-on-Chips (SoCs) over GRPLT Lite Config Tool.

### Audience

This document is intended for:

- GR5xx user
- GR5xx developer
- GR5xx tester
- GR5xx technical support engineer
- Technical writer

### **Release Notes**

This document is the seventh release of *GRPLT Lite Config Tool User Manual*, corresponding to GRPLT Lite Config Tool V1.1.4.

#### **Revision History**

Version	Date	Description	
1.0	2021-04-21	Initial release	
1.1	2021-10-11	<ul> <li>Updated some software interface screenshots and relevant functionality descriptions.</li> <li>Added the Cascading Cfg section.</li> </ul>	
1.2	2022-02-20	<ul> <li>Added descriptions specific to GR5526, a new series supported by GRPLT Lite Config Tool.</li> <li>Updated some software interface screenshots based on software changes.</li> <li>Added descriptions specific to new functionalities.</li> </ul>	
1.3	2022-06-27	Updated the software name and software interface screenshots.	
1.4	2023-01-10	<ul> <li>Added the following functionalities: erasing DUT transmit external Flash, configuring fool- proof time for programming startup by port level changes, and retesting the failed items.</li> <li>Delected description on the reserved function "External PA".</li> </ul>	
1.5	2023-03-30	Updated descriptions about GR5xx SoCs.	
1.6	2023-08-30	<ul> <li>Added descriptions about SoCs to which the RSSI test applies.</li> <li>In "Flash Cfg", updated the maximum number of sectors which can be erased each time to "3" when erasing by sector is selected.</li> <li>Added descriptions about the <b>Read OTP</b> functionality.</li> </ul>	

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# **1** Introduction

GRPLT Lite Config Tool is Goodix proprietary software for configuring the PLT Lite board. It packages relevant firmware, resource files, and mass production configurations to be downloaded to the PLT Lite board through USB-UART port, to support batch firmware download, resource download, parameter configuration, and functionality testing for Bluetooth Low Energy (Bluetooth LE) GR5xx SoCs.

#### Features:

- Configure firmware and resources.
- Configure Bluetooth address.
- Configure NVDS parameters.
- Configure firmware keys.
- Configure internal/external Flash.
- Configure crystal calibration parameters.
- Configure Received Signal Strength Indicator (RSSI) test parameters.
- Support configuring multiple DUTs connected in cascade.

#### **Note**:

- Golden Unit (GU) is an on-board Bluetooth LE module that has been calibrated prior to test.
- DUT refers to a PCB soldered with a GR5xx SoC in this document.

#### Functionalities of PLT Lite board:

- Crystal calibration: The GU generates specific square wave signals (40 Hz) and then delivers the signals to relevant I/O ports of the DUT, to perform crystal calibration for 1600000 times as expected.
- RSSI test: After a DUT performance test starts, the GU, as a slave, broadcasts data based on instructions sent via GRPLT Lite Config Tool. The DUT, as a master, receives RSSI test command frames via UART and uploads its RSSI value to the GU. The GU checks whether the DUT passes the performance test according to the uploaded RSSI value.

The RSSI test applies to GR551x, GR5525, and GR5526 SoCs only.

This document explains how to install and use GRPLT Lite Config Tool as well as fundamental processes of offline mass production programming on a GR5xx SoC.

# 2 Installation Instructions

This chapter describes the environment requirements as well as steps for installing GRPLT Lite Config Tool.

# 2.1 Installation Requirements

#### Hardware environment

Name	Description
СРИ	1.2 GHz and faster
Memory	1 GB and larger
USB	Power output: ≥ 500 mA; ripple: ≤ 100 mV

#### Operating system

Table 2-2 Operating system

Name	Description
Windows	Windows 7/Windows 10

## 2.2 Installation Steps

## 2.2.1 Installing CP2102N Driver

The complementary PLT Lite board adopts CP2102N chipset for UART communication. To ensure your PC recognizes all COM ports, you need to install CP2102N drivers prior to using GRPLT Lite Config Tool. Download the drivers from <a href="https://www.silabs.com/developers/usb-to-uart-bridge-vcp-drivers">https://www.silabs.com/developers/usb-to-uart-bridge-vcp-drivers</a>.

After installing CP2102N drivers, connect your PC to the PLT Lite board. Open **Windows/File Explorer** on your PC, and check COM ports in **Device Manager** > **Ports (COM & LPT)** to see whether the CP2102N drivers have been installed successfully.

Successful installation is indicated by a COM port (named as "Silicon Labs CP210x USB to UART Bridge") listed under **Ports (COM & LPT)**. Otherwise, installation fails or has not been completed.

#### 🛄 Note:

Ensure CP2102N drivers are successfully installed on your PC prior to downloading configurations on GRPLT Lite Config Tool to the DUT.

## 2.2.2 Installing GRPLT Lite Config Tool

GRPLT Lite Config Tool is available in a portable installation package (ZIP file). You can just decompress the ZIP file and start GRPLT Lite Config Tool by simply double-clicking <GRPLT Lite Config Tool\_Folder>\GRPLT Lite Config Tool.exe.

## Dote:

<GRPLT Lite Config Tool\_Folder> is the root directory of GRPLT Lite Config Tool software package.

The table below lists major folders and a file contained in <GRPLT Lite Config Tool\_Folder>.

#### Table 2-3 GRPLT Lite Config Tool software package

Folder/File Name Description		Remarks	
CustomApp	Stores to-be-programmed user firmware files (BIN).	Up to five BIN files are allowed.	
FlashData	Stores data to be programmed to DUT Flash.	-	
	Stores a nvds_config.json file that contains NVDS parameters		
NVDS	to be written to DUT Flash via GRPLT Lite Config Tool during	Only one JSON file is allowed.	
	DUT programming.		
	Stores files containing logs that are read from external		
log	Flash of the GU, PC-board interaction logs generated when		
LOg	configurations are downloaded to the DUT, and interaction		
	log (error) level settings.		
OtherOptions\BDAddr	Stores a Bluetooth address INI file.	Only one INI file is allowed.	
OtherOptions\CK_Memory	Stores a BIN file that enables SoC memory check.	Only one BIN file is allowed.	
OtherOptions\Enc. Custom	Stores a custom BIN firmware file that contains user-defined	Only one BIN file is allowed	
Other Options (Enc_Custom	encryption algorithms.	Only one Bin the is allowed.	
	Stores keys for DUT encryption in Made, control hin and	Only two BIN files are allowed. No	
OtherOptions\Enc_Goodix	Encrypt key info hin	modification on the file names is	
		allowed.	
	Stores test firmware files, which fall into four categories:		
	• Firmware where internal SoC clock is encrypted: Such BIN		
	file names shall contain a key word "INT_ENC".		
	• Firmware where internal SoC clock is unencrypted: Such		
	BIN file names shall contain a key word "INT".		
	Firmware where external crystal oscillator is encrypted:     Such PIN file pames shall contain a keyword "EXT_ENC"		
OtherOptions\FW_DUT		Prepare test firmware files based on	
	• Firmware where external crystal oscillator is unencrypted: Such BIN file names shall contain a key word "EXT".	actual project demands.	
	Note:		
	Firmware encryption is not required for tests on GR5526		
	SoCs. Therefore, the GR5526 file folder contains unencrypted		
	firmware files only. The same rule applies to other GR5xx		
	SoCs which do not require firmware encryption.		



Folder/File Name	Description	Remarks
OtherOptions\FW_GU	Stores a to-be-downloaded GU firmware file that contains all required logics in programming.	Only one BIN file is allowed. Neither modification nor deletion of the file is allowed.
OtherOptions\Reference	Contains ISP-enabled device connection diagrams, GRPLT Lite Config Tool error code for parameter configuration, and GRPLT Lite Config Tool error code for offline programming. The information is presented in both Chinese and English in ZH and EN folders respectively. Alternatively, you can directly open the files by simply clicking relevant buttons on the <b>Others</b> tab on GRPLT Lite Config Tool. For details, see "Section 3.2.6 Others".	Note that buttons in the <b>Reference Doc</b> area on the <b>Others</b> tab are unavailable if there are no files in OtherOptions \Reference.
OfflineUICfg.xml	Stores parameters set via GRPLT Lite Config Tool. For parameter details, see "Section 3.2 GRPLT Lite Config Tool Functionalities".	Parameter settings are automatically saved to <i>OfflineUICfg.xml</i> each time GRPLT Lite Config Tool is closed. In addition, GRPLT Lite Config Tool automatically loads the settings from the <i>OfflineUICfg.xml</i> file stored for the previous configuration each time you start the software.

# **3** Programming with GRPLT Lite Config Tool

This chapter explains the hardware connection, interface layouts, and operations in each functional module, to get started with GRPLT Lite Config Tool.

# **3.1 Hardware Connection**

Figure 3-1 shows how to connect a PLT lite board with your PC to download GU configurations to the PLT lite board through GRPLT Lite Config Tool.



Figure 3-1 Hardware connection

# **3.2 GRPLT Lite Config Tool Functionalities**

Double-click <GRPLT Lite Config Tool\_Folder>\GRPLT Lite Config Tool.exe to start GRPLT Lite Config Tool. Upon successful start, GRPLT Lite Config Tool automatically loads settings for the previous configurations stored in <GRPLT Lite Config Tool\_Folder>\OfflineUICfg.xml. If the XML file is missing, GRPLT Lite Config Tool loads the initial configurations.

Complete configurations on demand, and click **Download Cfg - Parallel** in the lower part of the interface to download the configurations to the DUT.

### Dote:

By default, clicking **Download Cfg - Parallel** starts configurations download and switches to the **Cascading** tab page. You can stop the download anytime by simply clicking **Interrupt** on the status bar.

# 3.2.1 Cfg Index

On the **Cfg Index** tab page (shown in Figure 3-2), GRPLT Lite Config Tool allows you to configure relevant parameters by jumping to corresponding tabs, download the configurations, and import/export the mirror files.

GRPLT Lite Config Tool		- 🗆 x 🔪
Cfg Index Basic Cfg Optional Cfg Fl	lash Cfg   eFuse/OTP Options   Others   Cascading Cfg   About	
PLT Lite Info Refresh Device status: No device GU Firmware> Configure	Basic cfg         Test Firmware Info>       Hardware Voltage>         Calibration Thresholds>       Custom Firmware>       Configure         RSSI Thresholds>       Rolling Test>	Configuration and Download Progress Info
Mirror File Options	Security Cfg Total Test Count: 500 UART Encryption	
Auto Save Download Cfg DOWNLOAD (Specific to selected COM)	Optional Cfg Start Test Mode> Bluetooth Address> I/O Level After Testing> NVDS Programming> Configure DUT Poweroff Delay> Encryption Algorithm>	
□ Download Cfg Only □ Lock Configurations Display Language ○ 简体中文 ● Enolish	Flash Program/Erase> Configure Cascading> Configure Debug eFuse W/R> Configure Others> Configure	Clear Display Info Read Logs Erase Logs
Download Cfg - Para	allel Interrupt Progress	0%



- In the **PLT Lite Info** area, you can check the status of the PLT Lite board.
  - **Refresh**: After plugging in/out PLT Lite boards to/from the PC, you need to click **Refresh** to update the board COM info.

For initial operation, GRPLT Lite Config Tool automatically displays the first COM port that is recognized by the software. You should select a proper COM port based on actual demands.

- **Device status**: It displays the current board status. Available statuses are listed below:
  - **Disconnected**: A board has been connected to the PC, but the GU fails to respond to the ISP Check instruction delivered by the PC.
  - **Connected**: The GU responds to the ISP Check instruction delivered by the PC, and the calibration value in the GU eFuse is not 0.
  - **GU Error**: The GU responds to the ISP Check instruction delivered by the PC, and the calibration value in the GU eFuse is 0.
  - **No device**: No PLT Lite board is connected to the PC.
- **GU Firmware**: In scenarios involving manual update of GU firmware or manual write of encryption info into the GU, click **Configure** to jump to the relevant configuration page. For details, see "Section 3.2.6 Others".
- In the Mirror File Options area, you can read or save the current configurations set on GRPLT Lite Config Tool.

- **Import** allows you to import an XML file that is generated by GRPLT Lite Config Tool for previous tests, and GRPLT Lite Config Tool automatically restores the imported data for the current configuration.
- Export allows you to save the current configurations to an XML file.
- In the **Download Cfg** area, click **DOWNLOAD** to download the current configurations to the GU corresponding to the selected COM port in the **PLT Lite Info** area.
- **Download Cfg Only**: Selecting the check box indicates that only manual configurations set on GRPLT Lite Config Tool are downloaded to the GU. Imported file data is excluded. Clearing the check box means downloading all relevant data set on GRPLT Lite Config Tool to the GU. By default, **Download Cfg Only** is cleared.

Note that **Download Cfg Only** can be selected only when no modification has been made to the imported file data.

- Lock Configurations: By default, this check box is cleared. Selecting the check box greys out configuration buttons on all tabs on GRPLT Lite Config Tool (exceptions: Refresh, DOWNLOAD, Download Cfg - Parallel, and Interrupt).
- In the Display Language area, you can switch the display language of the GRPLT Lite Config Tool user interface (UI) between Simplified Chinese and English. When you select a display language, GRPLT Lite Config Tool switches to the language after automatic restart.

### Dote:

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After you have downloaded configurations to the GU, the PLT lite board presents information in a language that is consistent with that you have chosen for GRPLT Lite Config Tool.

- In the **Basic Cfg** area, click the **Configure** button to jump to the corresponding configuration tab page. For details, see "Section 3.2.2 Basic Cfg".
- In the **Security Cfg** area, you can configure the following:
  - Total Test Count: total programming count of the PLT Lite board. This value is the upper programming number limit for a selected PLT Lite board. When the programming count reaches the limit, the programming on the PLT Lite board stops. Modification on this parameter is allowed only after current configurations are downloaded to the PLT Lite board.
  - **UART Encryption** (reserved): Selecting this check box means the GU-to-DUT communication data via UART is encrypted.
- In the **Optional Cfg** area, click the **Configure** buttons to jump to corresponding configuration tab pages. For details, see "Section 3.2.3 Optional Cfg", "Section 3.2.4 Flash Cfg", and "Section 3.2.7 Cascading Cfg".
- In the **Debug** area, click the **Operate** or **Configure** button to jump to corresponding configuration tab pages. For details, see "Section 3.2.5 eFuse/OTP Options" and "Section 3.2.6 Others".
- In the **Configuration and Download Progress Info** area, you can perform the following:
  - **Clear Display Info**: Click this button to clear data displayed in the above area.

- **Read Logs**: Click this button to read error logs stored in the external Flash of the GU, and the logs are saved as CSV files named as their saving time under <GRPLT Lite Config Tool\_Folder>\Log.
- **Erase Logs**: This function helps you erase error logs of all GUs that are connected to the PC, and set the log offset in the GU to zero.

# 3.2.2 Basic Cfg

Click Basic Cfg to open a tab page (as shown below) where you can configure basic programming parameters.

GRPLT Lite Config Tool			
Cfg Index Basic Cfg Optional Cfg Flash Cfg eFuse/OTP Options Others Cascad	ing Cfg About		
Test Firmware Info Test FW Type: GR5526  GR5526  Function Constraints of the set of the	Test Items         ✓ XTAL Calibration       XtalErrLimit: ≤       60       XtalIO:       GPI0_2 ∨         Write to NVDS       XtalNum:       0       XtalOffset:       0         ✓ RSSI Test       RSSt ≥       -90       -90         ☐ Rolling       InitValue:       Step:       BurnAddr (0x)		
Hardware voltage (1700 mV-3500 mV)         Custom Firmware Info           PWM_VOL (mV)         3300           UART_VOL (mV)         3300           FLASH_VOL (mV)         3300           DUT SoC Model:         GR5526VGBIP	Upload Firmware		
eFuse IO_LDO_SEL IO_LDO_Selector (3.3 V) IO_LDO_Bypass (VBAT) Inductance (1.5 µH) IO_PWR_SRC (External)	bin->ebin            bin->mbin		
Download Cfg - Parallel Interrup	t Progress 0%		

Figure 3-3 Basic Cfg tab

- In the **Test Firmware Info** area, you can configure relevant parameters for test firmware.
  - **Test FW Type**: Options include the specific part number of GR5xx SoC series, corresponding to the file folders in <GRPLT Lite Config Tool\_Folder>\OtherOptions\FW\_DUT.

### 🛄 Note:

Taking **GR5515** as an example, the following part in this section elaborates on how to select a proper test firmware file. The same rule applies to other GR5xx SoCs.



When you select External XO FW, GRPLT Lite Config Tool automatically loads corresponding files from <GRPLT Lite Config Tool\_Folder>\OtherOptions\FW\_DUT\GR5515. The files are displayed in the relevant fields.

Unencrypted FW: Displays a BIN file with a key word of "EXT".

- **Encrypted FW**: Displays a BIN file with a key word of "EXT\_ENC". Firmware encryption is not required for tests on GR5526 SoCs. Therefore, the **Encrypted FW** field is greyed out when you select **GR5526** for **Test FW Type**. The same rule applies to other GR5xx SoCs which do not require firmware encryption.
- When you select Internal CLK FW, GRPLT Lite Config Tool automatically loads corresponding files from <GRPLT Lite Config Tool\_Folder>\OtherOptions\FW\_DUT\GR5515. The files are displayed in the relevant fields.

Unencrypted FW: Displays a BIN file with a key word of "INT".

- **Encrypted FW**: Displays a BIN file with a key word of "INT\_ENC". Firmware encryption is not required for tests on GR5526 SoCs. Therefore, the **Encrypted FW** field is greyed out when you select **GR5526** for **Test FW Type**. The same rule applies to other GR5xx SoCs which do not require firmware encryption.
- Selecting **Unencrypted** greys out **Encrypted FW**, **ModeCtrl**, and **KeyInfo**.
- Selecting Encrypted greys out Unencrypted FW.
- Import files:
  - Import .bin for Encrypted FW and Unencrypted FW: These two buttons allow importing BIN files from <GRPLT Lite Config Tool\_Folder>\OtherOptions\FW\_DUT\GR5515 only.
  - Import .bin for ModeCtrl and KeyInfo: These two buttons allow importing BIN files from <GRPLT Li te Config Tool\_Folder>\OtherOptions\Enc\_Goodix only.
- In the **Test Items** area, you can configure relevant programming thresholds.
  - **XTAL Calibration**: Selecting this item means calibration test on DUT crystal oscillator is enabled.
    - **XtalErrLimit**: Upper limit gap between the systick value responded by the DUT and 1600000.
    - **XtalIO**: You can select a GPIO of the DUT for calibration from the drop-down list.
    - XtalNum: repeat test times for crystal calibration. Maximum: 100
    - **XtalOffset**: This item represents the limit difference between the maximum value and minimum value of the calibration register during repeat test for crystal calibration. Maximum **XtalOffset**: 255. Only when **XtalNum** is set to an integer larger than 1, **XtalOffset** takes effect.
  - Write to NVDS: Selecting this item means writing crystal calibration value into NVDS is enabled.
  - RSSI Test: Selecting this item means RSSI test on the DUT is enabled. This item applies to GR551x, GR5525, and GR5526 SoCs only.

**RSSI**: the lower RSSI limit in test.

• **Rolling**: Selecting this item means writing to DUT Flash from **InitValue** at **Step** is enabled (applicable to internal Flash only).

- InitValue: initial value for rolling
- Step: step value for rolling
- **BurnAddr(0x)**: Flash address to which rolling data is written. Each rolling data entry occupies four bytes.
- In the **Hardware Voltage** area, you can set the relevant voltages for the DUT within a range of 1700 mV–3500 mV (proper values should be set in accordance with the selected DUT schematics).
  - **PWM\_VOL**: communication voltage of I/O for crystal oscillator calibration
  - UART\_VOL: communication voltage of UART I/O
  - **FLASH\_VOL**: communication voltage of the I/O that is directly connected to external DUT Flash
  - **DUT SoC Model**: supported GR5xx SoC models

### 🛄 Note:

The eFuse configurations vary depending on the selected DUT SoC model.

- In the eFuse area, you can enable corresponding items in accordance with the selected DUT SoC model.
   Selecting Force Write means GRPLT Lite Config Tool writes the configurations on the UI to Bit0–Bit3 of IO\_LDO\_SEL regardless of the DUT SoC model. Clearing Force Write means GRPLT Lite Config Tool writes configurations to the corresponding bit based on the DUT SoC model that you have chosen.
  - Selecting Bit0: IO\_LDO Selector (3.3 V) means VIO\_LDO\_OUT output is set to 3.3 V, and clearing this item means VIO\_LDO\_OUT output is set to 1.8 V.
  - Selecting Bit1: IO\_LDO\_Bypass (VBAT) means voltage levels of some GPIOs are fixed to 3.3 V.
  - Selecting Bit2: Inductance (1.5 μH) indicates that the external inductance of the DC-DC converter of the DUT is 1.5 μH. Clearing this item means the inductance is 2.2 μH.
  - Selecting Bit3: IO\_PWR\_SRC (External) indicates that VBAT is the input for VDDIO and VIO\_LDO\_OUT with internal IO\_LDO disabled in the SoC. Clearing Bit3: IO\_PWR\_SRC (External) means that the VDDIO is supplied by the internal IO\_LDO that should not be disabled.

### Dote:

- Some GPIOs for Bit1: IO\_LDO\_Bypass (VBAT) include GPIO\_16, GPIO\_17, GPIO\_24–GPIO\_26, GPIO\_30, GPIO\_31, and AON\_GPIO\_1–AON\_GPIO\_3.
- Bit0–Bit3 represent the lower four bits with an offset of 0x111 in eFuse. Selecting the bit means writing 1 to the bit.
- For GR5513BENDU SoCs, the GPIO level is determined by the bypass bit. If the bypass bit in eFuse is set to 1, the GPIO level changes in accordance with the VBAT.
- In the **Custom Firmware Info** area, you can configure relevant parameters for custom firmware.

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## 🛄 Note:

- It is your responsibility to ensure that the saving address of custom firmware is within the address range in the DUT Flash. GRPLT Lite Config Tool does not check or guarantee the validity of your input address.
- During pre-programming, it is your responsibility to ensure the validity of the custom firmware that is to be written to the Flash of DUT (firmware data and image info of the firmware header should be correct). GRPLT Lite Config Tool does not check or guarantee the validity of your input firmware data.

Two firmware programming approaches are supported:

Local Programming: Custom firmware is programmed to the DUT during programming. Supported firmware file formats: BIN (default), EBIN, and MBIN. After you have selected a firmware type, GRPLT Lite Config Tool automatically loads the corresponding firmware file(s) in your selected format from <GRPLT Lite Config Tool\_Folder>\CustomApp. You can see the relevant file(s) on the firmware list below Local Programming.

You can click **Upload Firmware** to refresh the listed firmware files in a selected format from <GRPLT Lit e Config Tool\_Folder>\CustomApp.

GRPLT Lite Config Tool supports format conversion of locally programmed firmware.

- **bin->ebin**: Convert BIN files in <GRPLT Lite Config Tool\_Folder>\CustomApp to EBIN files.
- **bin->mbin:** Package BIN files in <GRPLT Lite Config Tool\_Folder>\CustomApp and boot options to one EBIN file.

Prior to clicking **Convert**, click **Upload Firmware** to refresh the listed custom firmware, and select boot option(s). Selecting **Delete Others** indicates that files in formats other than MBIN in <GRPLT Lite Config Tool\_Folder>\CustomApp (subfolder excluded) will be deleted after the conversion.

## Dote:

Prior to refreshing MBIN firmware files, ensure that there is only one MBIN file in <GRPLT Lite Config Tool\_F older>\CustomApp (subfolder excluded). Otherwise, an error occurs.

• **Pre-programming**: There is no need to programme custom firmware into the DUT during programming. You only need to set the saving address of boot options that will be started when the programming completes.

# 3.2.3 Optional Cfg

Click **Optional Cfg** to open a tab page (as shown in Figure 3-4) where you can configure optional programming parameters.

GRPLT Lite Config Tool			
Cfg Index   Basic Cfg   Optional Cfg   Flash Cfg   eFuse/OTP Options	hers Cascading Cfg About		
Test Start Mode	Bluetooth Address		
By Board Button	Programming Bluetooth Address	Write to NVDS	
	<ul> <li>Manual Setting (Hexadecimal)</li> </ul>	O Auto Read	
(Select a GMO) (Set GMO Edge)	Start Address 12 34 56	78 90 AB	
On GPIO_XX Edge GPIO_2 Rising edge	End Address 12 34 56	FF FF FF Remove Duplicate Import .ini	
5500 (500~5000)	NVDS Programming		
I/O Level After Testing	Program NVDS		
$\hfill VO$ Level GPIO_2 $\hfill \lor$ Rising edge $\hfill \lor$	Start Address: (0x) 002FE000	NVDS Sector Size: 1 (Multiple of 4096)	
(Select a GPIO) (Set GPIO Edge)	NVDS File Path:	Import .json	
DUT Poweroff Delay	Encryption Algorithm		
Delay (s) 20 (Decimal)	Goodix Encryption (Default for Encryption	oted Firmware)	
WDT	Custom Encryption		
T DW	Custom Algorithm FW:	Import .bin	
Initial Level High level V	Memory Check		
Cycle (ms) (1000ms-30s)	Memory Check		
Beeper	Memory Check FW:		
Sound upon Test Success Duration (s): Always 🗸 (Decimal)	Retry Setting		
Sound upon Test Failure Duration (s): 3 (Decimal)	Enable Retry Retry Count:	5 Restart Threshold: 4	
Download Ctg - Parallel	Interrupt Progress	0%	

#### Figure 3-4 Optional Cfg tab

- In the Test Start Mode area, you can configure the start mode for mass production programming on a DUT.
  - **By Board Button**: Start programming by pressing **K2/K5** on a PLT Lite board.
  - **On CHIP\_EN High**: Programming is started when the CHIP\_EN pin is detected high.
  - **On GPIO\_XX Edge**: Programming is started when edge transition on GPIO\_XX pin is detected.
  - Detection Interval (ms): When On CHIP\_EN High/On GPIO\_XX Edge is selected to start programming based on port level changes, set the interval to check whether the port level is still proper for programming, to avoid misoperation.

#### 🛄 Note:

You can select either On CHIP\_EN High or On GPIO\_XX Edge.

 In the I/O Level After Testing area, you can configure a GPIO as high/low level to indicate the programming is completed.

### 🛄 Note:

The configured GPIO should not be selected in **On GPIO\_XX Edge** in the **Test Start Mode** area.

• In the **DUT Poweroff Delay** area, you can set the delay (unit: second) after which the DUT is powered off when the programming is completed.

• In the **WDT** area, you can enable the PLT Lite board to output PWM waves which are applicable to scenarios involving external hardware watchdogs of the DUT.

You can set the initial state and cycle of PWM waves.

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• In the **Beeper** area, you can configure the sound mode and duration of the beeper when the programming succeeds or fails.

Selecting **Always** means that the beeper sounds until GU reset occurs.

• In the **Bluetooth Address** area, you can configure the Bluetooth address of the DUT to which the programmed data is written.

GRPLT Lite Config Tool supports two approaches to configuring the Bluetooth address. You can choose either one after selecting **Programming Bluetooth Address**.

- Manual configuration: Select Manual Setting (Hexadecimal), and type the address range in Start Address and End Address.
- Automated reading of Bluetooth address from a file: Select **Auto Read**, and click the **Import .ini** button to choose and import a local Bluetooth address INI file.

Select **Remove Duplicate** to remove duplicated Bluetooth addresses in the imported INI file.

- In the NVDS Programming area, you can decide whether to programme data to the NVDS in the DUT. Select
   Program NVDS, and configure both the Start Address: (0x) and NVDS Sector Size. Choose the JSON file from <GR</li>
   PLT Lite Config Tool\_Folder>\NVDS.
- In the Encryption Algorithm area, Custom Encryption allows you to implement your custom encryption algorithms in your encryption algorithm firmware. Place your algorithm firmware BIN file in <GRPLT Lite Config Tool\_Folder>\OtherOptions\Enc\_Custom prior to importing it to GRPLT Lite Config Tool.
- In the Memory Check area, you can check the memory of the SoC in the DUT.
   Prior to selecting Memory Check, you need to place the check firmware file (BIN) into OtherOptions\CK\_Memory. GRPLT Lite Config Tool automatically loads and displays the file in the Memory Check FW field.
- In the **Retry Setting** area, you can set the count (**Retry Count**) for retesting the failed items in a test and **Restart Threshold**.
  - **Retry Count**: Set the total test count for all the failed items in a test.
  - **Restart Threshold**: Set the threshold to restart DUT when the test count for failed items reaches the threshold, and then redo tests. **Restart Threshold** shall be less than **Retry Count**.

# 3.2.4 Flash Cfg

Click **Flash Cfg** to open a tab page (as shown below) where you can configure Flash-related parameters for both Flash programming and erasing.

GRPLT Lite Config Tool					- 🗆 × 🗌
Cfg Index Basic Cfg Optional Cfg Fla	eFuse/OTP Option	ns Others Cascading Cf	g About		
Flash Programming (Address 4 Kl	B Aligned)				
Flash Programming					
<ul> <li>Internal Flash</li> </ul>	Start Address 1: 0x		bin file 1		Import
O Direct External Flash	Start Address 2: 0x		bin file 2		Import
O DUT Transit External Flash	Start Address 3: 0x		bin file 3		Import Clear .bin File(s)
	Start Address 4: 0x		bin file 4		Import
	Start Address 5: 0x		bin file 5		Import
Direct External Flash Configure	Transit External Flash	Configure GPIO Type	GPIO Pin Pin MUX	GPIO Type	GPIO Pin Pin MLIX
Speed 8M V	O SPI				
Model: Others ~	O QSPI 0	NORMAL V GPIO	_26	TOT, NORMAL	GPIO_23 V MUX_0 V
Page Size: 256 🗸	O QSPI 1 CLK:	NORMAL V GPIO	_21 V MUX_0 V	IO2: NORMAL V	GPIO_24 V MUX_0 V
Block Erase	O QSPI 2 100:		_22 ~ MUX_0 ~	IO3: NORMAL ~	GPIO_25 V MUX_0 V
Erase Internal Flash (Address 4 KB Aligned)					
Erase Internal Flash Start	1: 0x	End 1: 0x	Erase External	Flash Start 1: 0x	End 1: 0x
Erase All Start 2	2: 0x	End 2: 0x	Erase All	Start 2: 0x	End 2: 0x
Timeout	2: 0x	End 2: 0x	Timeout	Start 2: 0v	End 2: 0x
Start.	3. UX			Start 5. 0X	Life J. ox
Download Cfg - Paral	llel	Interrupt	Progress		0%

#### Figure 3-5 Flash Cfg tab

• Flash Programming: Select Flash Programming, and configure the location of the (internal or external) Flash to which data is downloaded. Ensure the programmed data size does not exceed the space assigned in the Flash. GRPLT Lite Config Tool does not check or guarantee the correctness of the data size.

#### **Note**:

You can configure up to five start addresses from five BIN files to which data is written. The BIN files must be placed under <GRPLT Lite Config Tool\_Folder>\FlashData before the Flash settings.

- Internal Flash: The data is downloaded to internal Flash of the SoC. You need to set the start address(es) and BIN file(s) on demand.
  - For GR551x SoCs: A valid programming address starts from 01002000.
  - For GR5526 SoCs: A valid programming address starts from 00202000.

### 🛄 Note:

The above programming addresses are for GR551x and GR5526, respectively; the programming addresses for other SoC series are different depending on the practical Flash size.

- GODIX
  - Direct External Flash: The data is downloaded to external SoC Flash that is directly connected to the QSPI pin of the PLT Lite board. No configuration on programming pin(s) is required. You need to set the start address(es) and BIN file(s) on demand.

**Speed**: speed for downloading data to the direct external Flash via SPI. Maximum: 8 Mbps.

• **DUT Transit External Flash**: The data is downloaded to the external SoC Flash that is not directly connected to the PLT Lite board. You need to set the programming pin(s), start address(es), and BIN file(s) on demand.

Click Clear .bin File(s) to clear imported BIN files.

- Erase Flash: GRPLT Lite Config Tool allows you to erase both internal and external Flash of an SoC. You can choose to erase either all data or by sector (within a specified address range). Select Erase Internal Flash or Erase External Flash to erase internal or external Flash data.
  - **Erase All**: Selecting this item means all data in the Flash will be erased. There is no need to configure the erasing address.

**Timeout**: This parameter is to ensure that **Erase All** functions properly. It can be slightly longer than the reference time for chip erase as listed in the corresponding Flash datasheet.

• Erase by sector: Select **Erase Internal Flash** or **Erase External Flash**, and type the start and end addresses of the sector to be erased.

### Dote:

For erasing by sector, you can erase up to three sectors each time.

# 3.2.5 eFuse/OTP Options

Click **eFuse/OTP Options** to open a tab page (as shown below) where you can configure parameters specific to the DUT eFuse/OTP.



GRPLT Lite Config Tool		- 🗆 x 🔪
Cfg Index   Basic Cfg   Optional Cfg   Flash Cfg   eFuse/OTP	Options Others Cascading Cfg About	1
Data Display Area		
		DUT Operations         Read eFuse         Read OTP
Download Cfg - Parallel	Interrupt	Progress 0%

Figure 3-6 eFuse/OTP Options tab

In the **DUT Operations** area, you can perform the following:

• Click **Read eFuse**, and GRPLT Lite Config Tool automatically reads the eFuse information in the DUT and displays the results in **Data Display Area** on the left side of the tab page.

After the eFuse read operation completes, GRPLT Lite Config Tool analyzes the read information and displays the parsed key information in **Parsing Key Info** in the lower-right corner.

• Click **Read OTP**, and GRPLT Lite Config Tool automatically reads the OTP information in the DUT and displays the results in **Data Display Area** on the left side of the tab page.

## 3.2.6 Others

Click **Others** to open a tab page (as shown below) where you can configure other parameters that are not covered in the previous tab pages.





Figure 3-7 Others tab

The **Others** tab contains parameters or functionalities listed below:

- Repeat Count: number of programming performed on one DUT
- Print Test Logs: This function allows logs that are generated during mass production programming to be transmitted to a UART pin. GPIO\_0 or GPIO\_1 of the GU serves as the output pin for the log transmission (this function is not applicable to cascading scenarios, and RTS shall be cleared for Flow Control on GRUart). Disable Print Test Logs during mass production programming to shorten unnecessary test duration.
- **GU Firmware Upgrade (Encrypted)**: You can upgrade a GU independently by selecting and importing the relevant GU firmware file.
- **GU Encryption**: GRPLT Lite Config Tool allows you to write encryption information into a GU.
- Modify Boot Save Address of Unencrypted FW: Import a firmware file (BIN), and set the Target Address: 0x. Click Modify to generate a new firmware file in the directory where you have imported the legacy firmware file.
- **ISP Connection**: Click this button to open an ISP-enabled device connection diagram in PDF format in a browser.
- **Configuration Error Code**: Click this button to download and open *GRPLT Lite Config Tool Configuration Error Code*.
- **Test Error Code**: Click this button to download and open *GRPLT Lite Config Tool Mass Production Test Error Code*.

## 3.2.7 Cascading Cfg

# G@DiX

Click **Cascading Cfg** to open the cascading configuration tab. GRPLT Lite Config Tool allows you to download data to and configure data on multiple GUs that are connected to the PC.

1. Click **Update Device** to check the COM connection status.

GRPLT Lite Config Tool delivers an ISP check instruction to all GUs that are connected to the PC. As shown in the figure below, the status for a COM port displaying as "Connect" indicates successful instruction delivery.



Figure 3-8 Checking COM connection status

- 2. You can select **Check All** to choose all DUTs, or select some DUTs by selecting the corresponding COM ports.
- Click Download Cfg Parallel in the lower part of the tab to download the configurations to the selected DUT(s).
   You can check the configuration download progress from the display box of and progress bar below each DUT.
  - Progress bar: configuration download progress represented by percentage
  - Background color of display box and progress bar: The color green indicates a download succeeds while red indicates a download fails.

# 3.3 Programming

This section introduces process and operations of programming a DUT offline prior to putting it into mass production. You can obtain the programming results by observing the states of corresponding LEDs.

# 3.3.1 Programming Process

The following figure displays the process of programming a DUT offline:



Figure 3-9 Offline DUT programming process

### **Note**:

The programming process listed in the figure above applies to programming involving all configuration items only. For programming with different SoCs or with custom item selections, such as programming where downloading encryption information or custom firmware is not required, the actual programming process prevails.

# 3.3.2 Programming Operations

Follow the steps below to properly start programming on a DUT.

- 1. Upon successful configurations download, close GRPLT Lite Config Tool.
- 2. Connect a DUT to a PLT Lite board, as shown below.



Figure 3-10 Connection between PLT Lite and DUT

In programming involving multiple PLT Lite boards, connect the boards in parallel, and long press **K2** on the master board for data synchronization. In cascading scenarios, the master board is the one that is connected to another board via its male connector, and the rest are regarded as slave boards. Upon successful synchronization, each board LCD presents a synchronization number (Arabic number in sequence; a failed synchronization results in a RSSI test error).

### **Note**:

The RSSI test applies to GR551x, GR5525, and GR5526 SoCs only.

### 3. Start programming by pressing **K5** on the master board.

The table below elaborates on the button-related operations on a PLT Lite board.

Button and Operation	Description			
K2, press	Start programming on the corresponding board.			
K2, double-press	Present the name of the to-be-programmed custom firmware file on an LCD. When multiple custom firmware files are involved, double-press <b>K2</b> again to display the next file name.			
K2, long press	Enable data synchronization from the master board to slave board(s).			
K5, press	Start programming on all cascaded PLT Lite boards.			
K5, double-press	Present start address, end address, and programming times of Bluetooth device on an LCD.			

#### Table 3-1 PLT Lite board buttons

# G@DiX

Button and Operation	Description
K5, long press	Present the firmware version, total programming count, and programmed count of a GU on an LCD.

### **Note**:

In programming involving multiple PLT Lite boards connected in parallel, use either encrypted or unencrypted firmware files. Mixing of encrypted firmware files with unencrypted ones is not allowed.

# 3.3.3 Programming Results

When the programming is completed, you can check the programming results by reading data on the PLT Lite LCD or observing the flickering of LEDs in the lower-right corner of a board.

- Programming succeeded: The LED 2 (silkscreen: D2) keeps flickering in green, and the LCD presents that programming has succeeded.
- Programming failed: The LED 3 keeps flickering in red, and the LCD presents error information.
- Programming results of cascaded boards: The LED 4 serves as the cascading status indicator. When a master/ slave board is connected to an existing board or cascading data is delivered to the board, the LED 4 flickers in blue five times. If there is an existing master or slave board, the LED 4 remains on in blue.