TFA9882_DS

3.4 W I^2S Input Mono Class-D Audio Amplifier

Version: 4.2

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Contents

1 General description

The TFA9882 is a mono, filter-free class-D audio amplifier in a 9-bump wafer level chip-scale package (WLCSP) with a 400 µm pitch.

It receives audio and control settings via an I^2S digital interface. The power-down to operating mode transition is triggered when a clock signal is detected on the bit clock input (BCK). Two devices can be combined to build a stereo application.

In stereo applications, the left or right I^2S audio stream is selected by connecting the word select signal to, respectively, pin WSL or pin WSR. Mono mixing can be achieved by connecting the word select signal to both WSL and WSR. Switching off the word select signal selects Mute mode.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in the TFA9882 provides excellent audio performance and high supply voltage ripple rejection.

2 Features and benefits

- Small outline WLCSP9 package: 1.50 × 1.28 × 0.60 mm
- Wide supply voltage range (fully operational from 2.5 V to 5.5 V)
- High efficiency (90 %, 4 Ω/20 µH load) and low power dissipation
- Quiescent power:
  - 6.5 mW (V_{DDD} = 1.8 V, V_{DDP} = 3.6 V, 4 Ω/20 µH load, f_s = 32 kHz)
  - 7.65 mW (V_{DDD} = 1.8 V, V_{DDP} = 3.6 V, 4 Ω/20 µH load, f_s = 48 kHz)
- Output power:
  - 1.4 W into 4 Ω at 3.6 V supply (THD = 1 %)
  - 2.7 W into 4 Ω at 5.0 V supply (THD = 1 %)
  - 3.4 W into 4 Ω at 5.0 V supply (THD = 10 %)
- Output noise voltage: 24 µV (A-weighted)
- Signal-to-noise ratio: 103 dB (V_{DDP} = 5 V, A-weighted)
- Fully short-circuit proof across load and to supply lines
- Current limiting to avoid audio holes
- Thermally protected
- Undervoltage and overvoltage protection
- High-pass filter for DC blocking
- Simplified interface for audio and control settings
- Left/right selection and mono mixing
- Three gain settings: −3 dB, 0 dB and +3 dB
- Output slope setting for EMI reduction
- Clip control for smooth clipping
- Mute mode
- Low RF susceptibility
- Insensitive to input clock jitter
- ‘Pop noise' free at all mode transitions
- Short power-up time: 4 ms
- Short power-down time: 5 µs
- 1.8 V/3.3 V tolerant digital inputs
- Only two external components required

3 Applications

- PDAs
- Mobile phones
- Portable gaming devices
- Portable navigation devices (PND)
- Notebooks/netbooks
- Portable media players

4 Quick reference data

Table 4-1: Quick reference data

All parameters are guaranteed for V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{DDP}	power supply current	operating mode with load	-	1.5	1.7	mA
		mute mode	-	1.1	1.25	mA
		power-down mode	-	0.1	1	µA
I_{DDD}	digital supply current	operating mode	-	1.25	1.4	mA
		mute mode	-	1.1	1.2	mA
		Power-down mode BCK = WS = DATA = 0 V	-	2.5	10	µA
$P_{o(RMS)}$	RMS output power	THD+N = 1 %				
		V_{DDP} = 3.6 V, f_i = 100 Hz	-	1.4	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz	-	2.7	-	W
		THD+N = 10 %				
		V_{DDP} = 3.6 V, f_i = 100 Hz	-	1.75	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz	-	3.4	-	W
η_{po}	output power efficiency	$P_{o(RMS)}$ = 1.4 W	-	90	-	%

[1] R_L = load resistance; L_L = load inductance.

5 Ordering information

Table 5-1: Ordering information

Type number	Package		
	Name	Description	Version
TFA9882UK/N2	WLCSP9	wafer level chip-scale package; 9 bumps; 1.50 × 1.28 × 0.60 mm body	SOT1384-4

6 Block diagram

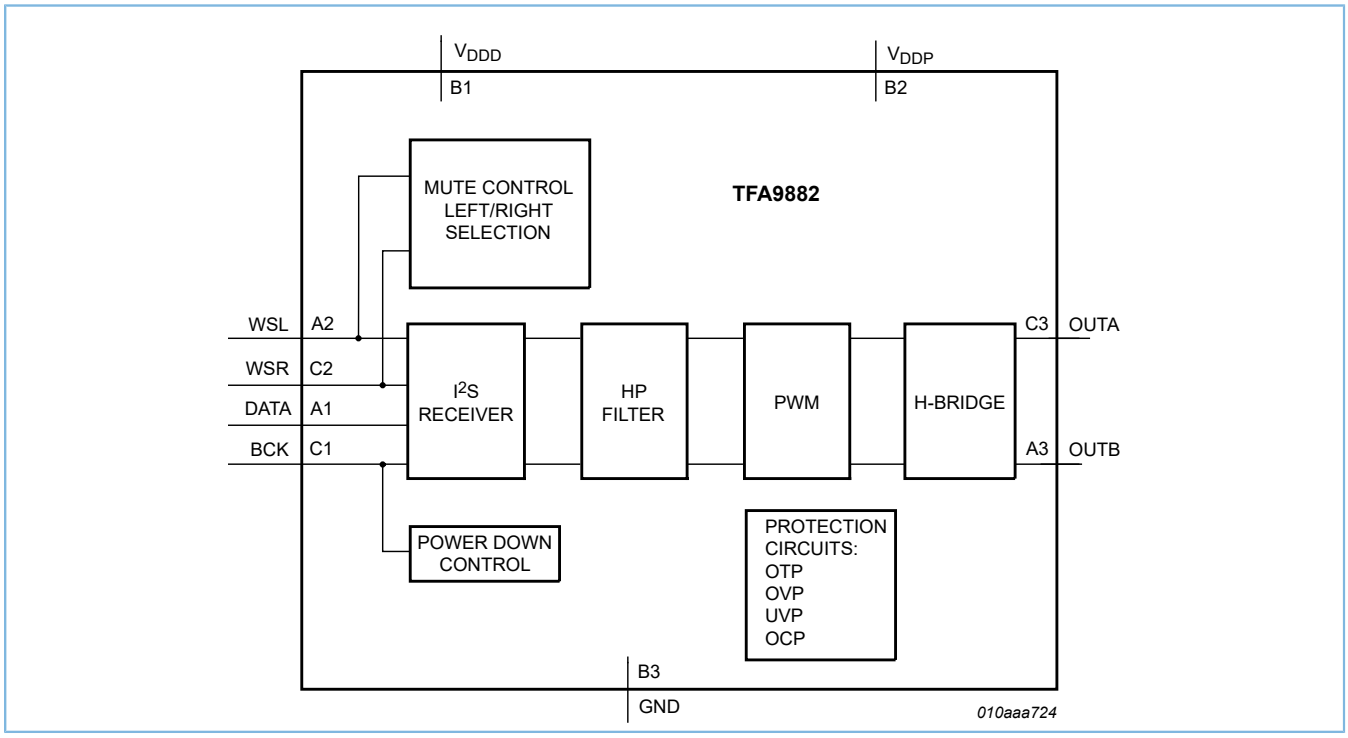
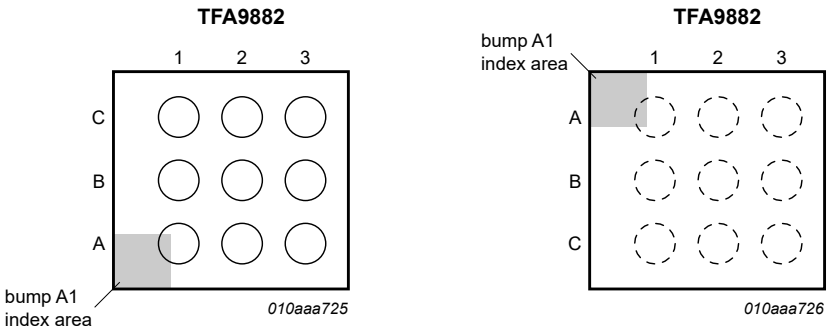


Figure 6-1: Block diagram of the TFA9882

7 Pinning information

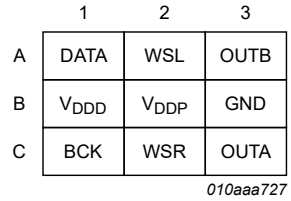
7.1 Pinning



a. Bottom View

b. Transparent top view

Figure 7-1: Bump configuration for WLCSP9



Transparent top view

Figure 7-2: Bump mapping for WLCSP9

7.2 Pin description

Table 7-1: Pin description

Symbol	Pin	Type	Description
DATA	A1	I	data input
WSL	A2	I	word select input left channel; connect to V_{DDP} or PCB ground if right channel is selected
OUTB	A3	O	inverting output
V_{DDD}	B1	P	digital supply voltage (1.8 V)
V_{DDP}	B2	P	power supply voltage (2.5 V to 5.5 V)
GND	B3	P	ground reference

Symbol	Pin	Type	Description
BCK	C1	I	bit clock input
WSR	C2	I	word select input right channel; connect to V_{DDP} or PCB ground if left channel is selected
OUTA	C3	O	non-inverting output

8 Functional description

The TFA9882 is a high-efficiency mono bridge tied load (BTL) class-D audio amplifier with a digital stereo I^2S input interface. A high-pass (HP) filter removes the DC components from the incoming I^2S stream. This stream is subsequently converted into two pulse width modulated (PWM) signals. A 3-level PWM scheme supports filterless speaker drive.

8.1 Mode selection and interfacing

The TFA9882 supports four operating modes:

- **Power-down mode**, with low supply current
- **Mute mode**, in which the output stages are floating so that the audio input signal is suppressed
- **Operating mode**, in which the amplifier is fully operational, delivering an output signal
- **Fault mode**

The TFA9882 switches to fault mode automatically when a protection mechanism is activated (see Section 8.8). The defined patterns required on the BCK, WSL and WSR inputs to select the other three modes are given in Table 8-1.

Power-down mode is selected when there is no bit clock signal on the BCK input. Applying the bit clock signal will cause the TFA9882 to switch from power-down mode to operating mode (provided the word select signal is switched on).

Mute mode is activated when the word select signal is switched off.

The left or right channel is selected by applying the word select signal to, respectively, the WSL or the WSR terminal. The word select terminal not connected should be connected to V_{DDP} or to PCB ground. This simplifies the connection to the V_{DDP} terminal in the WLCSP9 package.

When the word select signal is connected to both terminals, the TFA9882 amplifies the sum of both channels divided by two.

Table 8-1: Mode selection

Mode	Channel	Frequency on BCK	Frequency on WSL	Frequency on WSR	OUTA, OUTB
power-down		0 Hz	don't care	don't care	floating
mute		2.048 MHz to 3.072 MHz	0 Hz	0 Hz	floating
operating	left	2.048 MHz to 3.072 MHz	32 kHz to 48 kHz	0 Hz	switching
	right	2.048 MHz to 3.072 MHz	0 Hz	32 kHz to 48 kHz	switching
	(left + right) / 2	2.048 MHz to 3.072 MHz	32 kHz to 48 kHz	32 kHz to 48 kHz	switching

8.2 I²S format

The TFA9882 supports the Philips I²S standard with a BCK frequency 64 times greater than the sampling rate (64 fs). The bit length can be from 8 bits to 32 bits. Supported I²S sample rates are listed in Table 8-2 while Figure 8-1 illustrates the I²S data transfer format.

Table 8-2: Supported I²S sample rates

f_s (kHz)	WS (kHz)	BCK, 64f_s (MHz)
32	32	2.048
44.1	44.1	2.8224
48	48	3.072

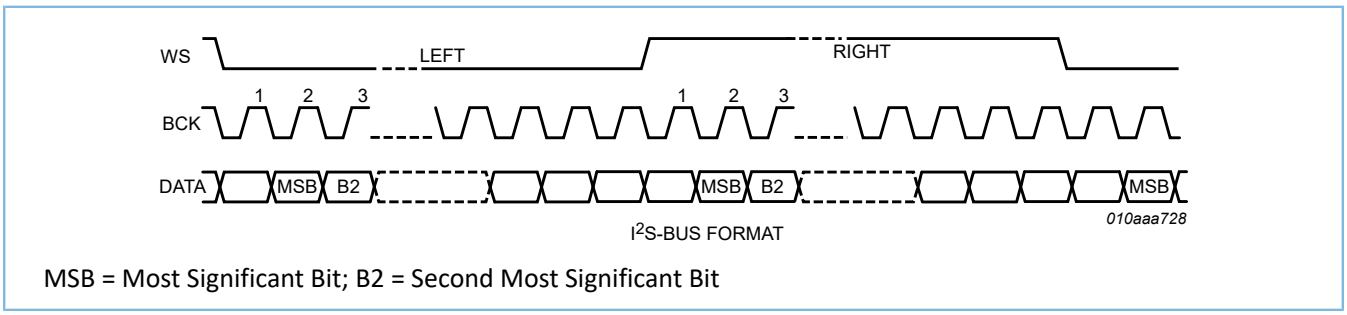


Figure 8-1: I²S format

8.3 Power-up/power-down sequence

The TFA9882 power-up/power-down sequence is shown in Figure 8-2. External power supplies V_{DDP} and V_{DDD} should be within their operating limits before the TFA9882 switches to Operating mode. The TFA9882 should be switched to power-down mode before the power supplies are disconnected or turned off.

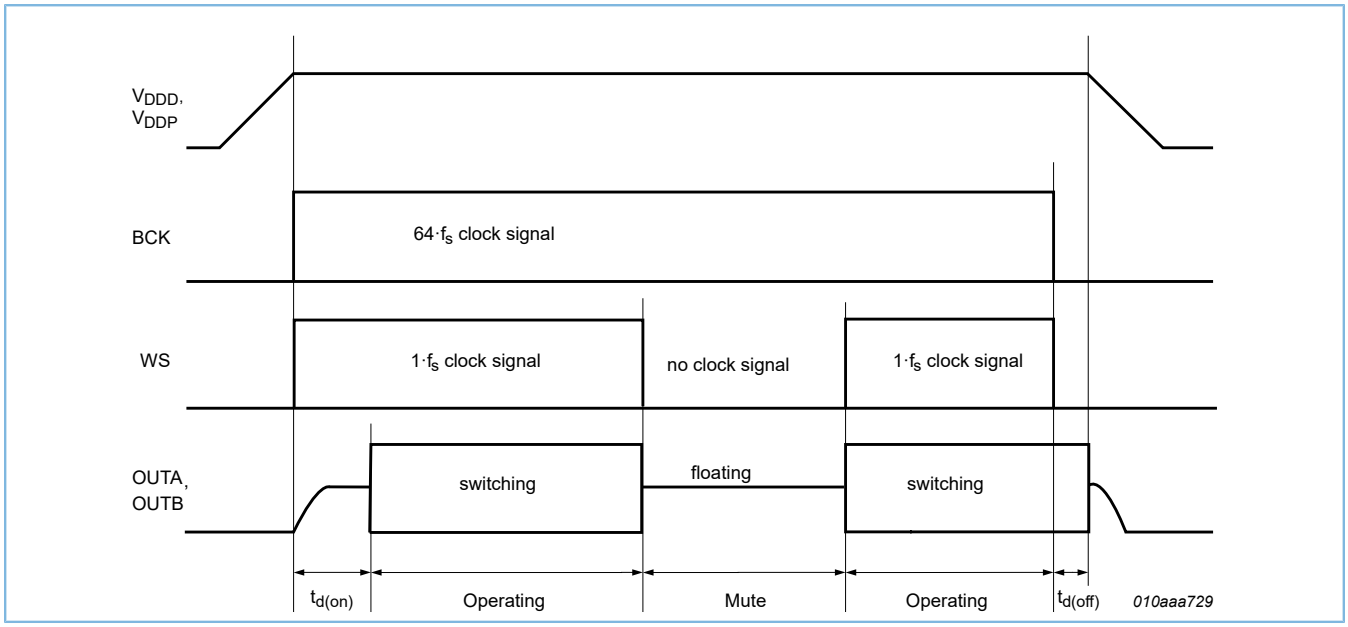


Figure 8-2: Power-up/power-down timing (without control settings)

Table 8-3: Power-up/power-down timing

All parameters are guaranteed for V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time		[2]	-	-	4	ms
$t_{d(off)}$	turn-off delay time		[2]	-	-	5	µs

[1] R_L = load resistance; L_L = load inductance.
[2] Inversely proportional to f_s.

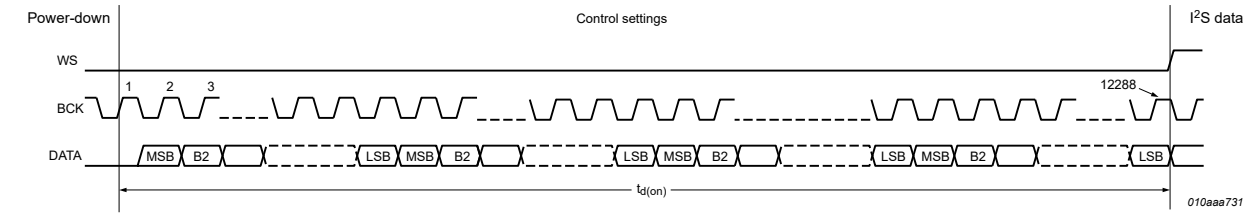
8.4 Control settings

If the device can operate effectively with the default settings, the control settings does not need to be changed.

8.4.1 Control setting pattern recognition

The TFA9882 can detect control settings via the I^2S input. Control settings are selected by transmitting control patterns on the DATA input during the power-up sequence (the first 12288-bit clock cycles). The word select signal (WS) must be switched off during this interval. Figure 8-3 illustrates the control setting sequence. After receiving 128 consecutive

control setting bytes, the TFA9882 activates the appropriate control setting (see the third column of Table 8-4). Control settings remain unchanged in all modes unless control pattern 0xAA is received or the V_{DDD} supply voltage is removed.



LSB = Least Significant Bit; MSB = Most Significant Bit; B2 = Second Most Significant Bit

Figure 8-3: Power-up/power-down timing (without control settings)

Table 8-4: Control settings

Byte	Related bytes	[1]	Control settings
0xD2	0x69/B4/5A/2D/96/4B/A5		clip control on; see Section 8.4.2
0xD4	0x6A/35/9A/4D/A6/53/A9		gain = −3 dB (V_{DDP} = 2.5 V); see Section 8.4.3
0xD8	0x6C/36/1B/8D/C6/63/B1		gain = +3 dB (V_{DDP} = 5.0 V); see Section 8.4.3
0xE1	0xF0/78/3C/1E/0F/87/C3		slope low (EMC); see Section 8.4.4
0xE2	0x71/B8/5C/2E/17/8B/C5		dynamic power stage activation (DPSA) off; see Section 8.4.5
0xAA	0x55		default; no mute, reset settings to default

[1] The related bytes are the bytes from the first column phase shifted by 1, 2, 3, 4, 5, 6 and 7 bits.

8.4.2 Clip control

TFA9882 clip control is off by default. Clip control can be turned on via control setting 0xD2 (see Section 8.4.1). The TFA9882 clips smoothly with clip control on. Output power is at maximum with clip control off.

8.4.3 Gain selection

Signal conversion from digital audio to PWM modulated audio out is independent of supply voltages V_{DDP} and V_{DDD}. At the default gain setting (0 dB), the audio output signal level is just below the clipping point at a supply voltage of 3.6 V at −6 dBFS (peak) input. The TFA9882 supports two further gain settings to support full output power at V_{DDP} = 2.5 V and V_{DDP} = 5.0 V. The gain settings can be selected via control settings 0xD4 and 0xD8 (see Section 8.4.1).

Table 8-5 details the corresponding peak output voltage level at −6 dBFS for the three gain settings.

Table 8-5: Output voltage

All parameters are guaranteed for V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1], L_L = 20 µH[1], f_i = 1 kHz, f_s = 48 kHz, T_{amb} = 25 °C, default settings; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{oM}	peak output voltage	at −6 dBFS (peak) digital input					
		gain = −3 dB, V_{DDP} = 2.5 V, R_L = 4 Ω	[1]	-	2.4	-	V
		gain = 0 dB, V_{DDP} = 3.6 V, R_L = 4 Ω; default	[1]	-	3.4	-	V
		gain = +3 dB, V_{DDP} = 5.0 V, R_L = 8 Ω	[1]	-	4.7	-	V

[1] R_L = load resistance; L_L = load inductance.

8.4.4 PWM slope selection

The rise and fall times of the PWM output edges can be set to one of two values, as detailed in Table 8-6. The default setting is 'slope normal' (10 ns with V_{DDP} = 3.6 V). 'Slope low' is selected via control setting 0xE1 (see Section 8.4.1). This function is implemented to reduce ElectroMagnetic Interference (EMI).

Table 8-6: Slope rise and fall times

Setting	Rise and fall times of the PWM output edges
slope low	40 ns at V_{DDP} = 3.6 V
slope normal; default setting	10 ns at V_{DDP} = 3.6 V

8.4.5 Dynamic power stage activation (DPSA)

The TFA9882 uses DPSA to regulate current consumption in line with the level of the incoming audio stream. This function switches off power stage sections that are not needed, reducing current consumption.

Each of the TFA9882 H-bridge power stages is divided into eight sections. The number of power stage sections activated depends on the level of the incoming audio stream. The thresholds used by the DPSA to determine how many stages are switched on are given in Table 8-7. The DPSA signal is used as a reference signal for switching power stage sections on and off. The DPSA signal will rise in tandem with the rectified audio input signal. When the rectified audio input signal falls, the DPSA decreases with a negative exponential function, as illustrated in Figure 8-4.

The DPSA function can be switched off via control setting 0xE2 (see Section 8.4.1). When DPSA is off, all power stage sections are activated in operating mode.

Table 8-7: DPSA input levels

Setting	Number of power stage sections active
≤ 0.035 × full scale (−29 dBFS)	1

Setting	Number of power stage sections active
> 0.035 × full scale (−29 dBFS)	2
> 0.07 × full scale (−23 dBFS)	4
> 0.105 × full scale (−19.5 dBFS)	8

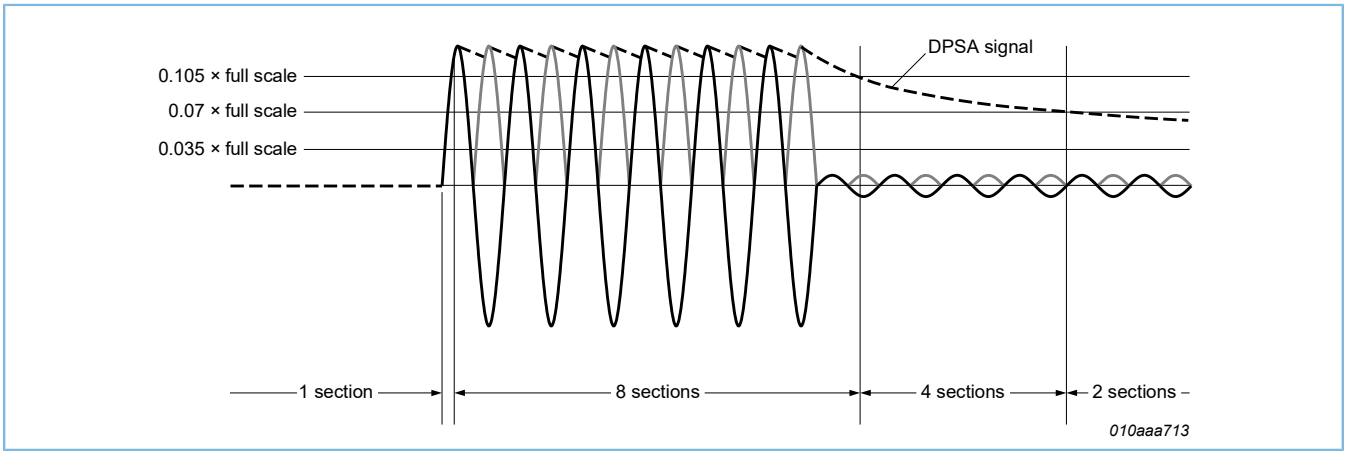


Figure 8-4: Dynamic power stage activation

8.5 High-pass filter

The high-pass filter blocks the DC components in the incoming audio stream. The cut-off frequency, $f_{high(-3dB)}$, is determined by the sampling frequency, f_s, and is defined in Equation 1:

$$f_{high(-3dB)} = \frac{-f_s \cdot \ln(4095/4096)}{2\pi} \quad (1)$$

$f_{high(-3dB)}$ is about 1.9 Hz at a sampling frequency of 48 kHz. The high-pass filter is always enabled.

8.6 PWM frequency

The TFA9882 translates the I^2S input stream into an amplified 3-level PWM output signal. The PWM switching frequency is linearly proportional to the sampling frequency, and is defined in Equation 2.

$$f_{sw(PWM)} = 8 \cdot f_s \quad (2)$$

The PWM switching frequency equals 384 kHz when the sampling frequency is 48 kHz.

8.7 Bandwidth

The TFA9882 output spectrum has a sigma-delta converter characteristic. Figure 8-5 illustrates the output power spectrum of the TFA9882 when it is receiving an I^2S input stream without audio content. The quantization noise is shaped above the band of interest. The band of interest (bandwidth) is determined by the high corner frequency where the noise is increasing. The bandwidth in Figure 8-5 scales with the sampling frequency and is defined in Equation 3:

$$BW = 0.4535 \cdot f_s \quad (3)$$

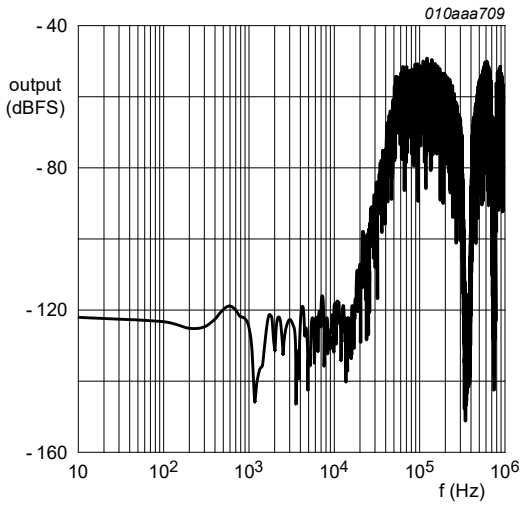


Figure 8-5: Output power spectrum, f_s = 48 kHz

8.8 Protection mechanisms

The following protection circuits are included in the TFA9882:

- Overtemperature protection (OTP)
- Overvoltage protection (OVP)
- Undervoltage protection (UVP)
- Overcurrent protection (OCP)

The reaction of the device to fault conditions differs depending on the protection circuit involved.

8.8.1 Overtemperature protection (OTP)

OTP prevents heat damage to the TFA9882. It is triggered when the junction temperature exceeds $T_{act(th\_prot)}$. When this happens, the output stages are set floating. OTP is cleared automatically via an internal timer (200 ms), after which the output stages will start to operate normally again.

8.8.2 Supply voltage protection mechanisms (UVP and OVP)

UVP is activated, setting the outputs floating, if the supply voltage drops below the undervoltage protection threshold, $V_{P(uvp)}$. This transition will be silent, without pop noise. When the supply voltage rises above $V_{P(uvp)}$ again, the system will be restarted after 200 ms.

OVP is activated, setting the power stages floating, if the supply voltage rises above the overvoltage protection threshold, $V_{P(ovp)}$. The power stages are re-enabled as soon as the supply voltage drops below $V_{P(ovp)}$ again. The system will be restarted after 200 ms.

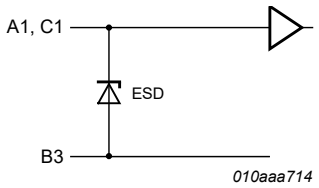
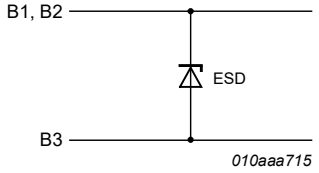
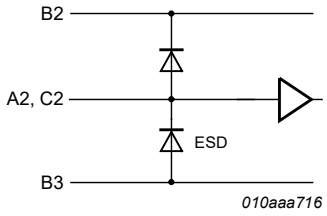
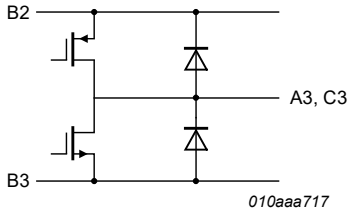
8.8.3 Overcurrent protection (OCP)

OCP will detect a short circuit across the load or between one of the amplifier outputs and one of the supply lines. If the output current exceeds the overcurrent protection threshold ($I_{O(ocp)}$), it will be limited to $I_{O(ocp)}$ while the amplifier outputs are switching (the amplifier is not powered down completely). This is called current limiting. The amplifier can distinguish between an impedance drop at the loudspeaker and a low-ohmic short circuit across the load or to one of the supply lines. The impedance threshold depends on which supply voltage is being used:

- In the event of a short circuit across the load or a short to one of the supply lines, the audio amplifier is switched off completely. It will try to restart again after approximately 200 ms. If the short-circuit condition is still present after this time, this cycle will be repeated. Average dissipation will be low because of the short duty cycle.
- In the event of an impedance drop (e.g. due to dynamic behavior of the loudspeaker), the same protection mechanism will be activated. The maximum output current is again limited to $I_{O(ocp)}$, but the amplifier will not switch off completely (thus preventing audio holes from occurring). This will result in a clipped output signal without artifacts.

9 Internal circuitry

Table 9-1: Internal circuitry

Pin	Symbol	Equivalent circuit
A1	DATA	
C1	BCK	
B1	V_{DDD}	
B2	V_{DDP}	
A2	WSL	
C2	WSR	
A3	OUTB	
C3	OUTA	

10 Limiting values

Table 10-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}		−0.3	+6.0	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		−0.3	+1.95	V
T_j	junction temperature			-	+150	°C
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
V_x	voltage on pin x	pins BCK and DATA		−0.3	+3.6	V
		pins OUTA and OUTB		−0.6	V_{DDP} + 0.6	V
		pins WSL and WSR		−0.6	V_{DDP}	V
V_{ESD}	electrostatic discharge voltage	according to the human body model (HBM)	[1]			
		pins OUTA and OUTB		−8	+8	kV
		any other pin		−2	+2	kV
		according to the charge device model (CDM)	[1]	−500	+500	V
		according to the machine model (MM)	[1]	−200	+200	V

[1] Measurements taken on the TFA9882 in a HVSON10 package (engineering samples) due to handling restrictions with WLCSP9.

11 Thermal characteristics

Table 11-1: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; natural convection			
		JEDEC test board	[1]	128	K/W
		2-layer application board		97	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		[2]	12	K/W

[1] Measured on a JEDEC high K-factor test board (standard EIA/JESD 51-7).
[2] Value depends on where measurement is taken on package.

12 Characteristics

12.1 DC characteristics

Table 12-1: DC characteristics

All parameters are guaranteed for V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C, default slope and gain settings; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{DDP}	power supply current	operating mode with load				
		f_s = 48 kHz	-	1.5	1.7	mA
		f_s = 32 kHz	-	1.38	-	mA
		mute mode	-	1.1	1.25	mA
		power-down mode	-	0.1	1	µA
I_{DDD}	digital supply current	operating mode				
		f_s = 48 kHz	-	1.25	1.4	mA
		f_s = 32 kHz	-	0.85	-	mA
		mute mode				
		f_s = 48 kHz	-	1.1	1.2	mA
		f_s = 32 kHz	-	0.8	-	mA
		power-down mode; BCK = WS = DATA = 0 V	-	2.5	10	µA
Series resistance output power switches						
R_{DSon}	drain-source on-state resistance		-	125	150	mΩ
Amplifier output pins; pins OUTA and OUTB						
$\lvert V_{O(offset)} \rvert$	output offset voltage		-	-	3	mV
BCK, DATA						
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	-	3.6	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDD}$	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance		-	-	3	pF
WSL, WSR						
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	-	V_{DDP}	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDD}$	V
C_i	input capacitance		-	-	3	pF
Protection						
$T_{act(th\_prot)}$	thermal protection activation temperature		130	-	150	°C
$V_{P(ovp)}$	overvoltage protection supply voltage		5.5	-	6.0	V
$V_{P(uvp)}$	undervoltage protection supply voltage		2.3	-	2.5	V
$I_{O(ocp)}$	overcurrent protection output current		1.45	-	-	A

[1] R_L = load resistance; L_L = load inductance.

12.2 AC characteristics

Table 12-2: AC characteristics

All parameters are guaranteed for V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C, default slope and gain settings; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output power						
$P_{o(RMS)}$	RMS output power	THD+N = 1 %				
		V_{DDP} = 3.6 V, f_i = 100 Hz	-	1.4	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz	-	2.7	-	W
		THD+N = 1 %; R_L = 8 Ω; L_L = 44 µH				
		V_{DDP} = 3.6 V, f_i = 100 Hz	-	0.75	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz	-	1.45	-	W
		THD+N = 10 %				
		V_{DDP} = 3.6 V, f_i = 100 Hz	-	1.75	-	W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{DDP} = 5.0 V, f_i = 100 Hz		-	3.4	-	W
		THD+N = 10 %; R_L = 8 Ω; L_L = 44 µH					
		V_{DDP} = 3.6 V, f_i = 100 Hz		-	0.95	-	W
		V_{DDP} = 5.0 V, f_i = 100 Hz		-	1.85	-	W
Performance							
η_{po}	output power efficiency	$P_{o(RMS)}$ = 1.4 W		-	90	-	%
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)}$ = 100 mW		-	0.02	0.1	%
$V_{n(o)}$	output noise voltage	a-weighted		-	24	-	µV
S/N	signal-to-noise ratio	V_{DDP} = 5 V; V_o = 3.4 V (RMS); a-weighted		-	103	-	dB
PSRR	power supply rejection ratio	V_{ripple} = 200 mV; f_{ripple} = 217 Hz		-	85	-	dB
V_{oM}	peak output voltage	at −6 dBFS (peak) digital input:					
		gain = −3 dB; V_{DDP} = 2.5 V		-	2.3	-	V
		gain = 0 dB; V_{DDP} = 3.6 V		3.1	3.3	3.5	V
		gain = +3 dB; V_{DDP} = 5.0 V; R_L = 8 Ω		-	4.7	-	V
Power-up, power-down and propagation times							
$t_{d(on)}$	turn-on delay time		[2]	-	-	4	ms
$t_{d(off)}$	turn-off delay time		[2]	-	-	5	µs
t_{PD}	propagation delay		[2]	-	600	-	µs

[1] R_L = load resistance; L_L = load inductance.
[2] Inversely proportional to f_s.

12.3 I²S timing characteristics

Table 12-3: I²S timing characteristics

All parameters are guaranteed for V_{DDP} = 3.6 V; V_{DDD} = 1.8 V; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C, default slope and gain settings; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency	on pins WSL or WSR	32	-	48	kHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin BCK	-	$64f_s$	-	Hz
t_{su}	set-up time	WS edge to BCK HIGH	10	-	-	ns
		DATA edge to BCK HIGH	10	-	-	ns
t_h	hold time	BCK HIGH to WS edge	10	-	-	ns
		BCK HIGH to DATA edge	10	-	-	ns

[1] R_L = load resistance; L_L = load inductance.

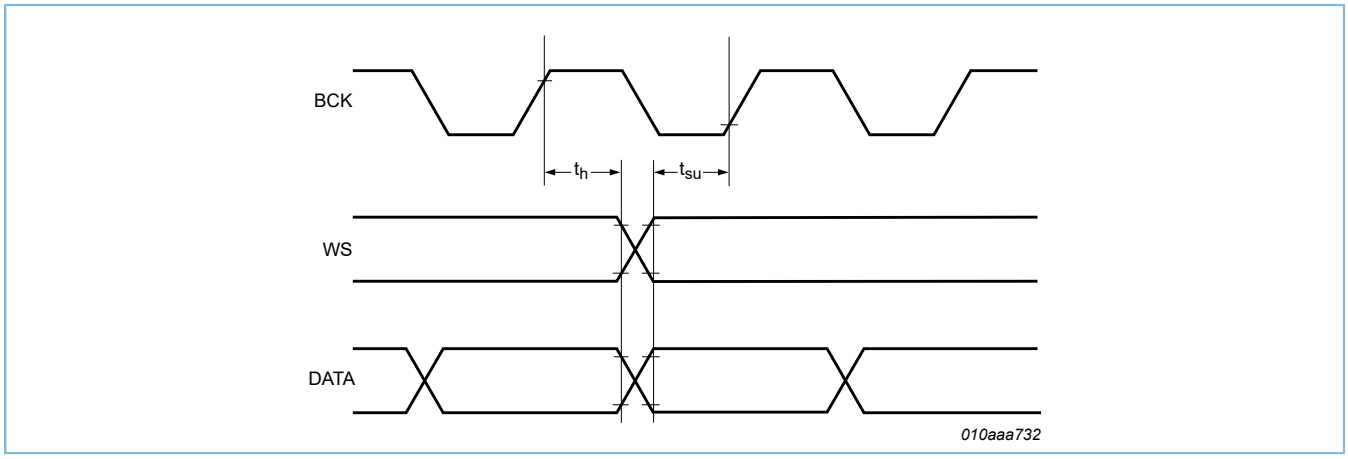


Figure 12-1: I^2S timing

13 Application information

13.1 Electromagnetic compatibility (EMC)

EMC standards define to what degree a (sub)system is susceptible to externally imposed electromagnetic influences and to what degree a (sub)system is responsible for emitting electromagnetic signals, when in standby mode or operating mode.

EMC immunity and emission values are normally measured over a frequency range from 180 kHz up to 3 GHz.

13.1.1 Immunity

A major reason why amplifier devices pick up high frequency signals, and (after detection) manifest these in the device's audio band, is the presence of analog circuits inside the device or in the (sub)system.

The TFA9882 has digital inputs and digital outputs. Comparative tests on a TFA9882-based (sub)system show that the impact of externally imposed electromagnetic signals on the device is negligible in both standby mode and operating mode.

13.1.2 Emissions

Since the TFA9882 is a class-D amplifier with digitally switched outputs in a BTL configuration, it can potentially generate emissions due to the steep edges on the amplifier outputs. External components can be used to suppress these emissions. However, the TFA9882 features built-in slope control to suppress such emissions by reducing the slew rate of the BTL output signals. By reducing the slew rate, the emissions are reduced by some 10 dB when compared with full-speed operation.

13.2 Supply decoupling and filtering

A ceramic decoupling capacitor of between 4.7 µF and 10 µF should be placed close to the TFA9882 for decoupling the V_{DDP} supply. This minimizes the size of the high-frequency current loop, thereby optimizing EMC performance.

13.3 Typical application diagram (simplified)

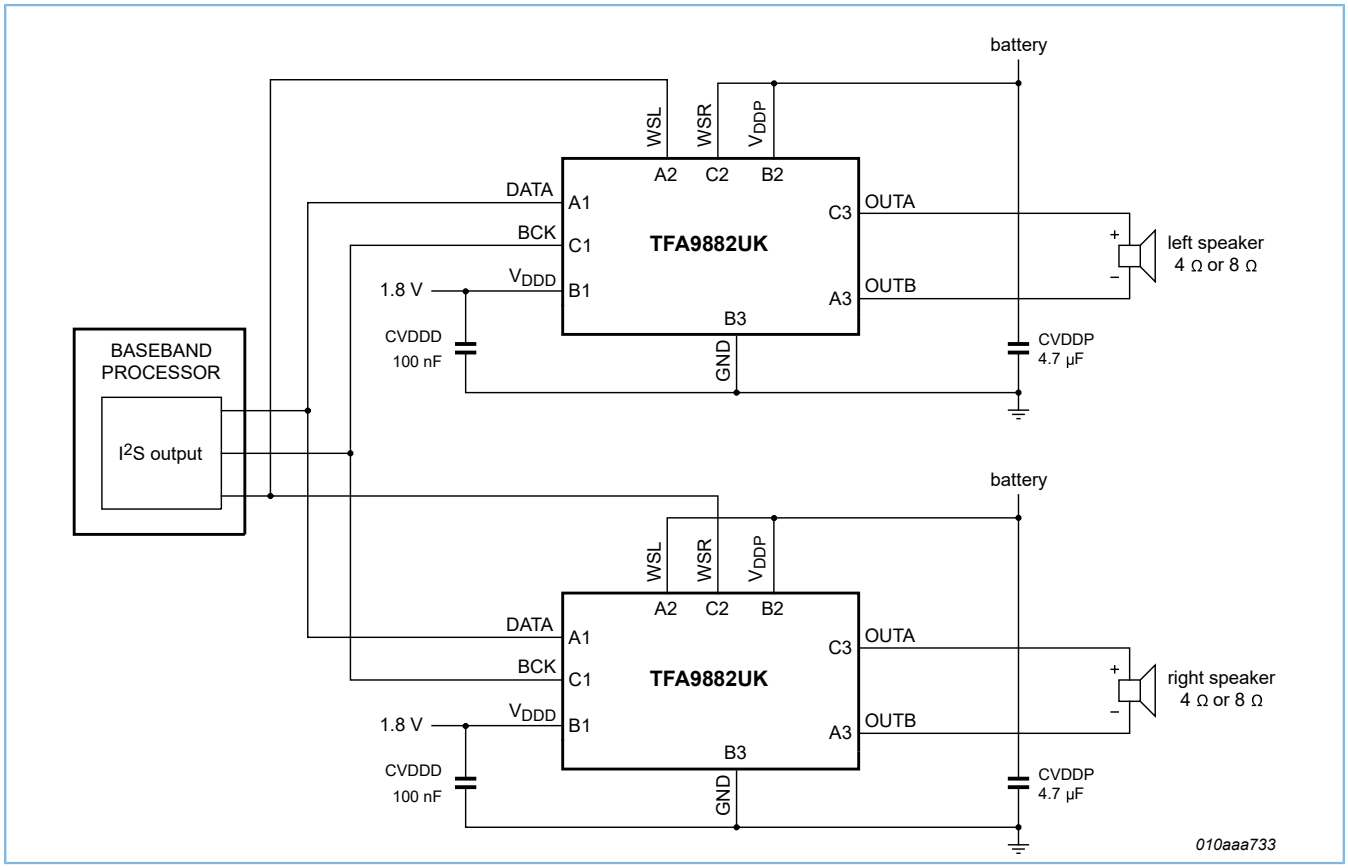
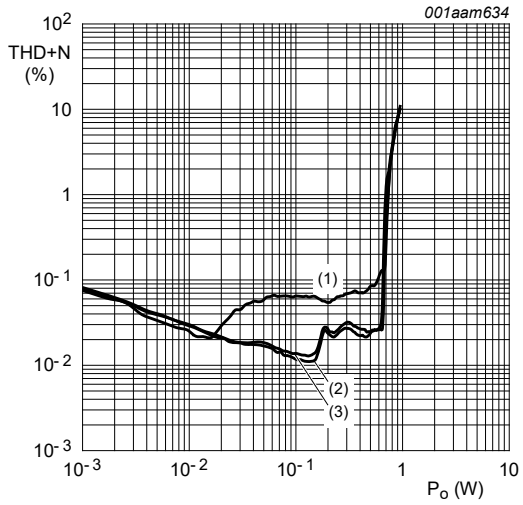


Figure 13-1: Typical stereo application (simplified)

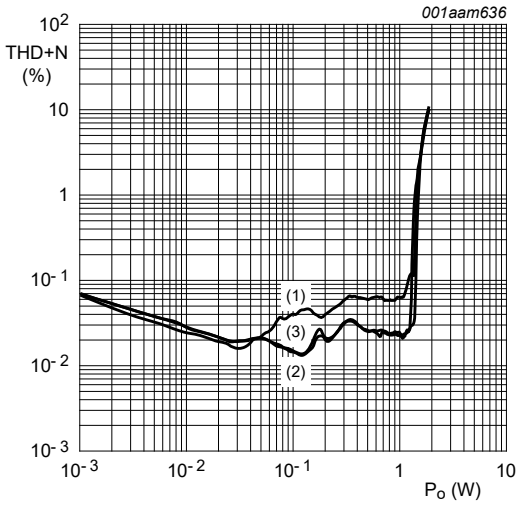
13.4 Curves measured in reference design (demonstration board)

All measurements were taken with V_{DDD} = 1.8 V, f_{clk} = 3.072 MHz, clip control off, DPSA off and slope normal, unless otherwise specified.



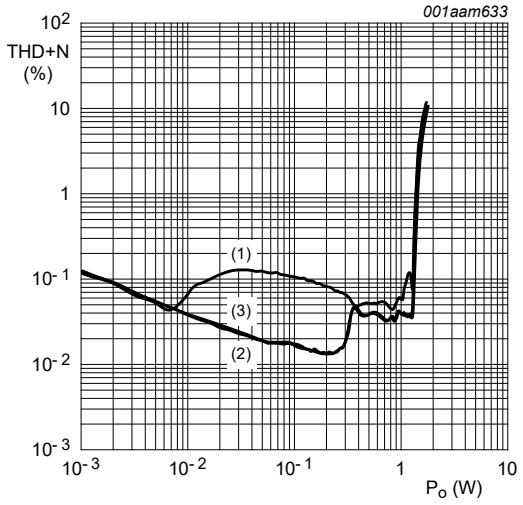
1. f_i = 6 kHz.
2. f_i = 1 kHz.
3. f_i = 100 Hz.

a. V_{DDP} = 3.6 V, R_L = 8 Ω, L_L = 44 µH



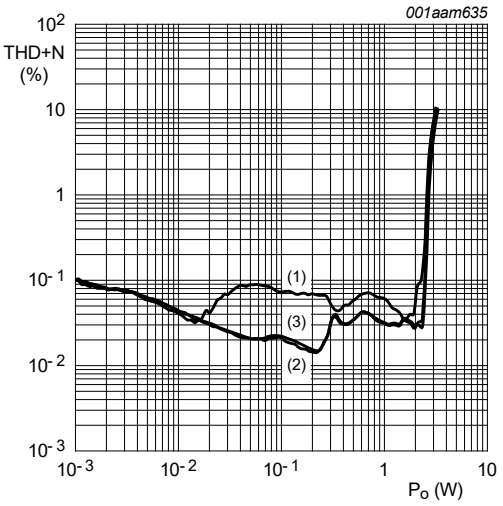
1. f_i = 6kHz.
2. f_i = 1 kHz.
3. f_i = 100 Hz.

b. V_{DDP} = 5 V, R_L = 8 Ω, L_L = 44 µH



1. f_i = 6 kHz.
2. f_i = 1 kHz.
3. f_i = 100 Hz.

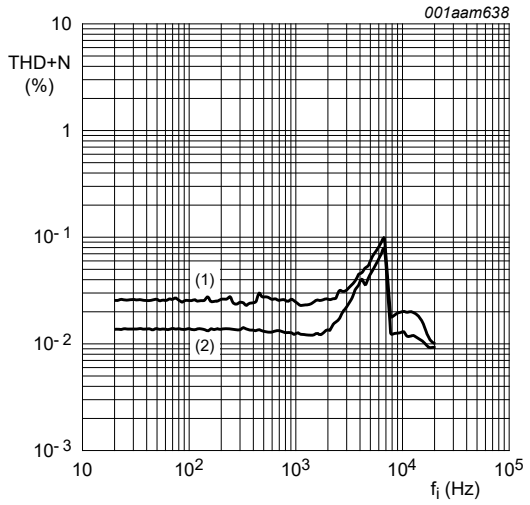
c. V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 µH



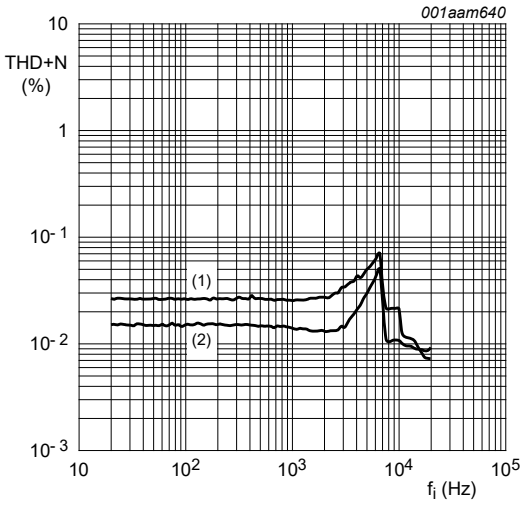
1. f_i = 6 kHz.
2. f_i = 1 kHz.
3. f_i = 100 Hz.

d. V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 µH

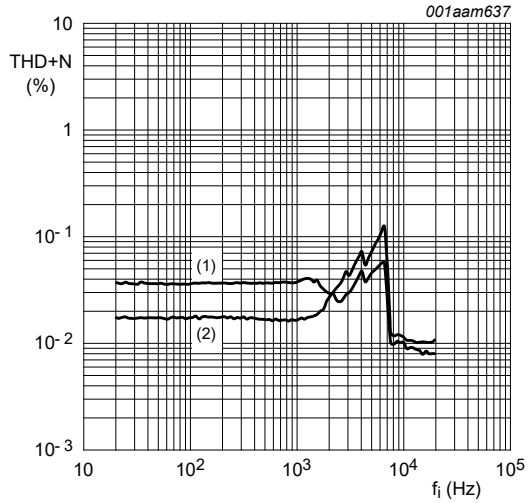
Figure 13-2: THD+N as a function of output power



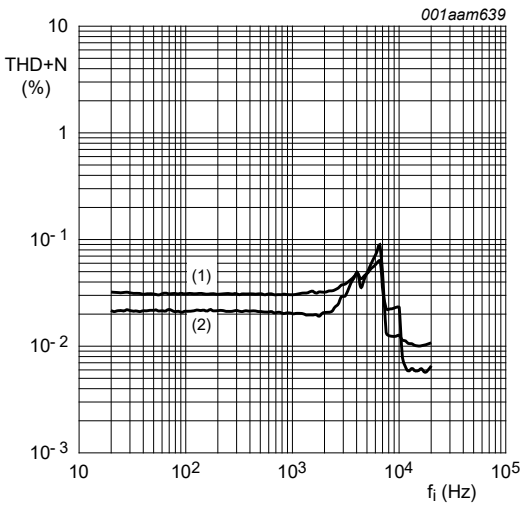
1. P_o = 500 mW
2. P_o = 100 mW
a. V_{DDP} = 3.6 V, R_L = 8 Ω, L_L = 44 µH



1. P_o = 500 mW
2. P_o = 100 mW
b. V_{DDP} = 5 V, R_L = 8 Ω, L_L = 44 µH

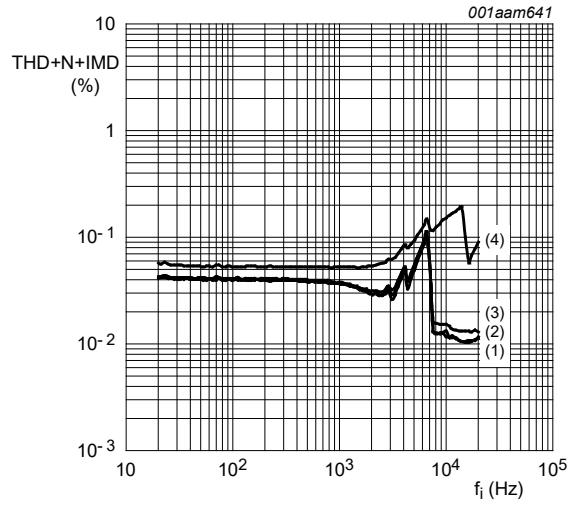


1. P_o = 1 W
2. P_o = 100 mW
c. V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 µH



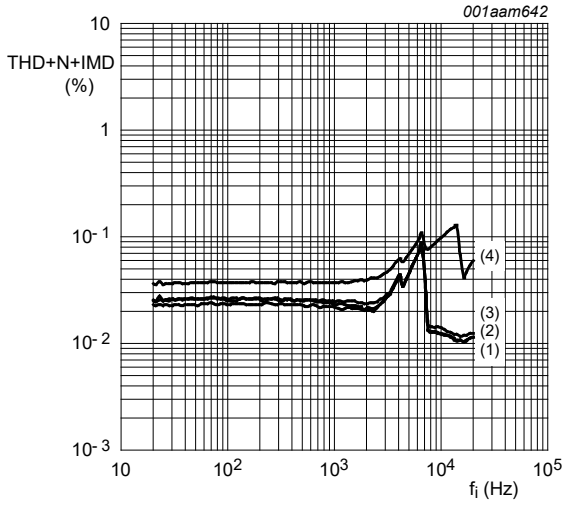
1. P_o = 1 W
2. P_o = 100 mW
d. V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 µH

Figure 13-3: THD+N as a function of frequency



1. V_{ripple} = 0 V (f_{ripple} = 0 Hz)
2. f_{ripple} = 217 Hz
3. f_{ripple} = 1 kHz
4. f_{ripple} = 6 kHz

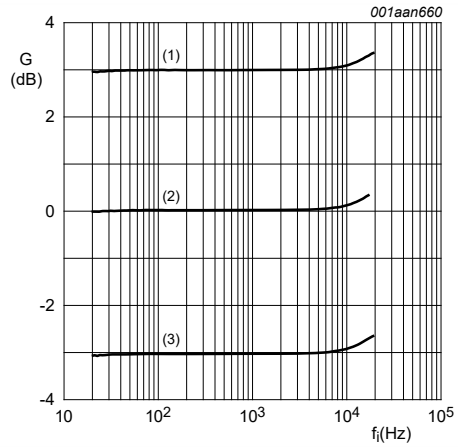
a. V_{DDP} = 3.6 V, R_L = 4 Ω, L_L = 20 µH, P_o = 100 mW
V_{ripple} = 200 mV (RMS)



1. V_{ripple} = 0 V (f_{ripple} = 0 Hz)
2. f_{ripple} = 217 Hz
3. f_{ripple} = 1 kHz
4. f_{ripple} = 6 kHz

b. V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 µH, P_o = 100 mW
V_{ripple} = 200 mV (RMS)

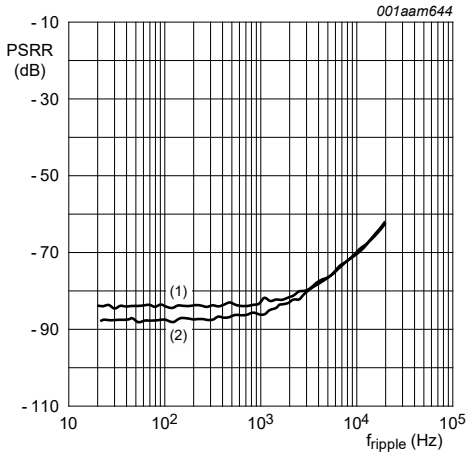
Figure 13-4: THD+N + power supply intermodulation distortion as a function of frequency



1. gain = +3 dB
2. gain = 0 dB
3. gain = −3 dB

VDDP = 3.6 V, RL = 4 Ω, LL = 20 µH, Po = 500 mW

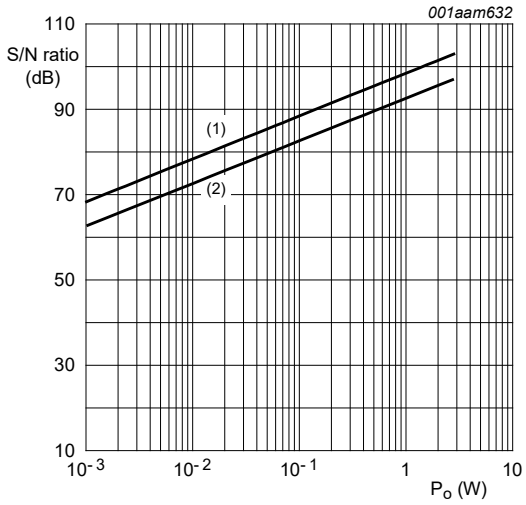
Figure 13-5: Normalized gain as a function of frequency



1. VDDP = 3.6 V
2. VDDP = 5 V

RL = 4 Ω, LL = 20 µH, Vripple = 200 mV (RMS)

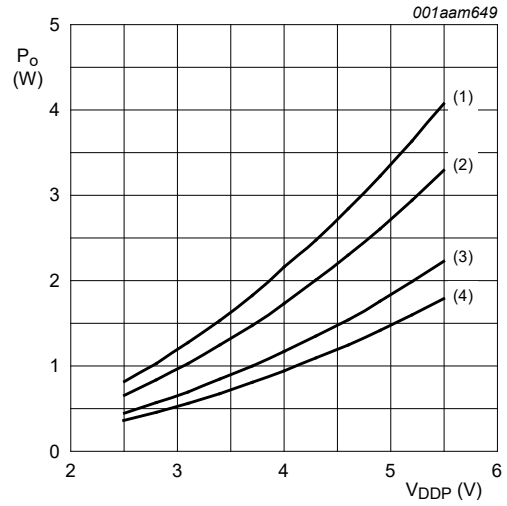
Figure 13-6: PSRR as a function of ripple frequency



1. A-weighted
2. 20 kHz brickwall filter

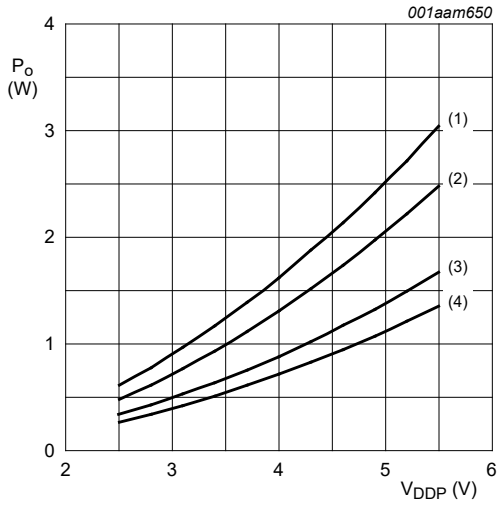
V_{DDP} = 5 V, R_L = 4 Ω, L_L = 20 µH, reference signal: 3.4 V (RMS)

Figure 13-7: S/N ratio as a function of output power



1. THD+N = 10 %, R_L = 4 Ω, L_L = 20 µH
2. THD+N = 1 %, R_L = 4 Ω, L_L = 20 µH
3. THD+N = 10 %, R_L = 8 Ω, L_L = 44 µH
4. THD+N = 1 %, R_L = 8 Ω, L_L = 44 µH

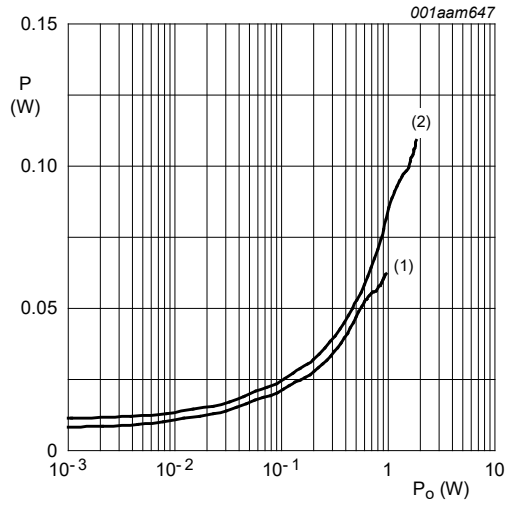
a. f_i =100 Hz, clip control off



1. THD+N = 10 %, R_L = 4 Ω, L_L = 20 µH
2. THD+N = 1 %, R_L = 4 Ω, L_L = 20 µH
3. THD+N = 10 %, R_L = 8 Ω, L_L = 44 µH
4. THD+N = 1 %, R_L = 8 Ω, L_L = 44 µH

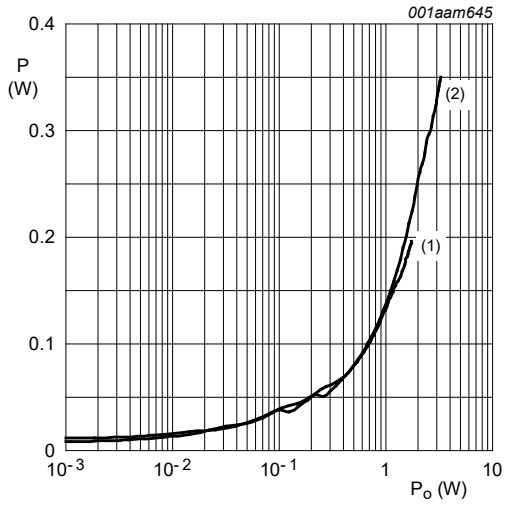
b. f_i = 100 Hz, clip control on

Figure 13-8: Output power as a function of supply voltage



1. V_{DDP} = 3.6 V
2. V_{DDP} = 5 V

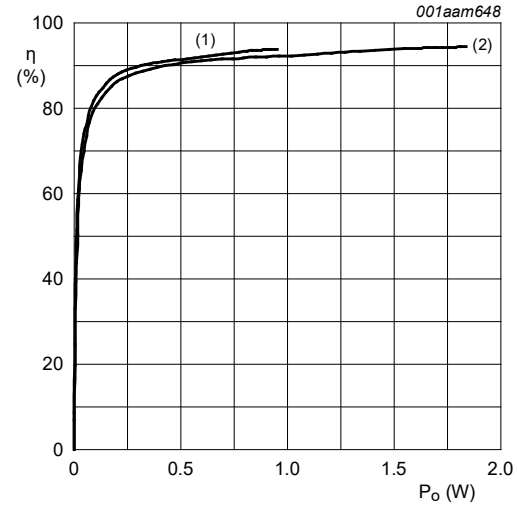
a. R_L = 8 Ω, L_L = 44 µH, f_i = 1 kHz, DPSA on



1. V_{DDP} = 3.6 V
2. V_{DDP} = 5 V

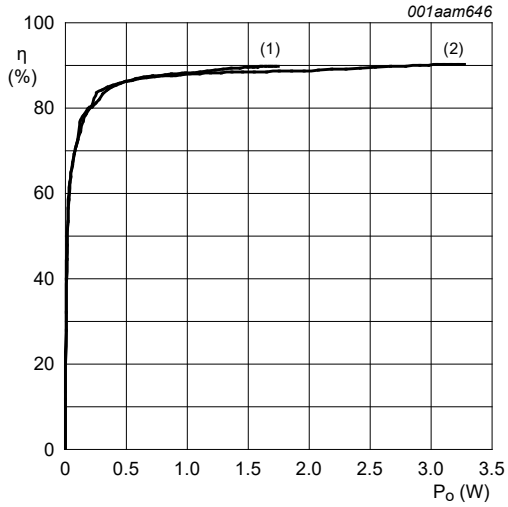
b. R_L = 4 Ω, L_L = 44 µH, f_i = 1 kHz, DPSA on

Figure 13-9: Power dissipation as a function of output power



1. V_{DDP} = 3.6 V
2. V_{DDP} = 5 V

a. R_L = 8 Ω, L_L = 44 µH, f_i = 1 kHz, DPSA on

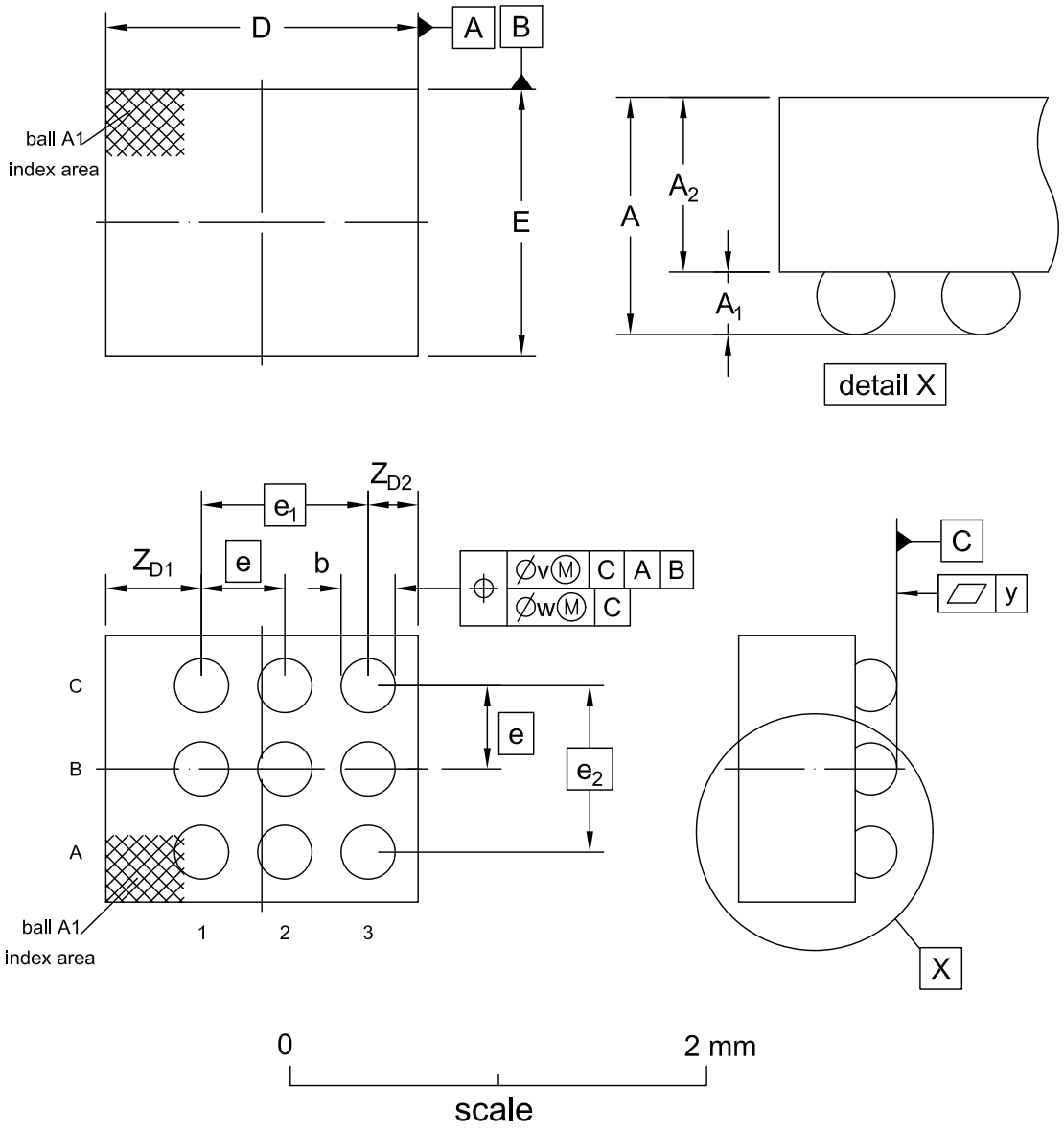


1. V_{DDP} = 3.6 V
2. V_{DDP} = 5 V

b. R_L = 4 Ω, L_L = 44 µH, f_i = 1 kHz, DPSA on

Figure 13-10: Efficiency as a function of output power

14 Package outline



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}
mm	MAX.	0.6	0.23	0.38	0.29	1.53	1.31								
	NOM.		0.20	0.36	0.26	1.50	1.28	0.4	0.8	0.8	0.015	0.04	0.03	0.46	0.24
	MIN.		0.17	0.34	0.23	1.47	1.25								

Figure 14-1: Package outline WLCSP9 (SOT1384-4)

15 Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix Technology WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

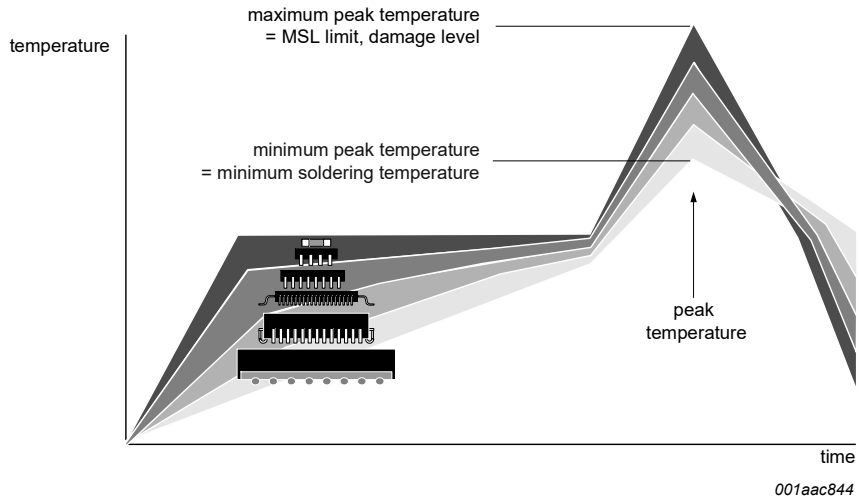
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15-1) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15-1.

Table 15-1: Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering (see Figure 15-1).



MSL: Moisture Sensitivity Level

Figure 15-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to thermal expansion coefficient (TEC) differences between substrate and chip.

15.3.2 Quality of solder joint

When the entire solder land has been wetted by the solder from the bump, a flip-chip joint is considered a good joint. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16 Legal and contact information

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Website: www.goodix.com

17 Revision history

Table 17-1: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9882_DS v 4.2	20200417	Product data sheet	-	TFA9882_DS v 4.1
Modifications:	• Added version number to the ordering information.			
TFA9882_DS v 4.1	20200221	Product data sheet	-	TFA9882_DS v 4.0
Modifications:	• Description of type number, package outline and doc ID amended.			
TFA9882_DS v 4.0	20200121	Product data sheet	-	TFA9882_DS v.3
Modifications:	• Updated document format based on Goodix template.			
TFA9882_DS v.3	20190318	Product data sheet	-	TFA9882_DS v.2
Modifications:	• Table 10-1: text in table header amended; max. limiting value for parameter V_{DDP} changed • Table 12-1: value of parameter V_{IH} (max) for pins WSL and WSR changed • Figure 14-1 amended • Figure 14-1 Package outline updated • Table 5-1: Description field updated.			
TFA9882_DS v.2	20110420	Product data sheet	-	TFA9882_DS v.1
TFA9882_DS v.1	20110331	Preliminary data sheet	-	-