



TFA9892_SDS

**12 V Boosted Audio System with Adaptive Sound Maximizer and
Speaker Protection**

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1 General description

The TFA9892 is a high efficiency class-D audio amplifier with a sophisticated speaker boost and protection algorithm. It can deliver 13.2 W peak output power into an 8 Ω speaker at a supply voltage of 4.0 V. The internal boost converter raises the supply voltage to 12 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9892 maximizes acoustic output while ensuring diaphragm displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker. An integrated Multiband Dynamic Range Compressor (MDRC) allows the speaker to operate at the highest possible power rating without suffering physical damage.

Unlike competing solutions, the adaptive sound maximizer algorithm uses feedback to accurately calculate both the temperature and the excursion, allowing the TFA9892 to adapt to changes in the acoustic environment.

Internal intelligent DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. This maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption in combination with a Pulse Frequency Modulation (PFM) scheme.

The device can be configured to drive either a hands-free speaker (4 Ω to 8 Ω) for audio playback, or a receiver speaker (32 Ω) for handset playback, allowing it to be embedded in platforms that support either or both options. The maximum output power, gain, and noise levels are lower in the Handset Call use case than in the Hands-free Call use case.

The TFA9892 also incorporates advanced battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which could cause a system undervoltage. The advanced processor minimizes the impact of a falling battery voltage on the audio quality by preventing distortion as the battery discharges.

Because it has a digital input interface, the TFA9892 features low RF susceptibility. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection. The TDM/I²S audio interface provides a wide range of settings for multiple slots and Digital I/O. The settings are communicated via an I²C-bus interface.

The device also provides the speaker with robust protection against ESD damage. In a typical application, no additional components are needed to withstand a 15 kV discharge on the speaker.

The TFA9892 is available in a 49-bump WLCSP (Wafer Level Chip-Size Package) with a 400 μ m pitch.

2 Features and benefits

- Output power: 6.6 W into 8 Ω at 4.0 V supply voltage (THD = 1 %)
- Wide range of speakers: 4 Ω to 8 Ω for hands-free mode and 16 Ω , 32 Ω for handset one
- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
 - Fully embedded software, no additional license fee or porting required
 - Total integrated solution that includes DSP, ClassD amplifier, DC-to-DC converter
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit
- Multiband dynamic range compressor (DRC) allows independent control of up to three frequency bands
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Four TDM/I²S inputs output (I/O) to support two audio sources or one PDM input and inter-chip communications
- Speaker current and voltage monitoring via TDM for Acoustic Echo Cancellation (AEC) at the host
- Option to route TDM input direct to TDM output to allow a second TDM output slave device to be used in combination with the TFA9892
- Sample frequencies f_s from 16 kHz to 48 kHz supported in TDM/I2S mode; speaker-boost and protection algorithm sample rate up to 48 kHz.
- 3 bit clock/word select ratios supported (32x, 48x, 64x) in TDM/I2S mode
- I²C-bus control interface (400 kHz)
- 12 V DC-to-DC converter using PFM mode
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Fully short-circuit proof across the load and to the supply lines
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- 15 kV system-level ESD protection without external components
- 'Pop noise' free at all mode transitions

3 Applications

- Mobile phones
- Tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- MP3 players and portable media players
- Small audio systems

4 Quick reference data

Table 4-1: Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------|--|------|------|------|---------------|
| V_{BAT} | battery supply voltage | on pin VBAT | 2.7 | - | 5.5 | V |
| V_{DDD} | digital supply voltage | on pin VDDD | 1.65 | 1.8 | 1.95 | V |
| I_{BAT} | battery supply current | on pin V_{BAT} and in DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive Boost mode (no output signal, $V_{BAT} = 3.6\text{ V}$, $V_{DDD} = 1.8\text{ V}$) | - | 2.45 | - | mA |
| | | Power-down mode | - | 1 | 5 | μA |
| I_{DDD} | digital supply current | on pin VDDD; Operating mode; no audio stream at the input; DSP enabled; SpeakerBoost activated | - | 20 | - | mA |
| | | Operating mode; no audio content; DSP bypassed | - | 4.5 | - | mA |
| | | on pin VDDD; Power-down mode no external CLK or Data provided | - | 15 | - | μA |
| | | on pin VDDD; Power-down mode; internal oscillator enabled; no external CLK or Data provided | - | 50 | - | μA |
| $P_{O(AV)}$ | average output power | THD+N = 1 %; $R_L = 8\ \Omega$; $V_{BAT} = 4.0\text{ V}$ | - | 6.6 | - | W |

5 Ordering information

Table 5-1: Ordering information

| Type number | Package | | |
|---------------|---------|--|-----------|
| | Name | Description | Version |
| TFA9892AUK/N1 | WLCSP49 | wafer level chip-scale package; 49 bumps; 3.13 × 3.63 × 0.5 mm | SOT1444-8 |

6 Block diagram

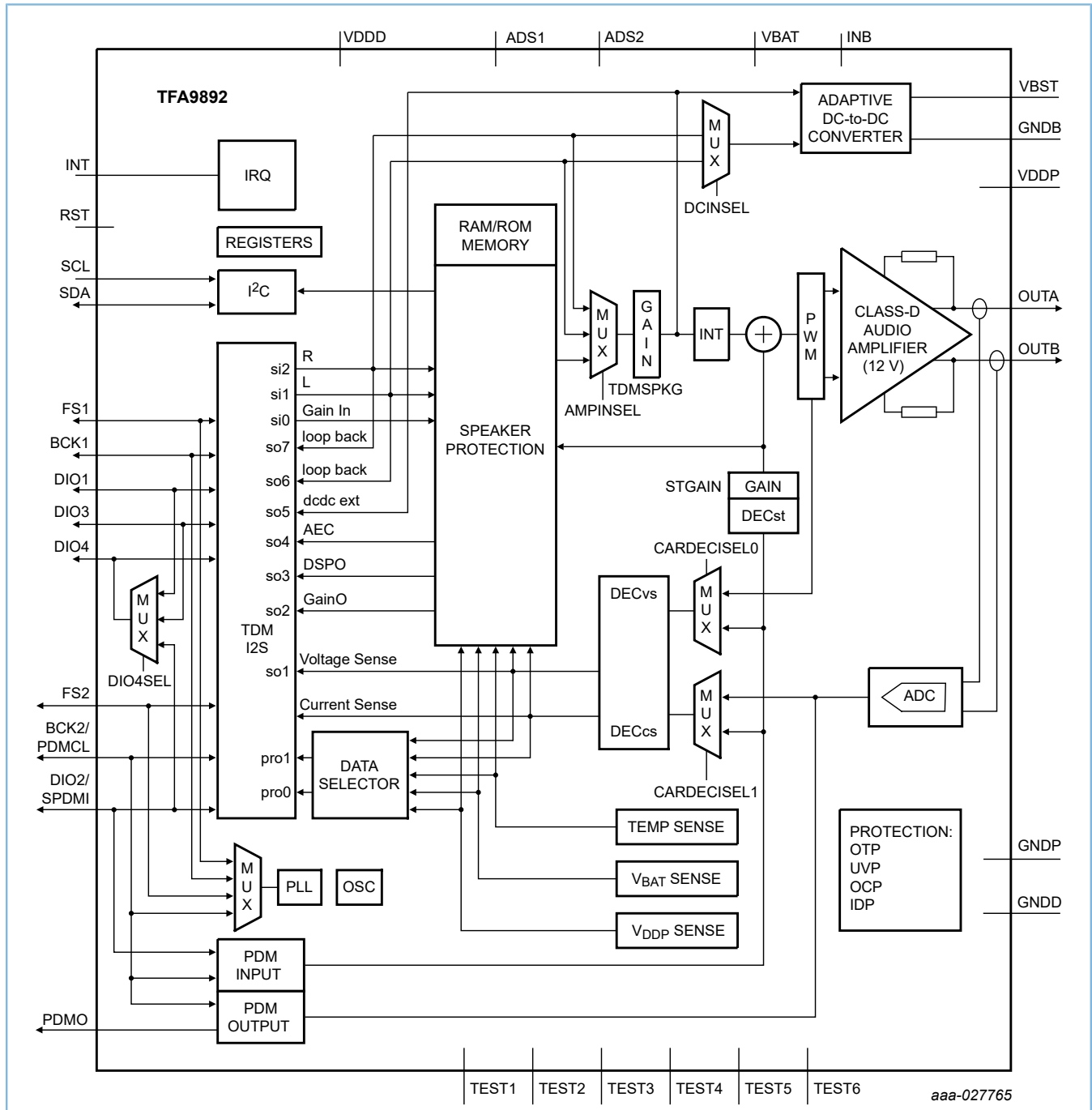


Figure 6-1: Block diagram

7 Pinning information

7.1 Pinning

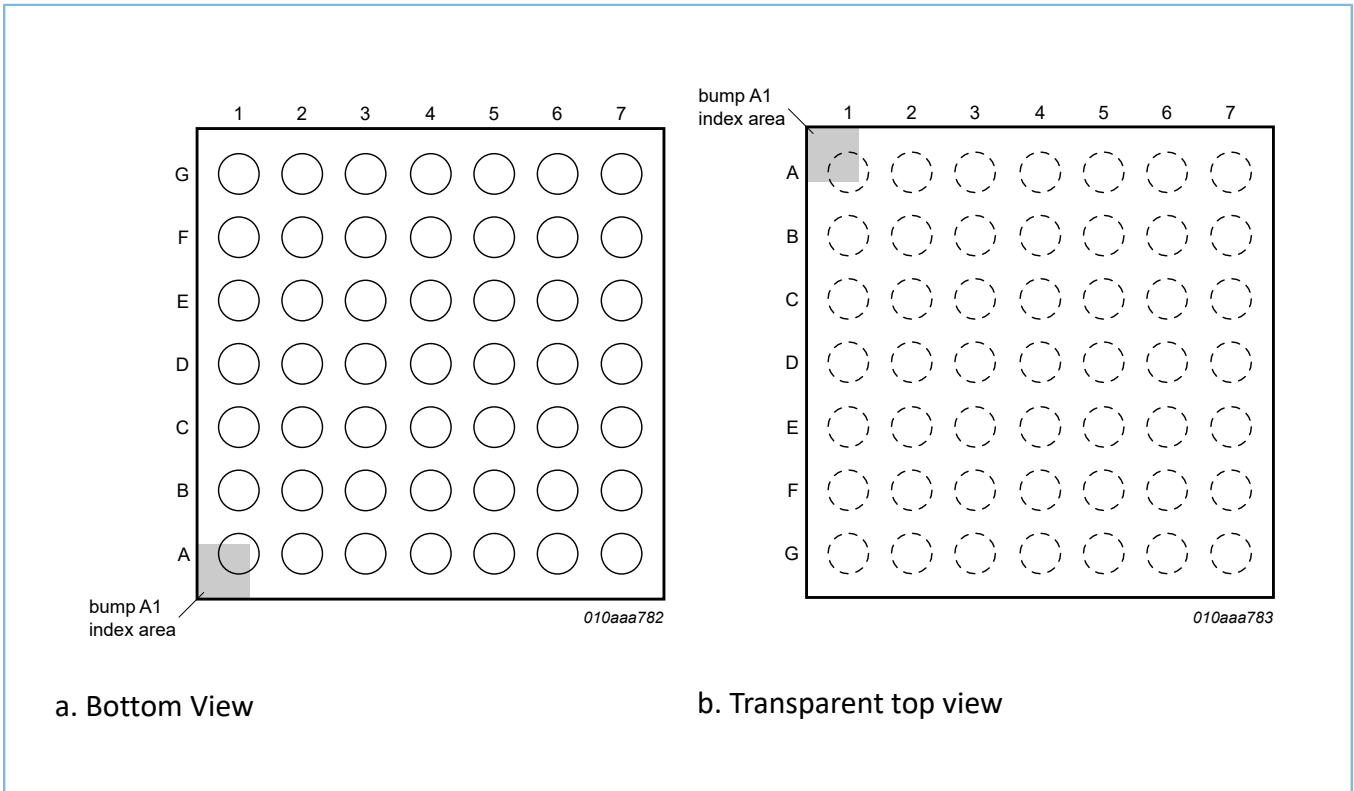


Figure 7-1: Bump configuration

| | | | | | | | |
|---|-----------------|-------|-------|-------|------|------|------|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| A | FS1 | DIO1 | DIO4 | INT | GNDD | OUTB | VDDP |
| B | BCK1 | GNDD | DIO3 | RST | GNDD | GNDD | VDDP |
| C | DIO/SPD MI | GNDD | TEST3 | TEST2 | GNDD | OUTA | VDDP |
| D | FS2 | GNDD | TEST4 | TEST1 | GNDD | OUTA | OUTA |
| E | BCK2/PDM CLK | SPDMO | TEST5 | TEST6 | GNDB | INB | VBST |
| F | SDA | ADS1 | ADS2 | GNDD | GNDB | INB | VBST |
| G | SCL | VBAT | VDDD | GNDD | GNDB | INB | VBST |

aaa-027680

1. Transparent top view

Figure 7-2: Bump mapping

Table 7-1: Pinning

| Symbol | Pin | Type | Description |
|--------|-----|------|-----------------------------------|
| FS1 | A1 | I | digital audio Frame Sync for DIO1 |
| DIO1 | A2 | I/O | digital audio interface DIO1 |
| DIO4 | A3 | I/O | digital audio data in / out DIO4 |
| INT | A4 | O | interrupt output; open if unused |
| GNDD | A5 | P | digital ground |
| OUTB | A6 | O | inverting output |
| VDDP | A7 | P | power supply voltage |
| BCK1 | B1 | I | digital audio bit clock DIO1 |
| GNDD | B2 | P | digital ground |
| DIO3 | B3 | I | digital audio data in/out DIO3 |
| RST | B4 | I | reset input |

| Symbol | Pin | Type | Description |
|-----------------|-----|------|--|
| GNDP | B5 | P | power ground |
| GNDP | B6 | P | power ground |
| VDDP | B7 | P | power supply voltage |
| DIO2/ SPDMI | C1 | I/O | digital audio data in/out DIO2 / SPDM data input |
| GNDD | C2 | P | digital ground |
| TEST3 | C3 | O | test signal input 3; for test purposes only, connect to PCB ground |
| TEST2 | C4 | O | test signal input 2; for test purposes only, connect to PCB ground |
| GNDD | C5 | P | digital ground |
| OUTA | C6 | O | non-inverting output |
| VDDP | C7 | P | power supply voltage |
| FS2 | D1 | I | digital audio word select for DIO2 |
| GNDD | D2 | P | digital ground |
| TEST4 | D3 | O | test signal input 4; for test purposes only, connect to PCB ground |
| TEST1 | D4 | O | test signal input 1; for test purposes only, connect to PCB ground |
| GNDD | D5 | P | digital ground |
| OUTA | D6 | - | non-inverting output ^[1] |
| OUTA | D7 | - | non-inverting output ^[1] |
| BCK2/ PDMCLK | E1 | I | digital audio bit clock DIO2 or PDM clock input |
| SPDMO | E2 | O | PDM output; output open if unused |
| TEST5 | E3 | O | test signal input 5; for test purposes only, connect to PCB ground |
| TEST6 | E4 | O | test signal input 6; for test purposes only, connect to PCB ground |
| GNDB | E5 | P | boosted ground |
| INB | E6 | P | DC-to-DC boost converter input |
| VBST | E7 | O | boosted supply voltage output |
| SDA | F1 | I/O | I ² C-bus data input/output |
| ADS1 | F2 | I | address select input 1 |
| ADS2 | F3 | I | address select input 2 |
| GNDD | F4 | P | digital ground |

| Symbol | Pin | Type | Description |
|--------|-----|------|------------------------------------|
| GNDB | F5 | P | boosted ground |
| INB | F6 | P | DC-to-DC boost converter input |
| VBST | F7 | O | boosted supply voltage output |
| SCL | G1 | I | I ² C-bus clock input |
| VBAT | G2 | P | battery supply voltage sense input |
| VDDD | G3 | P | digital supply voltage |
| GNDD | G4 | P | digital ground |
| GNDB | G5 | P | boosted ground |
| INB | G6 | P | DC-to-DC boost converter input |
| VBST | G7 | O | boosted supply voltage output |

[1] Is used to simplify routing to OUTA

8 Functional description

The TFA9892 is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost protection algorithm. [Figure 6-1](#) is a block diagram of the TFA9892.

A SpeakerBoost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of ± 10 °C. Furthermore, advanced signal processing ensures the audio quality remains acceptable at all times.

The protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

Output sound pressure levels are boosted within given mechanical, thermal and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high quality music in quiet environments.

The frequency response of the TFA9892 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 10 are processed with 24-bit single precision.

At low battery voltage levels, the gain is automatically reduced to limit battery current. The output volume can be controlled by the SpeakerBoost protection algorithm or by the host application (external). In the latter case, the boost features of the SpeakerBoost protection algorithm must be disabled to avoid neutralizing external volume control.

The SpeakerBoost protection algorithm output is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the SpeakerBoost protection algorithm. It switches to Follower mode ($V_{BST} = V_{BAT}$; no boost) when the audio output voltage is lower than the battery voltage. Next to adaptive DC to DC a PFM mode is selected when the requested output current is low. The adaptive boost and PFM mode ensures a high efficiency ClassHD Amplifier.

It contains four TDM/I2S input/output (DIO) ports. These ports can be selected as an input or an output on demand. i.e. DIO1 and DIO2, can be selected as the audio input stream. DIO3 is provided to support stereo applications, while DIO4 can be used to provide stereo AEC as well. DIO1, DIO3 and DIO4 are clocked by FS1 and BCK1, while DIO2 is clocked by FS2 and BCK2; see [Figure 6-1](#)).

DIO 3, 4 can be as well configured to transmit the DSP output signal, amplifier output current and voltage information, or amplifier gain information. The gain information can be used to facilitate communication between two devices in stereo applications.

A 'pass-through' option allows one of the DIO1, 2, 3 as input to be connected directly to the DIO4 output. The pass-through option is provided to allow an output slave device (e.g. a CODEC), connected in parallel with the TFA9892, to be routed directly to the audio host via DIO4 output.

9 Limiting values

Table 9-1: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------------|--|---------------------|-------|------|
| V _x | voltage on pin x | on pin VBAT | -0.3 | +6 | V |
| | | on pins VBST, VDDP | -0.3 | +12.4 | V |
| | | on pin INB, OUTA, OUTB | ^[1] -0.3 | +13.4 | V |
| | | on pin VDDD | -0.3 | +2.5 | V |
| | | on SCL, SDA, DIO1, DIO2, DIO3, DIO4 | -0.3 | +2.5 | V |
| T _j | junction temperature | | -40 | +150 | °C |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| V _{ESD} | electrostatic discharge voltage | according to Human Body Model (HBM) | -2 | +2 | kV |
| | | according to Charge Device Model (CDM) | -500 | +500 | V |

[1] Using a Goodix demo board with a 1 mm wire/PCB track length on pin INB, AC pulses up to 18 V and -9 V can be observed without causing any damage as these spikes only partly penetrate the device (which is protected by internal clamp circuits).

10 Thermal characteristics

Table 10-1: Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|---------------------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | 4-layer application board | 35 | K/W |

11 Characteristics

11.1 DC characteristics

Table 11-1: DC characteristics

All parameters are guaranteed for $V_{BAT} = 3.6\text{ V}$; $V_{DDD} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 12\text{ V}$, adaptive boost mode; $L_{BST} = 1\text{ }\mu\text{H}^{[1]}$; $R_L = 8\text{ }\Omega^{[1]}$; $L_L = 40\text{ }\mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|---------------------|------|-----------------|---------------|
| V_{BAT} | battery supply voltage | on pin VBAT | 2.7 | - | 5.5 | V |
| I_{BAT} | battery supply current | on pin VBAT and in DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive Boost mode (no output signal, $V_{BAT} = 3.6\text{ V}$; $V_{DDD} = 1.8\text{ V}$) | - | 2.45 | - | mA |
| | | Power-down mode | - | 1 | 5 | μA |
| V_{DDP} | power supply voltage | on pin VDDP | 2.7 | - | 12.2 | V |
| V_{DDD} | digital supply voltage | on pin VDDD; Brown out detector (BOD) disabled. | ^[2] 1.65 | 1.8 | 1.95 | V |
| I_{DDD} | digital supply current | on pin VDDD; Operating mode; no audio stream at the input; DSP enabled; SpeakerBoost activated | - | 20 | - | mA |
| | | Operating mode; no audio content; DSP bypassed | - | 4.5 | - | mA |
| | | Power-down mode | - | 15 | - | μA |
| | | Power-down mode; internal oscillator enabled | - | 50 | - | μA |
| Pins DIO1,2,3,4, BCK1, FS1, BCK2, FS2, ADS1, ADS2, SCL, SDA | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDD}$ | - | V_{DDD} | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DDD}$ | V |
| C_{in} | input capacitance | | ^[3] - | - | 3 | pF |
| I_{LI} | input leakage current | 1.8 V on input pin | - | - | 0.1 | μA |
| Pins DIO1,2,3,4, SPDMI, INT, push-pull output stages | | | | | | |
| V_{OH} | HIGH-level output voltage | $I_{OH} = 4\text{ mA}$ | - | - | $V_{DDD} - 0.4$ | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|------|-----|------------------------|------|
| V _{OL} | LOW-level output voltage | I _{OL} = 4 mA | - | - | 400 | mV |
| Pins SDA, open drain outputs, external 10 kΩ resistor to V_{DDD} | | | | | | |
| V _{OH} | HIGH-level output voltage | I _{OH} = 4 mA | - | - | V _{DDD} - 0.4 | V |
| V _{OL} | LOW-level output voltage | I _{OL} = 4 mA | - | - | 400 | mV |
| Pins OUTA, OUTB | | | | | | |
| R _{DSon} | drain-source on-state resistance | Amplifier Active, NMOS + PMOS V _{DDP} = 12 V | - | 600 | - | mΩ |
| Protection | | | | | | |
| T _{act(th_prot)} | thermal protection activation temperature | | 130 | - | 150 | °C |
| V _{uvp(VBAT)} | undervoltage protection voltage on pin VBAT | | 2.3 | - | 2.5 | V |
| I _{O(ocp)} | overcurrent protection output current | | 2 | - | - | A |
| DC-to-DC converter | | | | | | |
| V _{BST} | maximum voltage on pin VBST | Maximum boost voltage setting | 11.8 | 12 | 12.2 | V |

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).

[2] If BOD is enabled min V_{DDD} range goes to 1.7 V

[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

11.2 AC characteristics

Table 11-2: AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 12 V, adaptive boost mode; L_{BST} = 1 μH^[1]; R_L = 8 Ω^[1]; L_L = 40 μH^[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------|--|-----|-----|-----|------|
| Amplifier output power | | | | | | |
| P _{O(AV)} | average output power | Hands-free speaker THD+N = 1 %; V _{BAT} = 4 V | | | | |
| | | R _L = 8 Ω; V _{BST} = 12 V | | 6.6 | | W |
| | | R _L = 6 Ω; V _{BST} = 10 V | | 6.6 | | W |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--|-----|-----|-----|-----------------|
| | | $R_L = 4 \Omega$; $V_{BST} = 8.5 \text{ V}$ | | 6.7 | | W |
| | | Hands-free speaker THD+N = 10 %; $V_{BAT} = 4 \text{ V}$ | | | | |
| | | $R_L = 8 \Omega$; $V_{BST} = 12 \text{ V}$ | | 8 | | W |
| | | Handset speaker THD+N = 1 %; $V_{BST} = 12 \text{ V}$; $V_{BAT} = 4 \text{ V}$ | | 2 | | W |
| Amplifier output; pins OUTA and OUTB | | | | | | |
| $ V_{O(\text{offset})} $ | output offset voltage | absolute value | - | - | 0.5 | mV |
| Amplifier performance | | | | | | |
| η_{po} | output power efficiency | $P_{o(\text{RMS})} = 2.5 \text{ W}$; including DC-to-DC converter; 100 Hz audio signal | [2] | - | 80 | - % |
| THD+N | total harmonic distortion-plus-noise | $P_{o(\text{RMS})} = 100 \text{ mW}$; $R_L = 8 \Omega$; $L_L = 44 \mu\text{H}$ | [1] | - | - | 0.1 % |
| $V_{n(o)}$ | output noise voltage | A-weighted; no output signal; CoolFlux DSP bypassed; Handset mode; BCK clock jitter < 1 ns (PLL locked on BCK) | | - | 16 | - μV |
| DR | dynamic range | $V_O = 10 \text{ V}$ (peak); A-weighted | | - | 115 | - dB |
| S/N | signal-to-noise ratio | $V_O = 10 \text{ V}$ (peak); A-weighted | | - | 100 | - dB |
| PSRR | power supply rejection ratio | $V_{\text{ripple}} = 200 \text{ mV}$ (RMS); $f_{\text{ripple}} = 217 \text{ Hz}$ | | - | 75 | - dB |
| f_{sw} | switching frequency | directly coupled to the TDM FS input frequency | | 256 | - | 384 kHz |
| $G_{(I2S-V_O)}$ | I ² S to V _O gain | Coolflux DSP bypassed, measured at input level -12 dBFS; TDMSPKG = 0 dB | | - | 21 | - dB |
| V_{POP} | pop noise voltage | At mode transition and gain change | | | 2 | mV |
| R_L | load resistance | | 4 | 8 | 32 | Ω |
| C_L | load capacitance | | - | - | 200 | pF |
| Amplifier power-up, power-down and propagation delays | | | | | | |
| $t_{d(\text{on})}$ | turn-on delay time | PLL locked on BCK $f_s = 16$ to 48 kHz | - | - | 2 | ms |
| | | PLL locked on FS $f_s = 48$ kHz | - | - | 6 | ms |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|------------------------|--|-----|-----|-----|---------|
| $t_{d(off)}$ | turn-off delay time | | - | - | 10 | μs |
| $t_{d(mute_off)}$ | mute off delay time | | - | 1 | - | ms |
| $t_{d(soft_mute)}$ | soft mute delay time | Coolflux DSP enabled | [3] | 120 | - | ms |
| t_{PD} | propagation delay | CoolFlux DSP bypassed $f_s = 48$ kHz | - | - | 600 | μs |
| | | SpeakerBoost protection mode, $t_{LookAhead} = 10$ ms, $f_s = 48$ kHz | - | - | 12 | ms |
| Current-sensing performance | | | | | | |
| S/N | signal-to-noise ratio | $I_O = 1.2$ A (peak); A-weighted | - | 75 | - | dB |
| ΔI_{sense} | current sense mismatch | $I_O = 0.5$ A (peak) | -3 | - | +3 | % |
| B | bandwidth | | [2] | 8 | - | kHz |
| L_L | load inductance | $R_L \leq 32 \Omega$ | 30 | - | - | μH |
| C_L | load capacitance | to ground | [4] | 200 | - | pF |

- [1] L_{BST} = boost converter inductor; R_L = load resistance; L_L = load inductance (speaker).
 [2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
 [3] The pilot tone is removed at the zero crossing after a soft mute, which takes on average 10 ms (20 ms max.) at a sample rate of 48 kHz and 15 ms (30 ms max.) at a sample rate of 16 kHz.
 [4] If a higher value is used, LPM should be disabled.

11.3 TDM/I²S timing characteristics

Table 11-3: TDM I²S bus interface characteristics; see Figure 11-1

All parameters are guaranteed for $V_{BAT} = 3.6$ V; $V_{DD} = 1.8$ V; $V_{DDP} = V_{BST} = 12$ V, adaptive boost mode; $L_{BST} = 1 \mu H^{[1]}$; $R_L = 8 \Omega^{[1]}$; $L_L = 40 \mu H^{[1]}$; $f_i = 1$ kHz; $f_s = 48$ kHz; $T_{amb} = 25$ °C; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-----------|-----------------------|-----------------------|-----|---------|-----|----------|-----|
| f_s | sampling frequency | on pin FS | [2] | 16 | - | 48 | kHz |
| f_{clk} | clock frequency | on pin BCK | [2] | $32f_s$ | - | $512f_s$ | Hz |
| t_{su} | set-up time | FS edge to BCK HIGH | [3] | 10 | - | - | ns |
| | | DATA edge to BCK HIGH | | 10 | - | - | ns |
| t_h | hold time | BCK HIGH to FS edge | | 10 | - | - | ns |
| | | BCK HIGH to DATA edge | | 10 | - | - | ns |
| t_j | external clock jitter | PLL locked on BCK | [4] | - | - | 2 | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------------|-------|-----|-----|------|
| | | PLL locked on FS | [5] - | - | 20 | ns |

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.

[2] The I²S bit clock input (BCK) is used as a clock input for the DSP, as well as for the amplifier and the DC-to-DC converter. Note that both the BCK and FS signals need to be present for the clock to operate correctly.

[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

[4] When the PLL is locked on BCK, amplifier output noise can deteriorate when clock jitter > 1 ns.

[5] The system is less sensitive to jitter when the PLL is locked on FS.

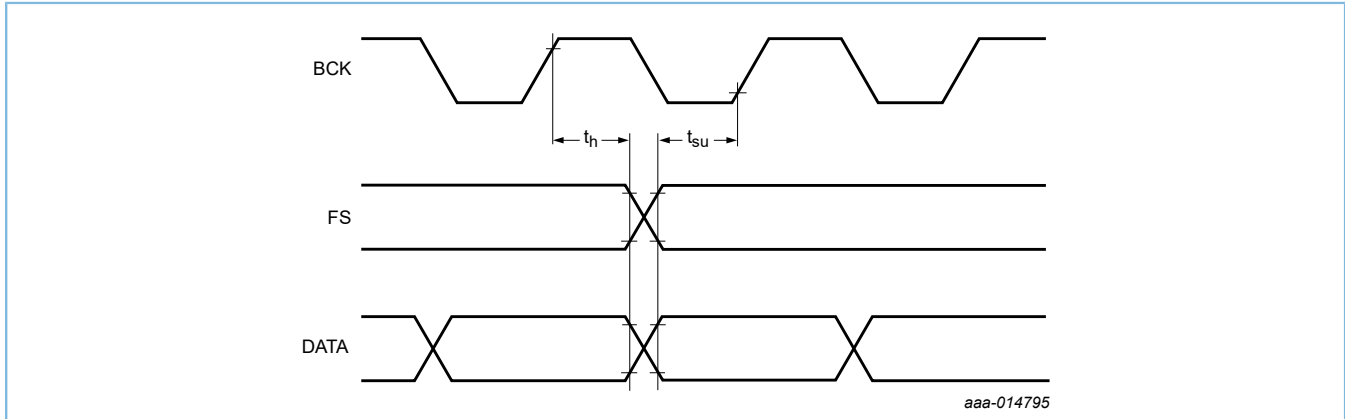


Figure 11-1: TDM/I²S timing

11.4 I²C timing characteristics

Table 11-4: I²C-bus interface characteristics; see [Figure 11-2](#)

All parameters are guaranteed for $V_{BAT} = 3.6\text{ V}$; $V_{DD} = 1.8\text{ V}$; $V_{DDP} = V_{BST} = 12\text{ V}$, adaptive boost mode; $L_{BST} = 1\text{ }\mu\text{H}^{[1]}$; $R_L = 8\text{ }\Omega^{[1]}$; $L_L = 40\text{ }\mu\text{H}^{[1]}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; default settings, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|--|---------------------|--------------------|-----|-----|---------------|
| f_{SCL} | SCL clock frequency | | - | - | 400 | kHz |
| t_{LOW} | LOW period of the SCL clock | | 1.3 | - | - | μs |
| t_{HIGH} | HIGH period of the SCL clock | | 0.6 | - | - | μs |
| t_r | rise time | SDA and SCL signals | [2] $20 + 0.1 C_b$ | - | - | ns |
| t_f | fall time | SDA and SCL signals | [2] $20 + 0.1 C_b$ | - | - | ns |
| $t_{HD;STA}$ | hold time (repeated) START condition | | [3] 0.6 | - | - | μs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 0.6 | - | - | μs |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---|------------|-----|-----|-----|---------|
| $t_{SU;STO}$ | set-up time for STOP condition | | 0.6 | - | - | μs |
| t_{BUF} | bus free time between a STOP and START condition | | 1.3 | - | - | μs |
| $t_{SU;DAT}$ | data set-up time | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | - | - | μs |
| t_{SP} | pulse width of spikes that must be suppressed by the input filter | [4] | 0 | - | 50 | ns |
| C_b | capacitive load for each bus line | | - | - | 400 | pF |

- [1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
- [2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
- [3] After this period, the first clock pulse is generated.
- [4] To be suppressed by the input filter.

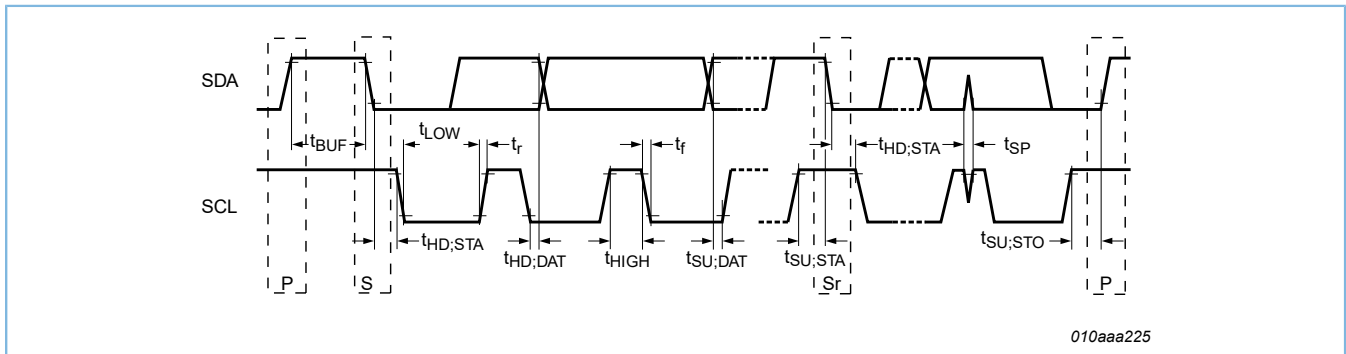


Figure 11-2: I²C timing

12 Application information

12.1 Application diagrams

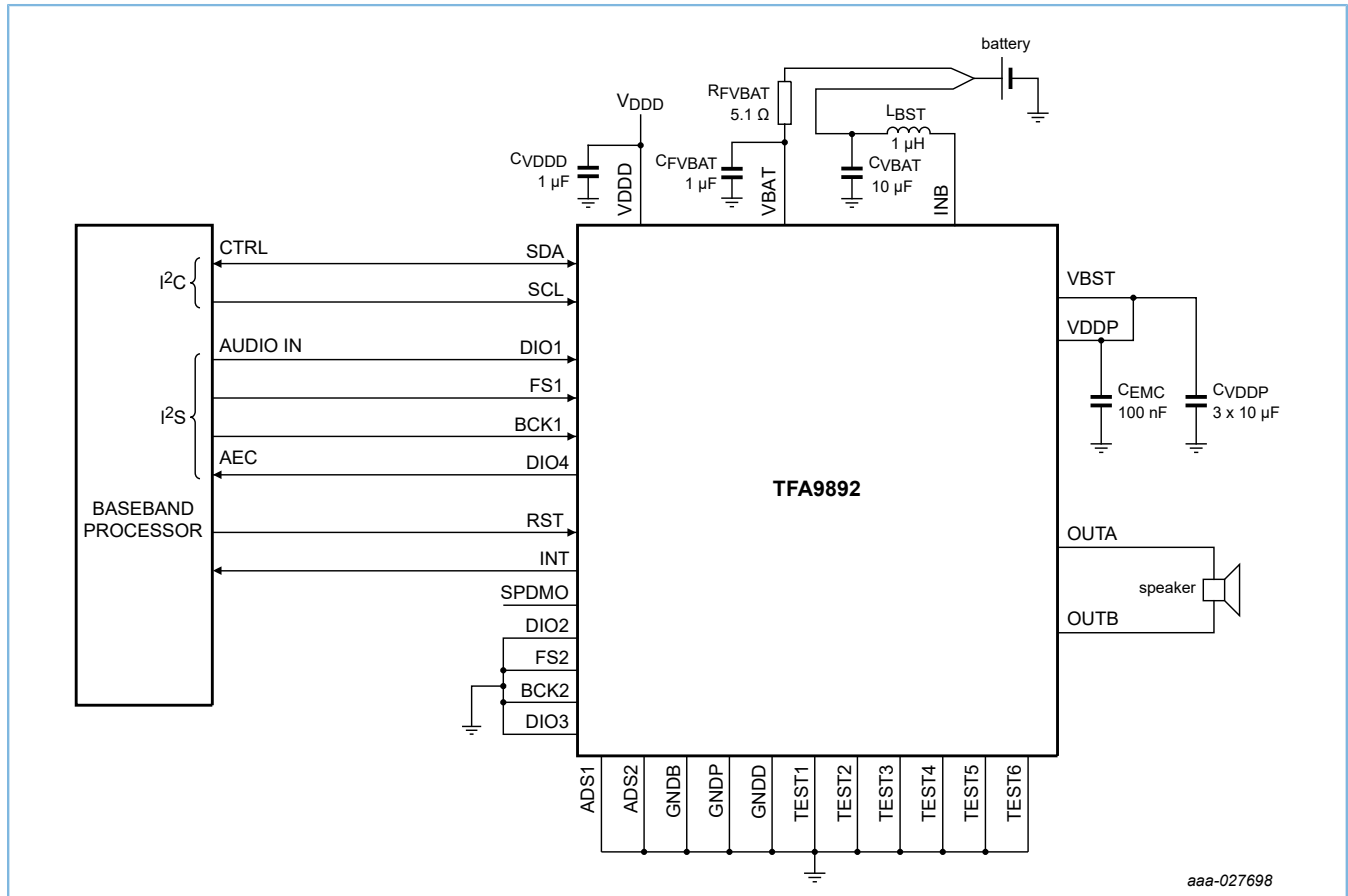


Figure 12-1: Typical mono application

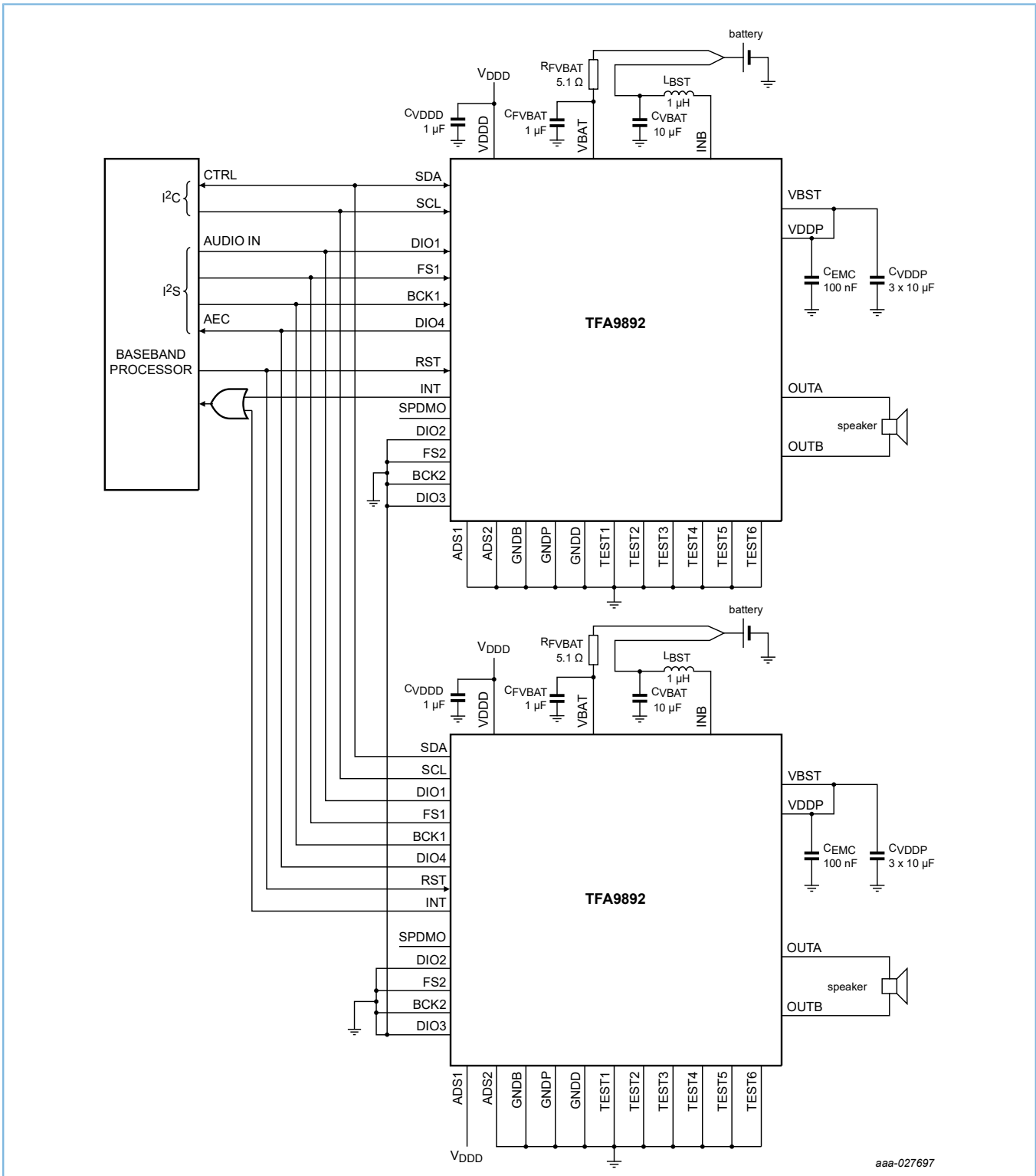


Figure 12-2: Typical stereo application

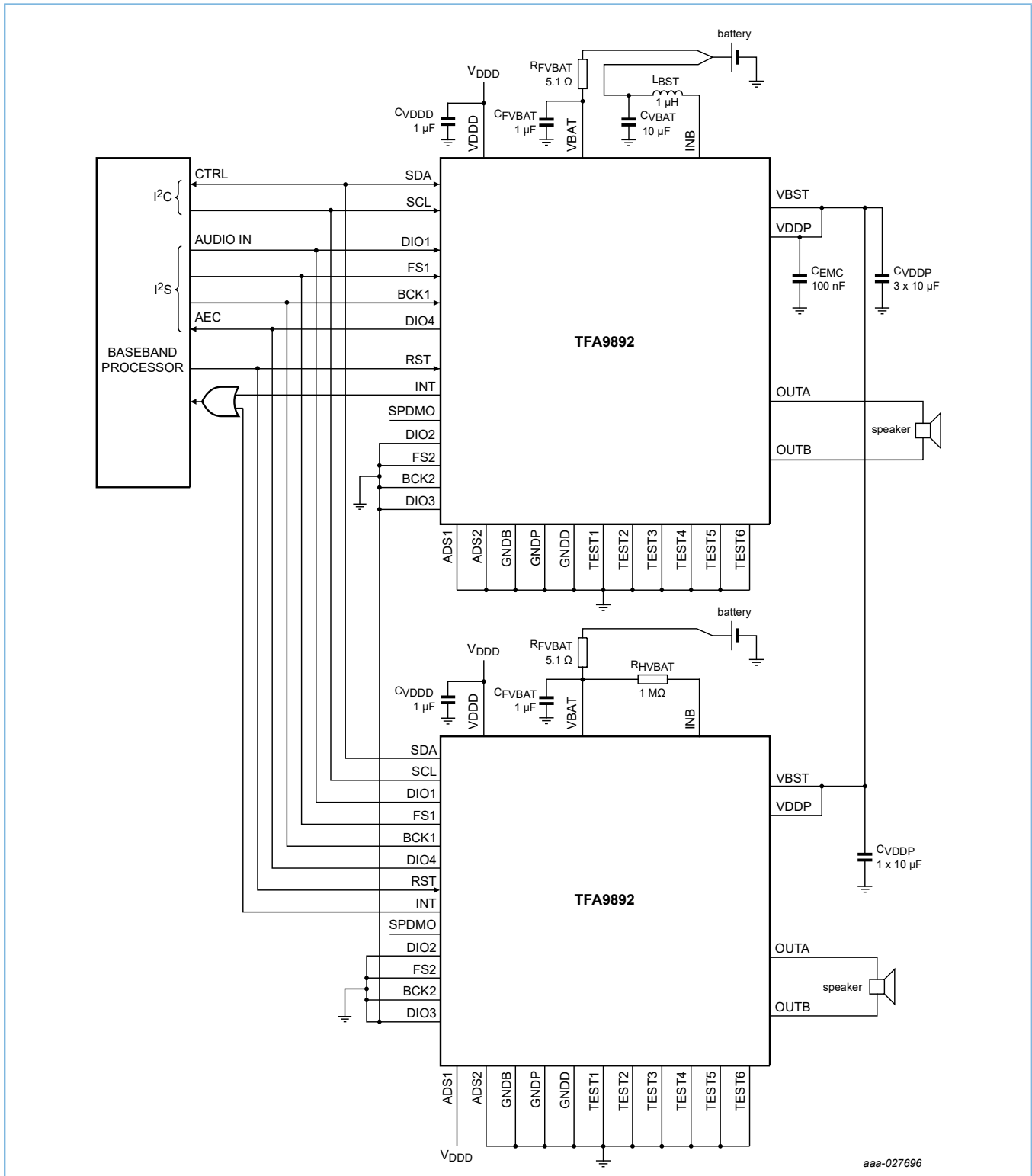


Figure 12-3: Stereo application using single coil

13 Package outline

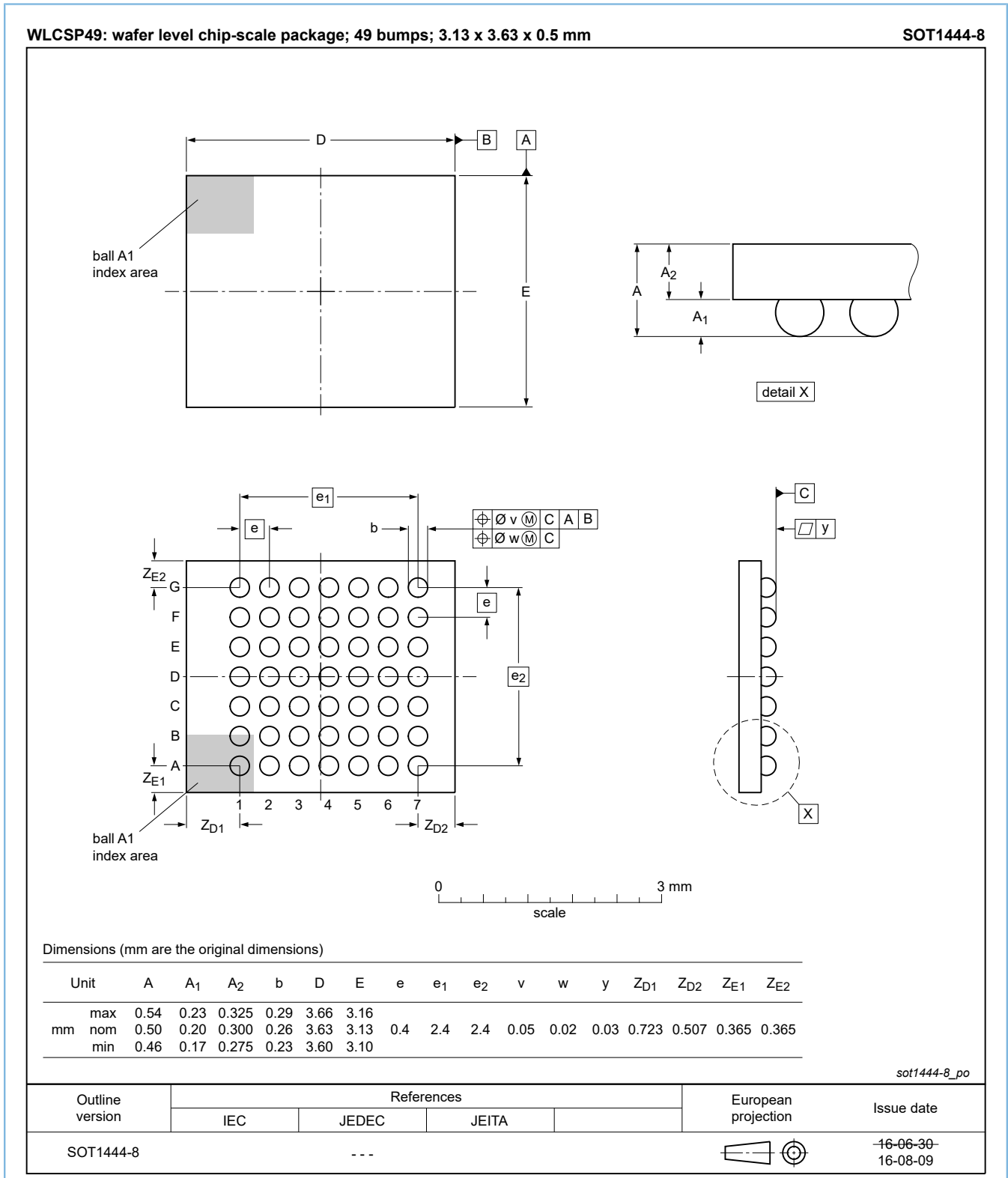


Figure 13-1: Package outline TFA9892AUK/N1 (WLCSP49)

14 Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. More information about handling, packing, shipping and soldering of moisture/reflow sensitive surface-mount devices can be found in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

Wave soldering is not suitable for this package.

All Goodix WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 14-1](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14-1](#).

Table 14-1: Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|--------------|---------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2 000 | > 2 000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 14-1](#).

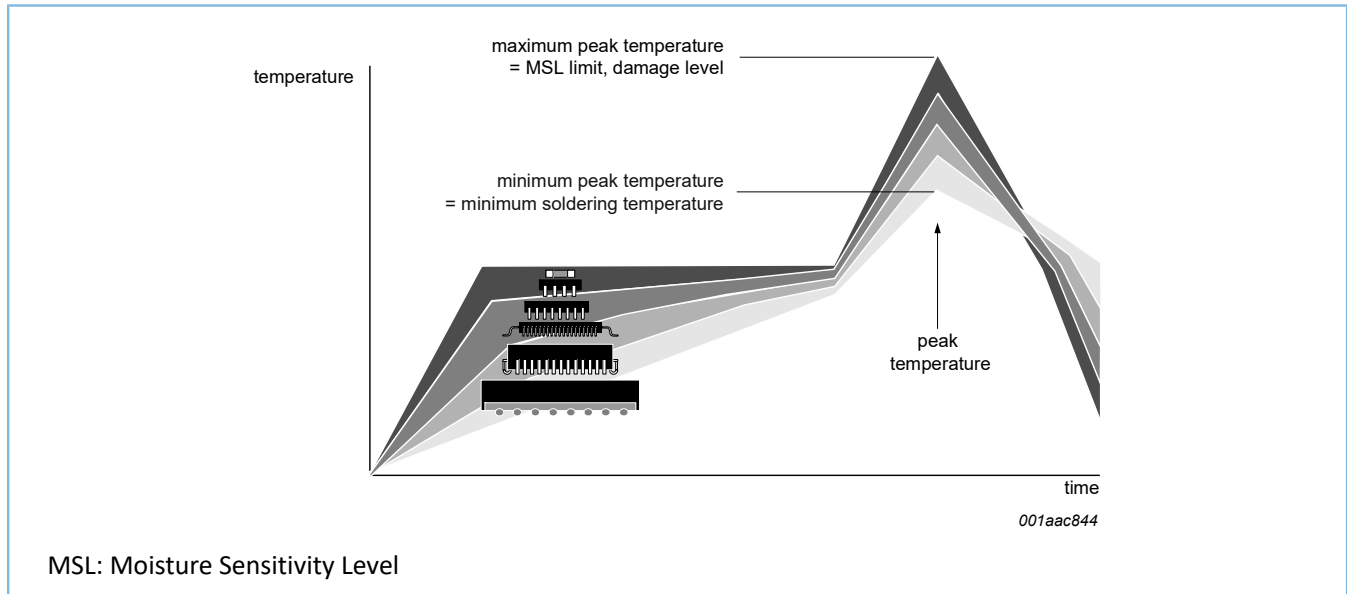


Figure 14-1: Temperature profiles for large and small components

For further information on temperature profiles, refer to IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in IPC/JEDEC J-STD-033 and IPC/JEDEC J-STD-020.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15 Legal and contact information

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16 Revision history

Table 16-1: Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|--------------------------|---------------|-----------------|
| TFA9892_SDS v 2.0 | 20200121 | Product short data sheet | - | TFA9892_SDS v.1 |
| Modifications: | • Updated document format based on Goodix template | | | |
| TFA9892_SDS v.1 | <td> | Product short data sheet | - | - |